Lecture 15
The Forward PWM Converter Circuit Topology and Illustrative Examples

I. Erickson Problem 6.4 A DCM Two Transistor Flyback Converter

II. Forward Converter

A. Overview

B. Forward Converter with a Three Winding Transformer Drive: Two Case Studies

1. One Transistor Implementation
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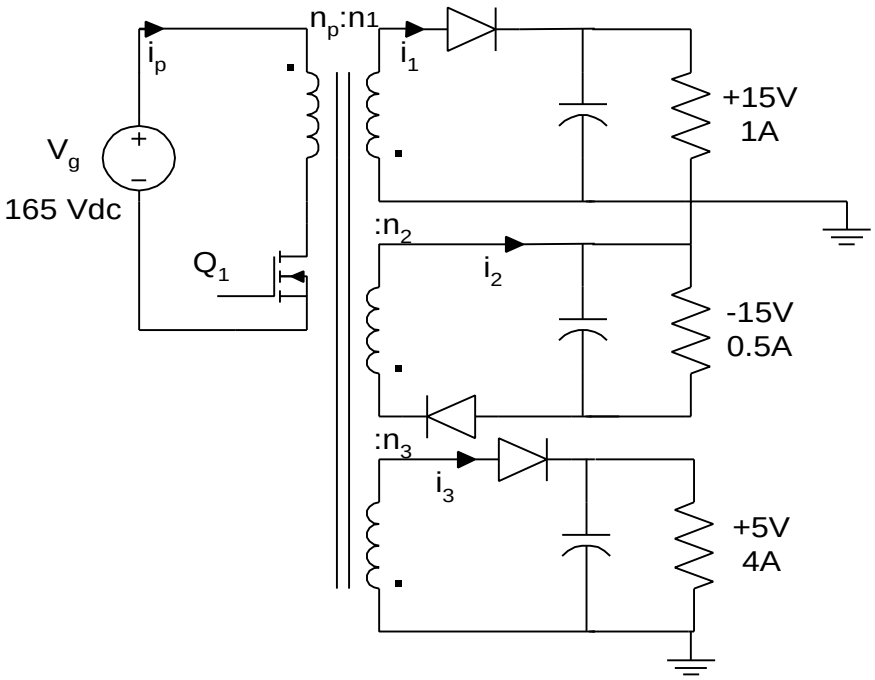
Forward PWM Converter Circuit Topologies

I. Erickson Problem 6.4 A DCM Two Transistor Flyback Converter

b) Erickson Problem 6.10: One transistor Flyback implementation in the DCM mode of operation.

We will consider only DCM operation below:



Note the ability to provide ±15 V as well as +5 easily. If we employed feedback for V_o stabilization we could use just one of the three V_o to monitor and slave the other two. WHAT OTHER WAY IS POSSIBLE??

Neglect:

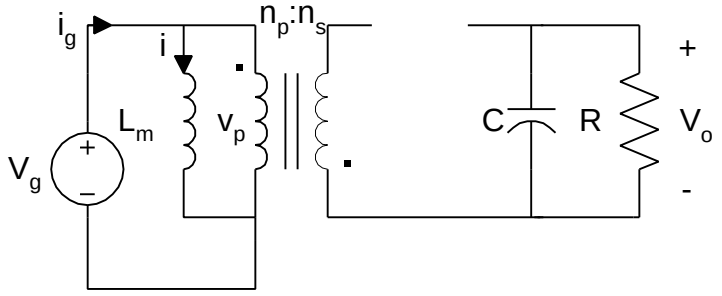
1. All losses in the electronic circuits.
2. No magnetic core losses.

Also for this problem we arbitrarily set the specification V_g is fixed

and i_{load} is fixed for the DCM operation.

We expect given 3 DCM time intervals: D_1, D_2, D_3 but we arbitrarily fix $D_3 = 0.1 \Rightarrow D_2 = 0.9 - D_1$.

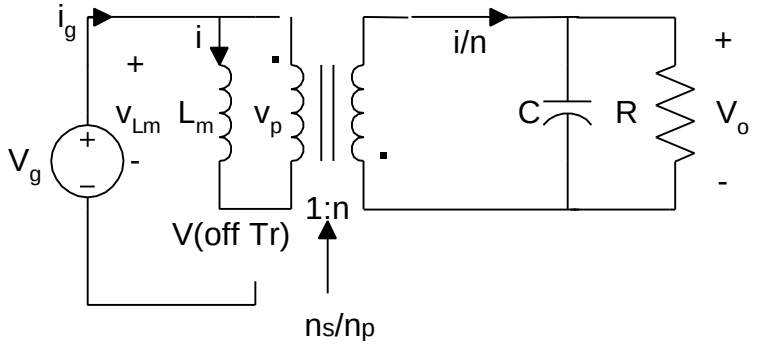
Goal: Find steady state design, where the V(off) blocking voltages are minimum for both the transistors (< 300 V) and diode (< 30 V) solid state switches.
Below we give circuit conditions for each time interval.
Interval D_1T_s: Control signal puts Q_1 on and using current flow dot's on the transformer we see that all three diodes in the secondary are off.



$V_{Lm} = V_g$ $\qquad$ $i_c + i_R = 0$

$i = i_g$ $\qquad$ $i_c = -\frac{V_o}{R}$

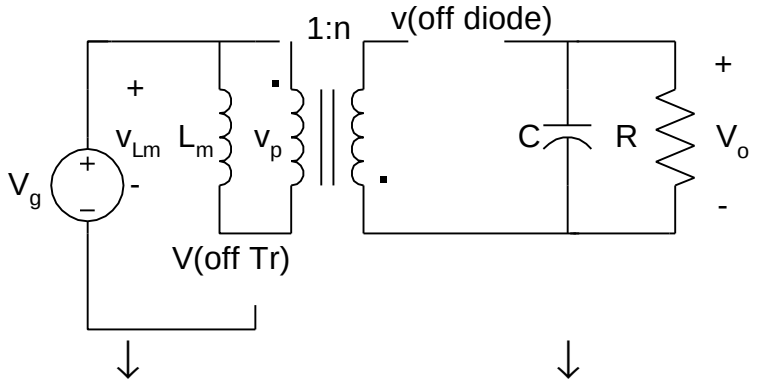
Interval D_2T_s: Control signal puts Q_1 off, all secondary diodes conduct using current flow dots on the transformer.



$i_g = 0$ $\qquad i_c = \frac{i}{n} - \frac{V_o}{R}$

$V_L = \frac{V_o}{n} = V(\text{primary})$

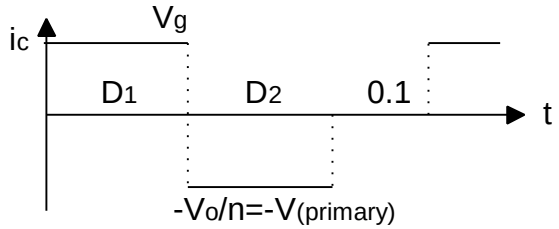
Period D_3T_s: Q_1 off, all secondary diodes off V(off diode)



$V_{Lm} = 0$ $\qquad i_r + i_c = 0$

$i_g = 0$ $\qquad i_c = -\frac{V_o}{R}$

Draw i_c waveform versus time using the above circuits to determine values of i_c for each interval.



Remember $-\frac{V_o}{n} = -V(\text{primary})$ for all ac conditions encountered.

Applying volt-sec balance to the L_m inductor:

$\langle V_{Lm} \rangle_{Ts} = 0 \quad D_1V_g + D_2(-V_p) + 0 = 0$

$$D_1 V_g = (0.9 - D_1) V_p$$

$$D_1 (V_g + V_p) = .9\, V_p$$

$$D_1 \leq \frac{.9\, V_p}{V_g + V_p}$$, setting an upper bound on D_1.

For cost considerations we limit maximum voltages to the switches as follows:

Choose: Transistor: $V_{off} < 300$ V
Diode: $V_{off} < 30$ V

$300 - V_p + V_g$ from primary circuit and transistor maximum standoff voltage spec.

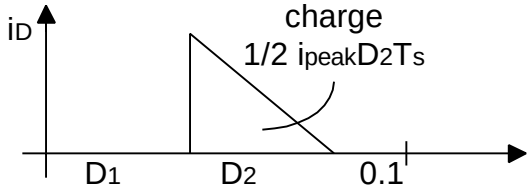
$V_p = 300 - V_g(165) = 135$

$$D_1 \leq \frac{0.9(135)}{300} = 0.405$$

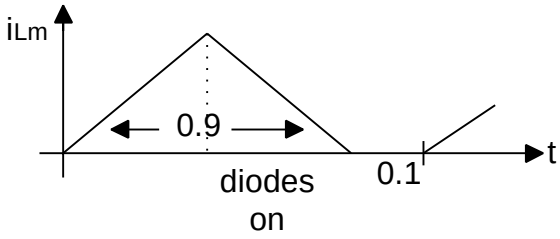
Pick $D_1 = 0.4 \Rightarrow D_2 = 0.5$ Try this 1st choice and see the effect.

Diode currents for all three secondaries which are similar in time.

Three diode currents each have a unique charge passed through them during $D_2 T_s$.



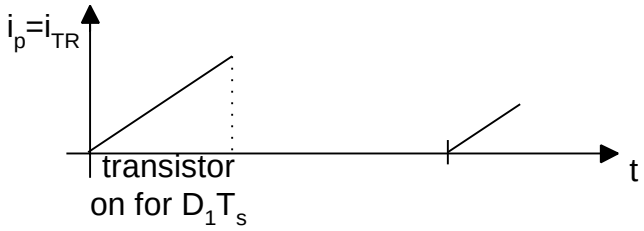
Current flow in L_M is on for 0.9 T_s, given D_3 fixed at 0.1.



Notice the fact that for the buck-boost and flyback:

i_{Lm} = i(diode) + i(transistor)

The corresponding current in the transistor and the primary winding is:



Remember i_D is secondary current, whereas i_{Lm} is the primary current.

<u>Values of Diode Peak Currents:</u> (Given chosen maximum off voltages)

$$i_{D1}(\text{peak}) = \frac{2\,i_{D1}(\text{DC})}{D_2} = \frac{(2)(1)}{0.5} = 4\,\text{A}$$

$$i_{D2}(\text{peak}) = \frac{2\,i_{D2}(\text{DC})}{D_2} = \frac{(2)(\frac{1}{2})}{0.5} = 2\,\text{A}$$

$$i_{D3}(\text{peak}) = \frac{2\,i_{D3}(\text{peak})}{D_2} = \frac{(2)(4)}{0.5} = 16\,\text{A}$$

We must check that each diode can carry these current levels from the diode manufacturer spec. sheets.

Peak I_{Lm} is worth calculating because hysteresis core loss varies

with peak current, not rms current.

$$i_{Lm}(\text{peak}) = \sum i_{Dx} * 1/n_x$$

i_{Lm}(peak): primary current; $\sum i_{Dx}$: secondary diode currents

$$n_1 = \frac{15}{135} = \frac{V}{V_p}, \quad n_2 = \frac{15}{135} = \frac{V_2}{V_p}, \quad n_3 = \frac{5}{135}$$

$$i_{Lm}(\text{peak}) = \frac{4}{9} + \frac{2}{9} + \frac{16}{27} = 1.26\,\text{A}$$

We must check that this peak current does not saturate the magnetic core.

<u>Transistor peak current</u>

$$i_{TR}(\text{peak}) = i_{Lm}(\text{peak}) = 1.26\text{A}$$

$$V_{Lm} = L_m \frac{di_{Lm}}{dt}$$

$$i_{Lm}(\text{peak}) = \frac{V_{Lm}}{L_m} D_1 T_s = \frac{V_g}{L_m} D_1 T_s$$

(165 → V_g; .5 → D_1; 10^{-5} → T_s)

i_{Lm} depends on L_m values. The L_m value of the chosen transformer is set by the peak transistor current.

$$L_m = \frac{V_g}{i_{peak}} D_2 T_s = \frac{(165)(.4)}{1.26} 10^{-5}$$

$$= 0.52\ \text{mH}$$

Calculate I_{RMS} using the above current waveforms and Appendix 1 on pg. 705 of Erickson's text.

$$[I_X(\text{output})]_{RMS} = \sum_x i_{Dx}(\text{peak}) * \sqrt{\frac{D_2}{3}}$$

x = 1-3 for the three secondary windings.

$I_1(\text{rms}) = 4 * .41 = 1.63$

$I_2(\text{rms}) = 2 * .41 = 0.81$

$I_3(\text{rms}) = 16 * 41 = 6.53$

$$I_{Lm}(\text{rms}) = i_{Lm}(\text{peak}) \sqrt{\frac{D_1 + D_2}{3}} = 0.69\ \text{A}$$

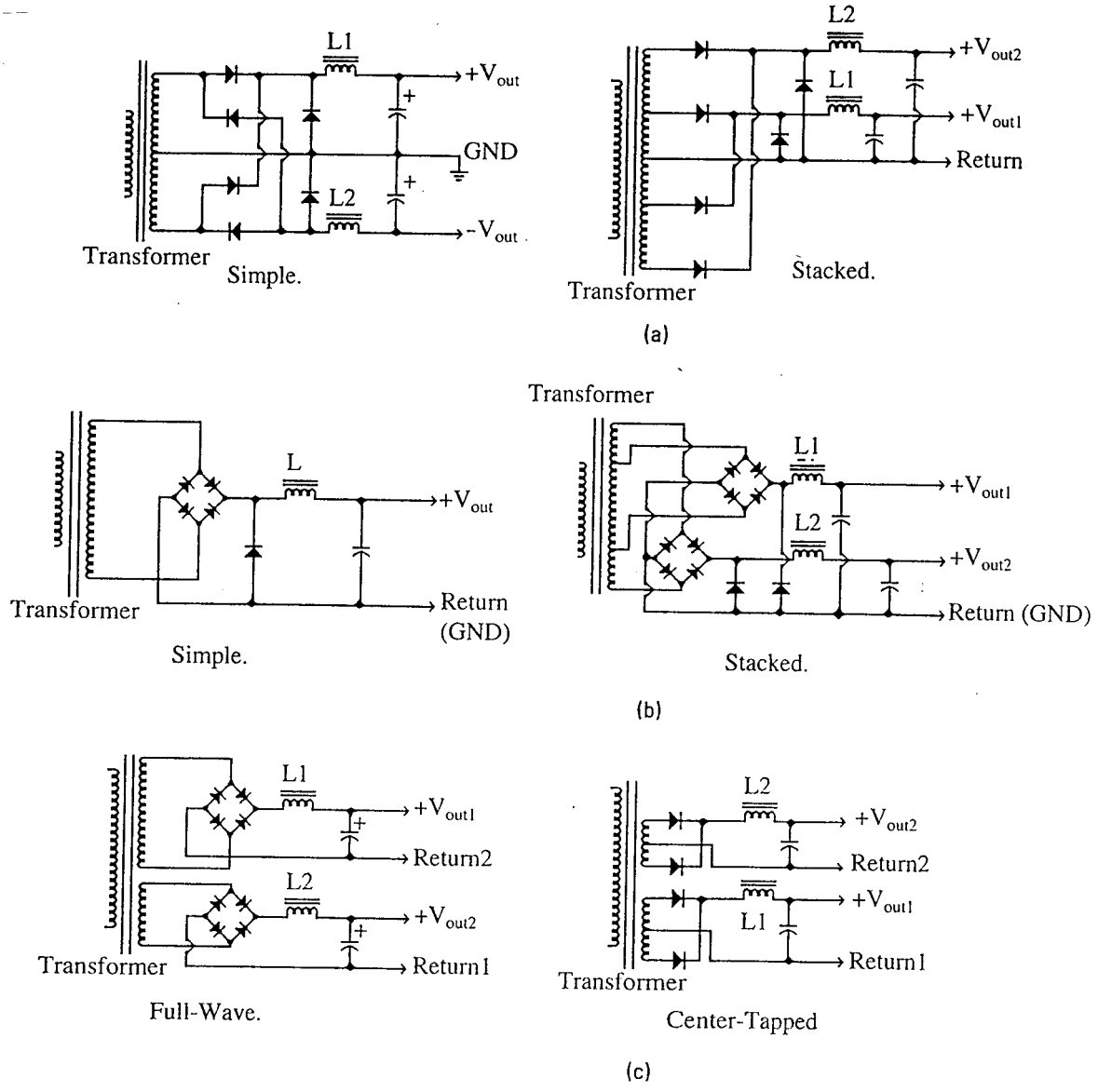
II. Forward Converters

A. Overview

Here we choose in the circuit topology the dots on the transformer coils and the primary / secondary diode placement so that when primary current flows so will secondary current unlike the flyback converter. Hence, the name forward converter. Three secondary arrangements for the forward converter are given below:

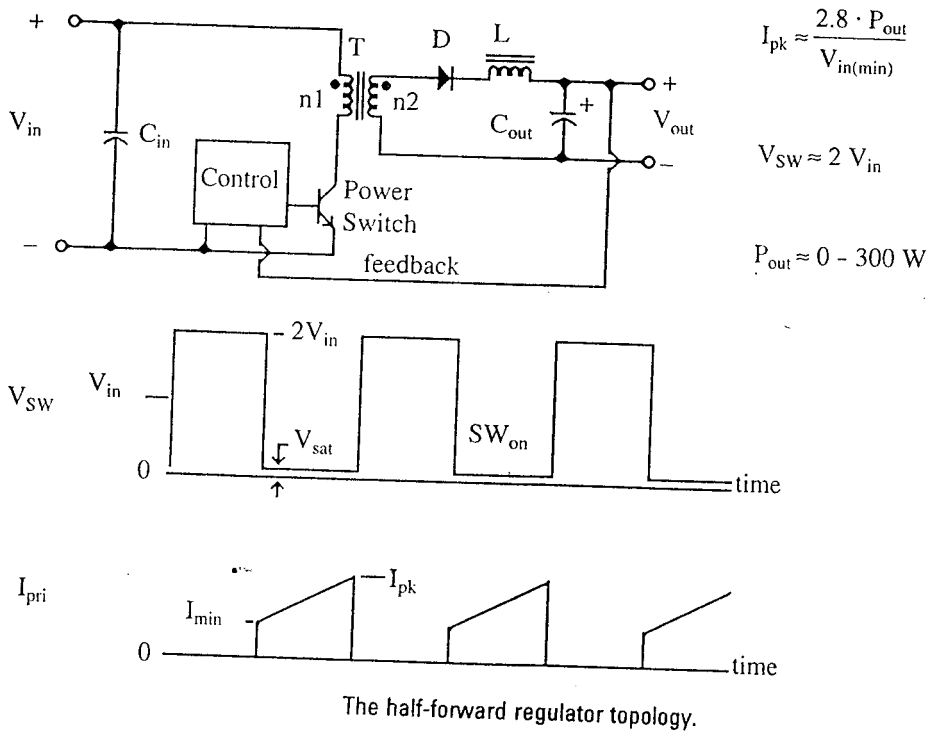
- Simple center tapped transformers are the key elements to one approach
- Full wave rectification without isolation of the secondary voltages and without center taps is a second approach to the forward converter topology
- Fully isolated secondaries without center taps with full wave rectification is the third topology approach

Note that in all cases the transformer has the role of dielectric isolation, which is accomplished by the choice of isolation material between wire windings on the transformer. The winding turns ratio provides the step up or step down ratio desired. There is no air gap in the core so the forward transformer stores no energy, it merely transfers energy form the primary coil to the secondary coil. Of, course we must never allow the peak flux in the transformer core to EXCEED THE SATURATION VALUE of the chosen core. **Forward converters posses both a transformer and an output choke** and this distinguishes them from flybacks of lecture 14.



Forward-mode secondary winding arrangements: (a) center-tapped secondaries; (b) full-wave secondaries; (c) isolated secondaries.

On the next page we will outline the voltage and current waveforms in a simple half-wave forward converter to give a clear picture of the unipolar drive that occurs in each portion of the transformer secondary that is synchronous with the primary drive sequence. In full wave center tapped operation each half of the transformer sees similar waveforms. The full wave rectification in the secondary insures that the current waveforms are unipolar as does half-wave rectification.



The half-forward regulator topology.

Notice that the output circuit of an L-C filter directly after the power switch or output rectifier is the CALLING CARD of the forward converter. This is clearly a BUCK-LIKE TOPOLOGY with V_{out} being proportional to D x V_{in}.

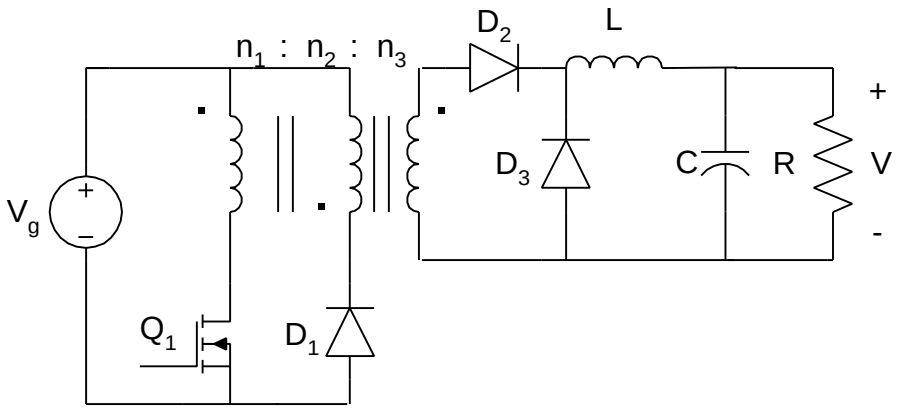
B. DCM Forward Converter Operation: Two Case Studies

On the following pages we will outline the operation of froward converters operating in the DCM of operation via two illustrative examples. One will employ a single transistor switch while the second will employ two temporally synchronized switches. DCM operation is more complex than CCM operation due to the third time interval that is introduced into the switching period, T_{sw}.

1. DCM operation using only one transistor I_{out} is non-pulsating for a fixed load and the L-R-C filtering.

For the Forward Converter notice that: buck- like operation occurs in the secondary circuit to the right of diodes "D_2" and "D_3".

To start with, for the dotted transformer windings always assume all currents flow into the dots and $n_1i_1 + n_2i_2 + n_3i_3 = 0$.



If the input, or primary, current flow direction is known by circuit means to flow the opposite to that initially assumed then this reverse flow occurs also at other coils. The dotted side specifies which way current flows.

DCM operation has three intervals in T_s of duration D_1, D_2 & D_3. i_{Lm} is reset to zero so that saturation of the magnetic core does not occur as follows, in DCM operation.

Interval D_1T_s: Q_1 and diode "D_2" conduct creating simultaneous primary and secondary transformer currents while diodes "D_1" and "D_3" are off again by current flows.

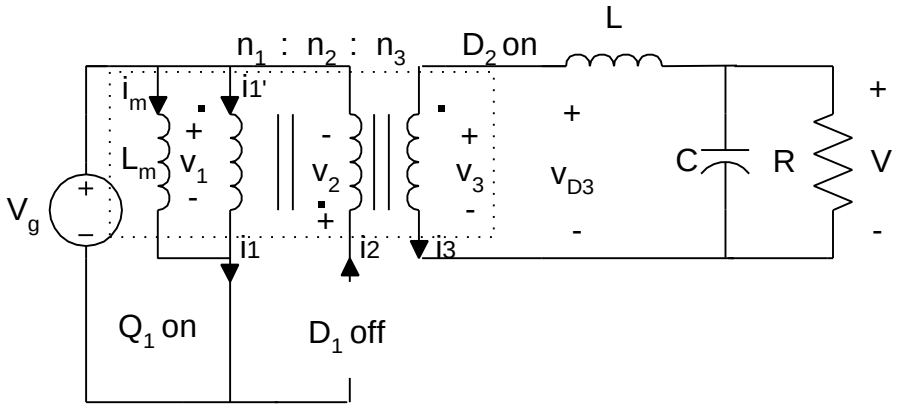
All currents are assumed into the dots of all windings.

a) When Q_1 is on $+V_g$ appears across n_1
b) A voltage of polarity $-V_g\, n_2/n_1$ appears across turn $n_2 \Rightarrow D_1$ is off. This is also seen by current flow. i_1 flows into dot of

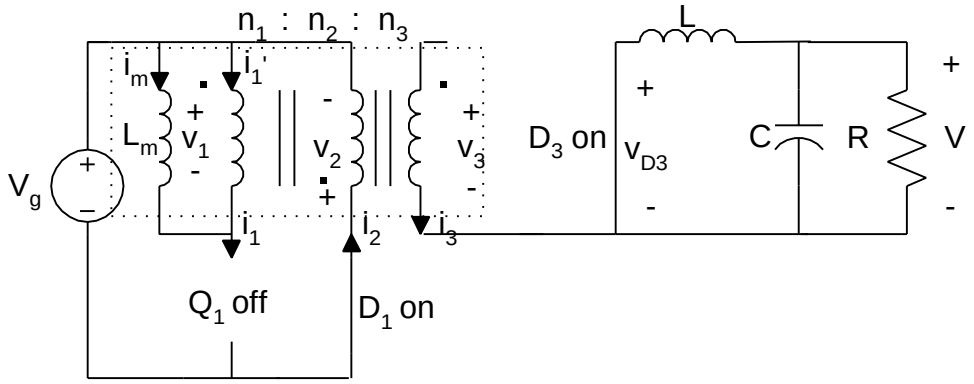
coil #1 $\Rightarrow$ i_3 flows out of the dot of coil #3 and D_2 is on.

c) $+V_g\ n_3/n_1$ appears across turn n_3 $\Rightarrow$ diode D_2 is on drawing a secondary current which appears in the primary as i_1'. Then the current drawn from V_g is $i_1 = i_m + i_1$'.

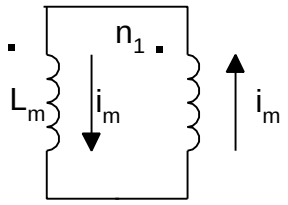
Note that the primary is composed of the magnetizing inductance in parallel with the n_1 winding as per the standard transformer model. Coil #2 is open because of diode D_1 being off.



Interval D_2T_s: Q_1 is put off actively by the control signal forcing a current loop in L_m and the n_1 coil. This causes current to flow out of the n_1 coil at the dotted end, and current flows into the dotted end of the n_2 coil.



i_m now flows in the n_1 winding as shown exiting the dot of the n_1 coil. The n3 coil has current flow into the dotted end.



In total then the conservation of mmf gives:
$-n_1i_1 + n_2i_2 - n_3i_3 = 0$
+ sign is into dot
- sign is out of dot

i_2 and i_3 coil current directions are as assumed but i_1 is known to flow out of the dot of the n_1 coil due to Q_1 being off during the i_1 time interval D_2T_s. Due to the current flow direction we can say that during D_2T_s:

- Q_1 is off and diodes D_1 and D_3 are on whereas diode D_2 is off as shown above.
- Diode D_1 is <u>on</u> because of current flow into the dot of winding n_2 which turns D_1 on.
- Diode D_2 is <u>off</u> because of current flow into the dot of winding n_3 which turns diode D_2 off.
- Diode D_3 is <u>on</u> because of current flow into the dot of winding n_3 equals i_3 out of undotted n_3 turning D_3 on.

With diode D_1 on we have:

<u>INPUT</u>	<u>OUTPUT</u>
$+V_g$ across n_2 coil so by the dot convention	Current i_3 as shown flows from the n_3 coil to the output

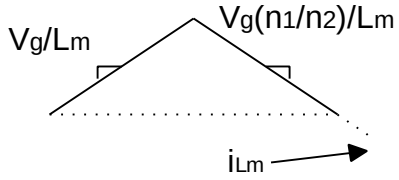
$$V_{Lm} = -V_g \frac{n_1}{n_2}$$

and this negative voltage across L_m causes the magnetizing current to decrease with a slope di/dt: $\frac{n_1}{n_2}\frac{V_g}{L_m}$

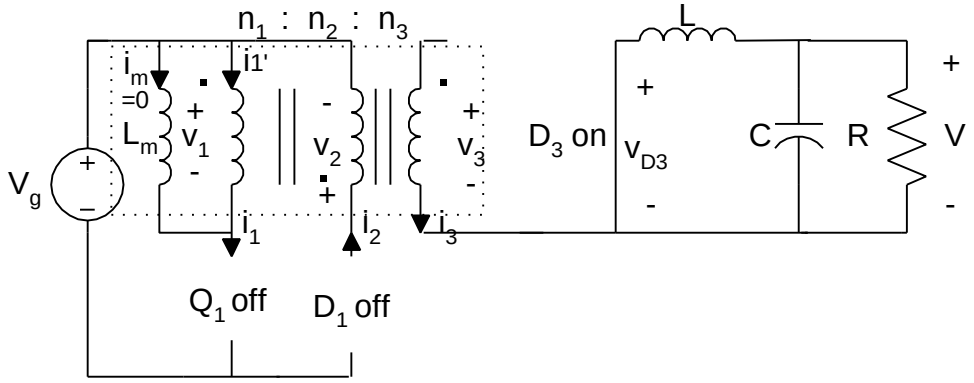
Note also that in the primary we have the sum of two voltages across the transistor. $[V_{Tr}(\text{off})]_{max} = V_g[1 + \frac{n_1}{n_2}]$

Interval D_3T_s: i_{Lm} will try to reverse sign after the time period D_1T_s going up and the time period D_2T_s going down as shown below in the i_{Lm} plot versus time.

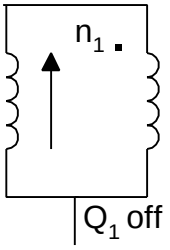
$\frac{V_g}{L_m}$ (upslope) $V_g \frac{n_1/n_2}{L_m}$ (downslope)



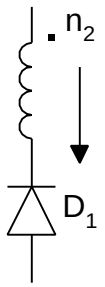
First i_{Lm} hits zero then i_{Lm} tries to go negative. At this point a new circuit topology arises as diode D_1 goes off and diode D_3 goes on.



If i_{Lm} now goes negative with Q_1 off then the dot convention tells that the i_{Lm} current loop now enters the n_1 winding from the dotted side in the current loop seen below.



This current flow direction for i_1 causes i_2 to also try to flow into the dotted side of coil #2 as shown below:



But i_2 tries to flow out but diode D_1 does not allow this direction of current flow. So diode D_1 goes off.

Likewise i_{Lm} flow into n_1 dot $\Rightarrow$ current flow into the n_3 dot and D_3 is turned on when i_{Lm} hits zero.
Since both transistor Q_1 and diode D_1 are off i_{Lm} remains zero for the whole period D_3T_s.
A tradeoff must be made in the forward converter since:

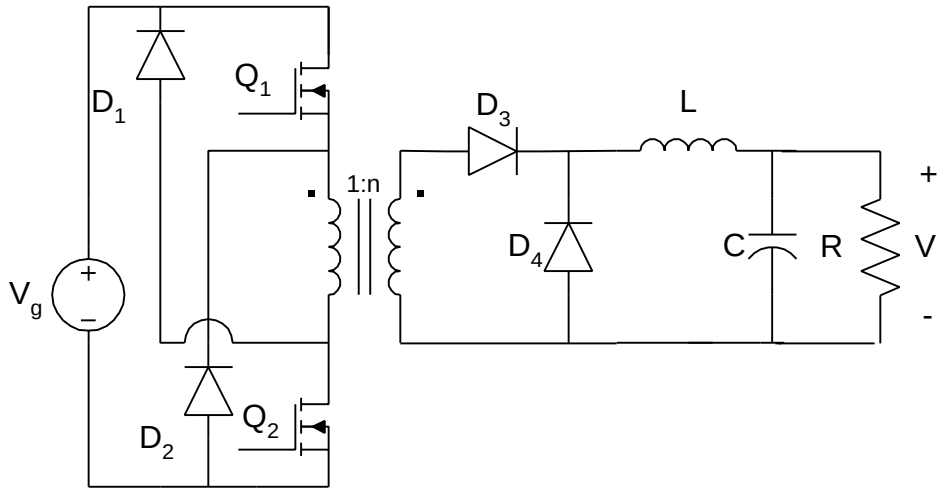
$D_2 = \frac{n_2}{n_1} D_1$ moving the turns ratio $\frac{n_2}{n_1}\downarrow$ allows the interval $D_1\uparrow$ for fixed interval D_2

BUT $\frac{n_1}{n_2}\uparrow$ implies that the standoff voltage across the transistor increases since:

$V_{Tr}(\text{off}) = V_g[1 + \frac{n_1}{n_2}]$ So we trade off decreased Tr on time D_1 for increased voltage stress.
This transistor switch voltage stress may be too much for one transistor to work in its safe operating area (SOA). Below we show a way to solve this by utilizing two rather than one switch and dividing the switch stress between them.

2. Two transistor implementation of the Forward Converter operating in DCM operation.

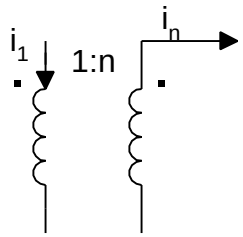
What do you guess the phasing of Q_1 and Q_2 gate control is?



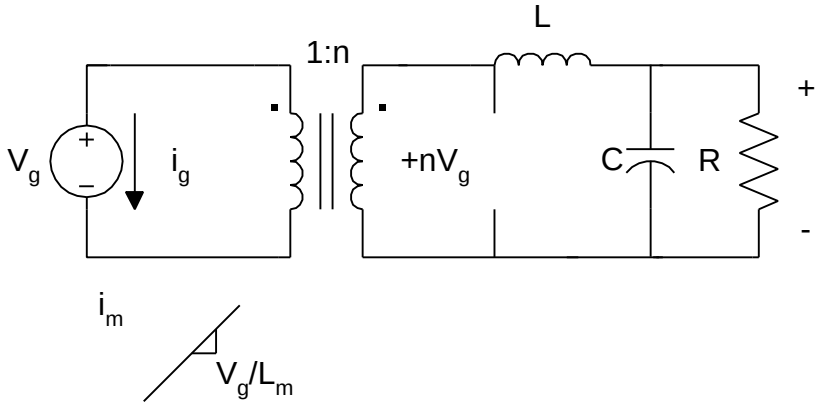
The tandem transistors Q_1 and Q_2 have the same phase gate control. So they are both in the same state.

Here our L_m is considered large as the core has no slotted opening and the core magnetic reluctance is low. Although i_{Lm} is small we still we need to consider L_m effects.
Now the primary voltage when Q_1 and Q_2 are both off can be dropped across the two transistors as both are in series, reducing switch stress to more allowable levels.

Interval D_1T_s: Control signal forces both Q_1 and Q_2 on, primary diodes D_1 and D_2 are both off. Current flow is such that i_1(primary) flows into the dot end of the one turn coil so i_2 flow is out of the secondary winding of n turns. The secondary current is 1/n of the primary current.

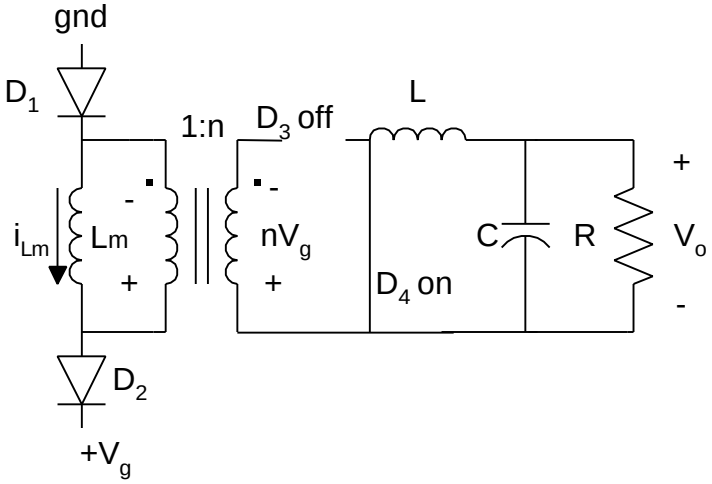


when i_1 flows into the dot on winding 1 a current i_1/n flows out of the dot on the n turn winding as shown above. This insures that diode D_4 is off and diode D_3 is on.

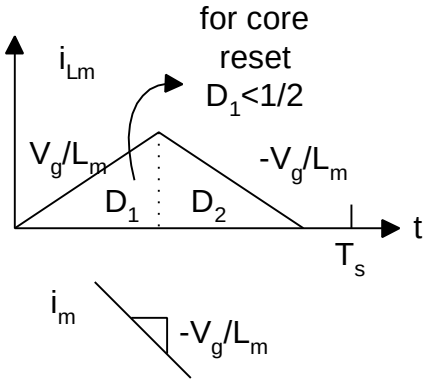


The current in L_m increases linearly during switch interval D_1 with a slope V_g/L_m.

<u>Interval D_2T_s</u>: The external control signal forces both Q_1 and Q_2 off. Both primary diodes D_1 and D_2 are on as shown below during the interval D_2T_s driving the magnetizing current down during time D_2T_s.



Note that i_{Lm} flow is always positive with respect to zero during intervals D_1 and D_2. It first rises during D_1T_s and then falls during D_2T_s as shown below.
What occurs if i_{Lm} does not reach zero?



The i_{Lm} current period as shown in DCM of operation could lead over a few switch cycles to core saturation if i_{Lm} did not return to zero. DCM operation, however, guarantees that this occurs. If i_{Lm} tries to go negative, then diodes "D_1" and "D_2" go off and prevent it from doing so.

Setting/Fixing $i_{Lm} = 0$ so the core doesn't saturate

We will find below in part 3 for i_{Lm} to <u>reset</u> the transistor on time $D_1 < ½$ is required. Is this clearly why?

<u>Period D_3T_s</u>: Q_1, Q_2, as well as diodes D_1 and D_2 are all off in the primary circuit
$i_{Lm} = 0$, $V_{primary} = 0$

C. Forward Transformer Overview

As stated earlier we must never allow the flux density, B, in the forward converter core to exceed the saturation flux for that core. If we do, the transformer will look like a short circuit and no doubt fry the power switches. We will employ Faraday's law to see the trends between transformer core size and the choice for the

number of turns in the windings.

V(out) = N(# turns of wire) x ω(radian frequency)x ϕ(flux)

Where ϕ(flux) given by is given by B(flux density)x A_{core}(core area)

Now each core material has a maximum allowable flux density that it can handle before the onset of core saturation. Hence, we can say that there is a required number of turns on the transformer windings. Consider first the primary windings. We will find below the result that N varies inversely with B_{max}(saturation value).

$$N_{primary} = V_{primary} /(\omega \times B_{max} \times A_{core})$$

That is the MINIMUM number of primary winding turns varies as:

- the input voltage level $V_{primary}$
- Inversely with operating frequency
- Inversely with the saturation flux of the core
- Inversely with the core size

Clearly, there is lots of design tradeoffs to be considered. Regardless, once the number of primary winding turns is set this acts as the reference for all other secondary winding turn choices as described below.

The secondary turns are unique for each secondary voltage desired. We start with the secondary that requires the most output power. The voltage across the output rectifers should also be accounted for. The starting point for all such calculations is the fact that the voltage in a specific winding divided by the number of turns in that winding must be equal to the output voltage of another winding divided by its number of turns. Finally, we have to consider worst case when the input voltage is minimum, V_{in}(min), and the duty cycle is maximum, D_{max}.. That is we find the relationship:

$$N_{secondary} = \frac{N_{primary} \times (V_{out} + V_{diode})}{V_{in}(max) \times D_{max}}$$

We solve for N_{sec} at lowest V_{in} and highest D we expect to occur.

The result is always a non-integer number and one must round off to the nearest number of turns. This could result in the output voltage being not what we desire. Again an iterative process is required to meet all desires. Note that adding secondary turns on the primary winding will always move you in the safe direction of a lower flux density, below the dangerous B(saturation)

D. DCM Forward Converter with External Reset to actively avoid core saturation.

Next we explain how to actively achieve L_m core reset by use of an external voltage source, with the secondary goal of causing less standoff voltage stress for both Q_1 and diode D_2. Also the duration D_1T_s can be increased so for a fixed D_2T_s:

$D_2 = \frac{n_3}{n_1} D_1 \Rightarrow \frac{n_3}{n_1}$ can be reduced if D_1T_s increases. Why is this good?

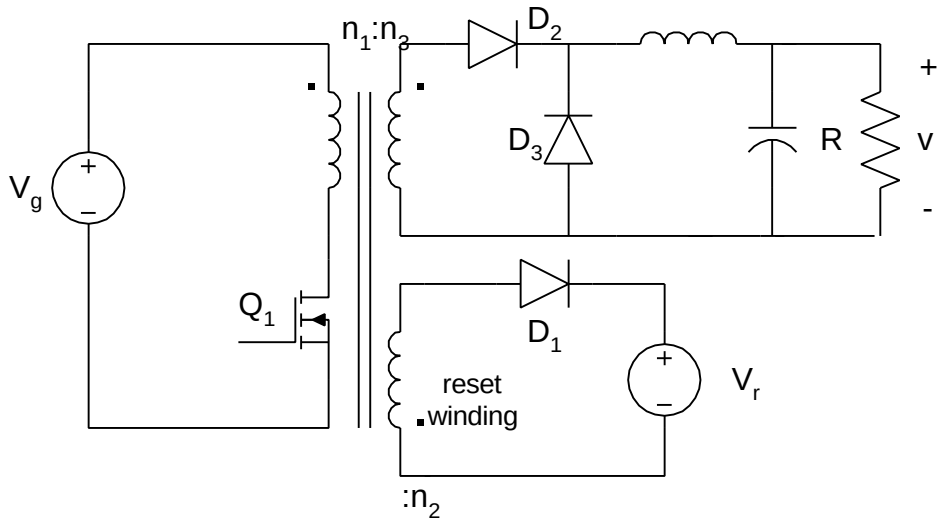
$\downarrow \quad \downarrow \quad \uparrow$

fixed

If $\frac{n_3}{n_1} \downarrow \Rightarrow$ Lower peak transistor current occurs

Erickson Problem 6.9: External V_r resets the core with less stress than reset with - V_g as shown below:

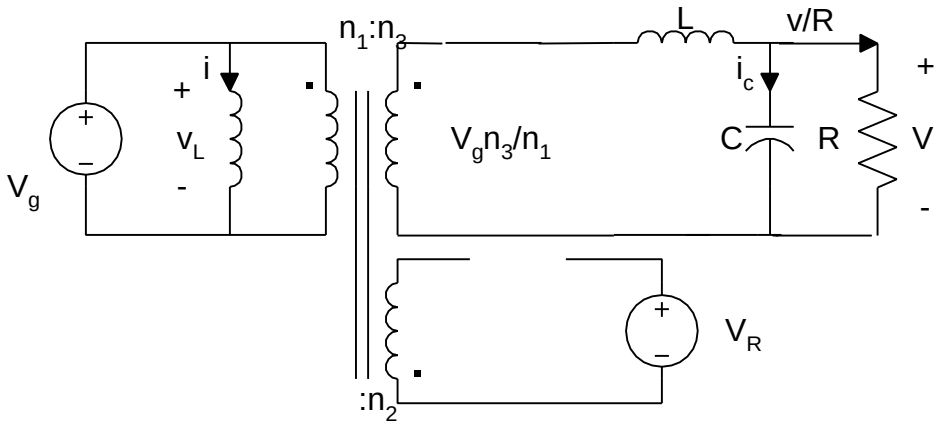
Note that the auxiliary secondary winding n_2 is not an output circuit, rather it is a reset voltage entry point.
The full schematic is shown on the following page.



In DCM operation there will be 3 periods as shown below:

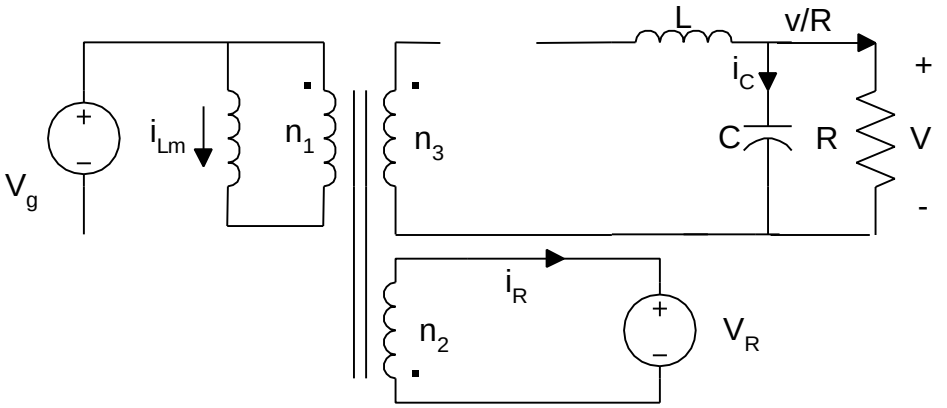
$\underline{D_1T_s}$	$\underline{D_2T_s}$	$\underline{D_3T_s}$
Q_1 on	Q_1 off	Q_1 off
Diode D_2 on	Diode D_2 off	Diode D_2 off
Diode D_3 off	Diode D_3 off	Diode D_3 off
Diode D_1 off	Diode D_1 on	Diode D_1 off

<u>Interval D_1T_s</u>: Diode D_2 on and diode D_3 off in the winding n_3.



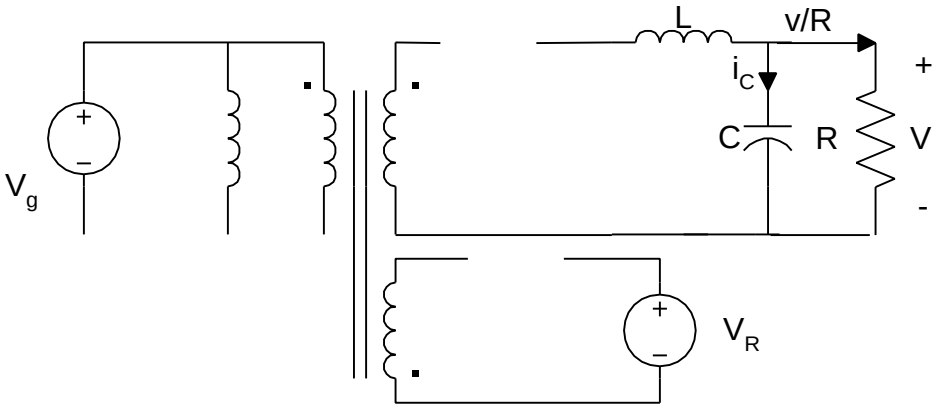
During interval D_1T_s an effective DC voltage of magnitude $D(n_3/n_1)V_g$ appears across winding n_3. As diode D_1 is off, V_R does not affect the core flux levels.

Interval D_2T_s: Diode D_1 in winding #3 is on activating the reset current on the magnetic core. The current i_{Lm} flows out of the n_1 winding dot implying current flows into both n_2 and n_3 windings. Hence, diode D_2 is off and diode D_1 is on.



Reset of core via integrating V_R for the interval D_2T_s.

Interval D_3T_s: All circuits are open and no volt-sec drive to the magnetic core flux occurs.



Below we calculate the applied V_R to the windings required for duration D_2T_s to cancel V_g applied for duration D_1T_s to winding #1.

Magnetizing Inductor: L_M

Volt-sec balance to L_M has only two components.

$$\langle V_{Lm}\rangle_{Ts} = 0 \quad V_g D_1 T_s + D_2\left[-V_r \frac{N_1}{N_2}\right] T_s = 0$$

$\langle V_{Lm}\rangle_{Ts} = 0$ sets the relation $D_2 = \frac{V_g}{V_r} D_1 \frac{n_2}{n_1}$

Setting D_1 and D_2 still must leave a non-zero interval D_3T_s.

$D_3 = (1-D_1-D_2) \geq 0$

$$\Rightarrow \frac{1-D_1}{V_g D_1} \frac{n_1}{n_2} \geq \frac{1}{V_R}$$

or $V_R \geq \frac{V_g D_1}{(1-D_1)} \frac{n_2}{n_1}$ Sets minimum value of V_R to be applied during interval D_2T_s for L_m core reset

Consider Switch Stress for Interval D_2T_s.

$V_{Tr}(\text{off}) = V_g + \frac{n_1}{n_2} V_R \rightarrow$ substitute for via

↑ +V_g from source

↑ appears on n_1 coil due to V_R on n_2 coil

$$V_{Tr}(\text{off}) = V_g\left[1 + \frac{D_1}{1-D_1}\right]$$

$$V_{Tr}(\text{off}) = V_g/(1-D_1)$$

Output Inductor of "Buck": L

$\langle D3\rangle = V_o \Rightarrow \langle V_L\rangle_{Ts} = 0$

↑ voltage equal either side

$D_1 \frac{n_3}{n_1} V_g = V_o \Rightarrow D_1 = \frac{n_1}{n_3} * \frac{V_0}{V_g}$ sets D_1T_s time so L has $\langle V_L\rangle_{Ts}=0$ in steady state.

Estimating the Significant Minimum Parameters of the Power Semiconductors

	Bipolar Power Switch		MOSFET Power Switch		Rectifier(s)	
Topology	V_{CEO}	I_C	V_{DSS}	I_D	V_R	I_F
Flyback	$1.7V_{in(max)}$	$\frac{2P_{out}}{V_{in(min)}}$	$1.5V_{in(max)}$	$\frac{2P_{out}}{V_{in(min)}}$	$10V_{out}$	I_{out}
One Transistor Forward	$2V_{in}$	$\frac{1.5P_{out}}{V_{in(min)}}$	$2V_{in}$	$\frac{1.5P_{out}}{V_{in(min)}}$	$3V_{out}$	I_{out}

The above summarizes a comparison between flyback and forward converter topologies as regards the switch stress and a crude estimate of the required SOA for the switches.

Finally, For HW#3 Due in 1 week:

1. Answer any Questions asked throughout lectures 12-15.
2. Chapter 6 Problems 7, 8, and 11(the forward converter).