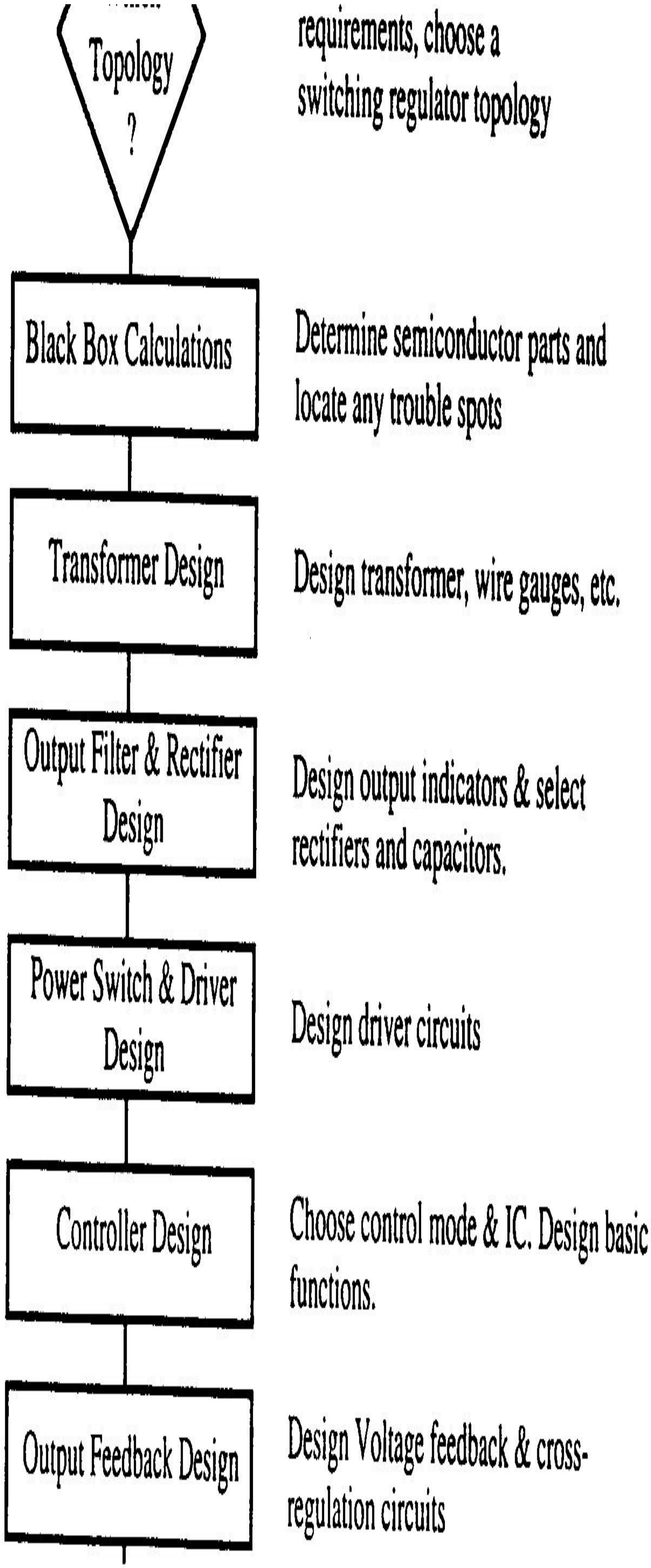
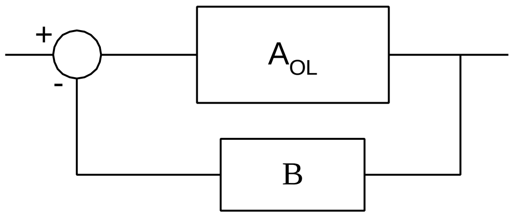
LECTURE 11
Introduction to Feedback

I. Feedback on PWM Converters
   A. Why Employ Feedback?
      1. Improved Stability
      2. Lower Z_{out} for Stiffer V(out) vs. I(out)
      3. Faster Frequency Response
      4. BUT Danger of Oscillation is introduced by feedback
   B. How to implement feedback
      1. Voltage Feedback
      2. Current Feedback
   C. Various Semiconductor Control Chips and Switch Device Components

III. Transient Effects
   A. Start Up
   B. Other


Topology ?
requirements, choose a switching regulator topology
Black Box Calculations
Determine semiconductor parts and locate any trouble spots
Transformer Design
Design transformer, wire gauges, etc.
Output Filter & Rectifier Design
Design output indicators & select rectifiers and capacitors.
Power Switch & Driver Design
Design driver circuits
Controller Design
Choose control mode & IC. Design basic functions.
Output Feedback Design
Design Voltage feedback & cross-regulation circuits

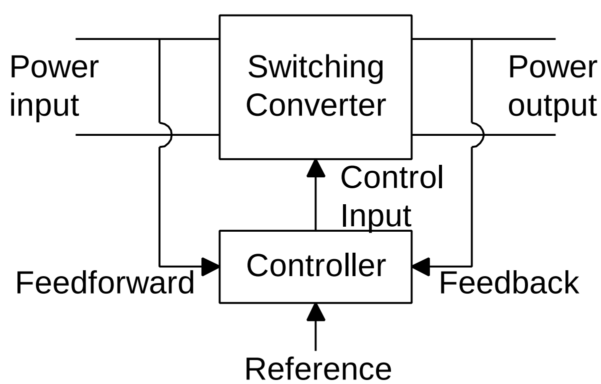


$$A_{CL} = \frac{A_{OL}}{1 + A_{OL} b}$$

$$\approx 1/\beta \text{ for large } A_{OL}$$

This lecture is to give a view of the total system surrounding the PWM converter circuit. It is an awesome amount of auxiliary electronics around the simple PWM circuit but most of it is built into the commercial control and driver chips that we will employ. As a consequence we will have a broad but shallow coverage in this lecture with details of each portion of feedback, especially compensation of feedback, taken up again in second semester.

A. Why Employ Feedback?



1. Stability

   $A_{OL} \to \infty$, $A_{CL} \sim 1/\beta$

   so small variations in A_{OL} due to aging, thermal effects, or component variation have little effect.

2. Reduced Z_{out} to allow for large I_{out} at V_{out}.

$$Z_{out(CL)} = \frac{Z_{o(OL)}}{1 + A b}$$

Without feedback V_o/V_{in} determines D from M(D). With feedback D may vary dynamically to keep V_o fixed while V_{in} varies or the circuit changes.

3. Faster Frequency Response

Most converter transfer functions have at least two poles. Transient response for A_{OL} with two poles is much faster when using feedback due to gain-bandwidth product being constant. Reduced gain means wider bandwidth and faster transient response. Hence, for DC-DC converters with feedback we will need to find $A_{OL}(\omega)$ in order to design proper transient response and evaluate:

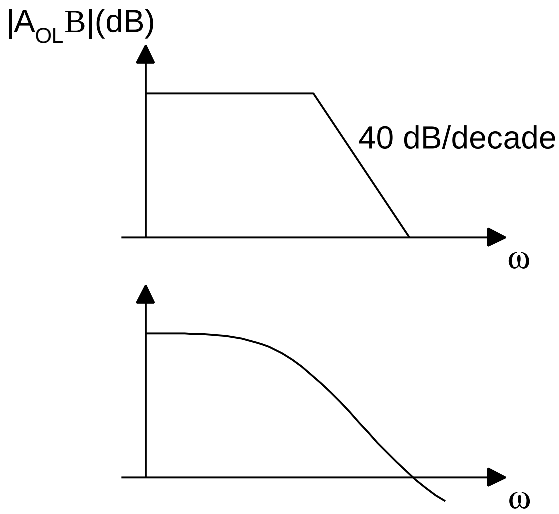
$A_{CL}(w) = \dfrac{A_{OL}(w)}{1 + A b}$ Loop gain vs. ω, see Ch. 7 of Erickson

4. Danger of feedback is oscillation--if $A b \rightarrow -1$ then

$A_{CL} \rightarrow \infty$

For two poles, phase shift may reach 180° at $|A b| = 1$.

This condition is well known to any audio system that suddenly starts to SCREECH.



$|A\,b| \rightarrow 1$ or 0 dB

and $\phi = 180°$

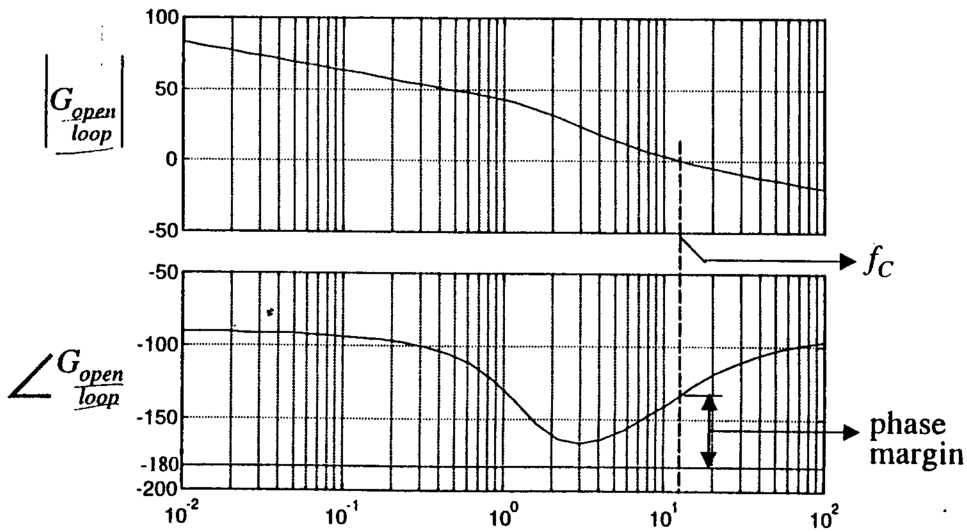
Recall from op amp design and control theory, one designs the feedback loop carefully such that undesired loop oscillation does <u>not</u> occur at any frequency. In some server computer power supplies or system tape drives, safe reliable operation is as important as speed - ultrasafe case.

Ultra-safe case: cross unity gain of A_{OL} only at a slope of 20 dB/octave due to a single pole only. Only one pole in A_{OL} converters are made by design. Discontinuous mode and current programmed mode converters are examples of one pole transfer functions we can design for. See Chapter 10 and 11 of Erickson respectively.

We will see second semester that for an optimum feedback design we need to hit a specific value of phase margin for the open loop gain. This value gives the fastest response without any danger of oscillation.

Phase margin

- Phase margin should be in the range of 45^0 to 60^0 to prevent large overshoots



B. How to implement feedback

There are several feedback schemes:

- Voltage Feedback
- Current Feedback
- Frequency Feedback

Below we will focus on voltage and current feedback only. We will leave frequency feedback , which is employed in resonant switching converters, for second semester.

1. Voltage Feedback (Chapter 8 and 9 of Erickson)

Feedback itself, in PWM dc-dc converters, can operate in two circuit modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The former has well orchestrated control of switches while the later has intervals controlled by the circuit and not the switch drivers.

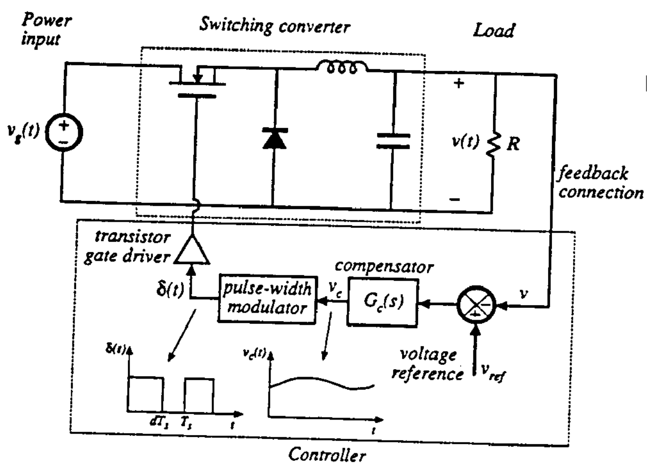


Fig. 7.1. A simple dc-dc regulator system, including a buck converter power stage and a feedback network.

$$A_{OL} = \frac{\Delta v_{out}}{\Delta D}$$

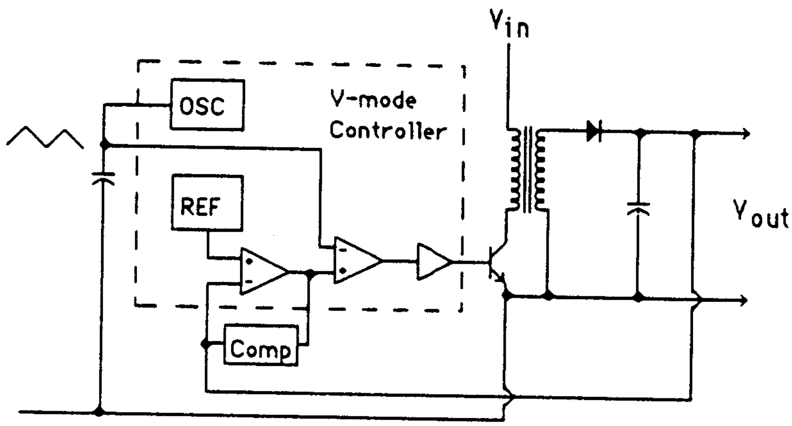
Loop gain with respect to duty cycle

We will find later that for the same feedback loop on the same converter operating either in continuous conduction mode (CCM) or operating in discontinuous conduction mode (DCM) will have two very different closed loop gains and dynamic conditions:

a. CCM has two poles and we need to design carefully for phase margin of 76° to avoid oscillation.

b. DCM has only one pole in transfer function. It is unconditionally stable and will never oscillate.

In summary for voltage feedback we have:



Voltage-mode control.

• Has a characteristic comparator fed by the output voltage and the ramp voltage across a timing capacitor

• V control is slow and cannot protect against fast current transients in the power switch

- the transient response is too SLOW to protect switches

- Many switch failures occur due to core saturation of inductors when using V control

2. Current Programmed Mode Feedback CPM PWM converter—Chapter 10 of Erickson

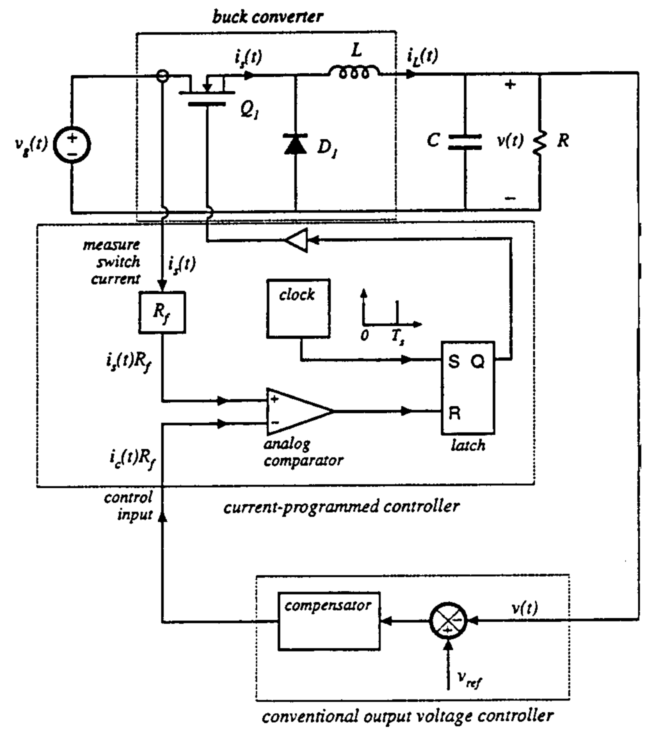


Fig. 11.1. Current-programmed control of a buck converter. The peak transistor current replaces the duty cycle as the control input.

To protect costly solid state switches we often monitor i_s anyway to avoid I_{pk}. So why not utilize this monitor for current feedback? Combine i_s monitor and conventional v_{out} controller to set D and D'. Both changes in Vo and is will cause compensating changes in D to fix system parameters we desire fixed.

Consider for now only current feedback signals:

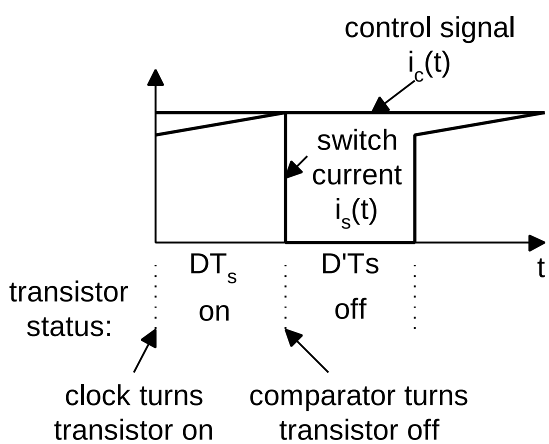
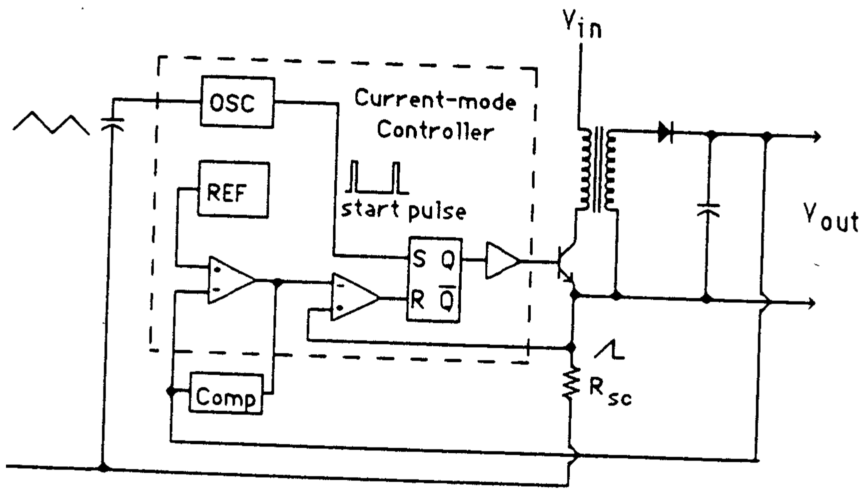


Fig. 11.2 Switch current $i_s(t)$ & control current $i_c(t)$ waveforms for the current programmed system of Fig. 11.1.

I_s is compared to $I_{control}$ to set D and D' the transition from D to D' is set when $I_s > I_c$

In summary for current feedback we have:



A current-mode controller.

• Characterized by a comparator fed by the difference between the error voltage and the instantaneous power switch current. Modern switch devices have on board current sensors to protect the switch from over current

•Now peak currents are sensed immediately and switches protected in a more direct and faster responding manner. This reduces costly field replacement of switches.

•

C. Various Semiconductor Control and Switch Device Components

1. Overview

The three major categories of PWM converter parts, for the PWM parts bill of lading, are given below.

a. <u>Cheap IC controller chips exist with many on-board capabilities:</u>

•timing components

•current sensing

•PWM with variable D

•switch drivers

(b) <u>Power devices for switching</u>: See Chapter 5 of text

•MOSFET's •IGBT's •diodes
•GTO (Gate turn-off Thyristor)
•MCT (MOS-Controlled Thyristor)

(c) <u>Reactive elements</u>:
•Capacitors •Inductors on cores

In practice **parasitic R, L, and C compo**nents often **make up half the circuit model components though they do not appear on the bill of lading**.

2. Commercial Controller Chips

The controller chip is available from integrated circuit manufacturers at very low cost, yet, featuring a host of capabilities. Two types of control chips are listed on the next page. Features on board the chips include:

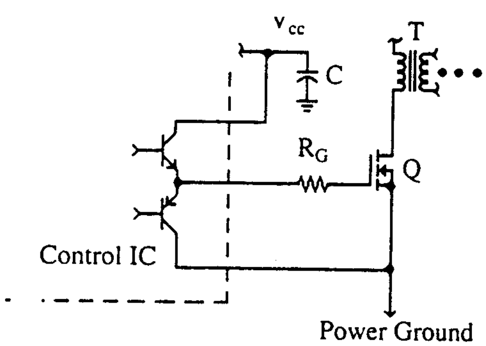
- Power MOSFET Drive Circuits for the power switch
- Multiple Output Sensing with Weighting of Each Output
- Over-current Shutdown circuits
- Over-voltage Protection Circuits
- Under-voltage Protection Circuits

a. Commercial Control Chips

Examples of (a) Voltage-mode and (b) Current-mode Switching Power Supply Control Integrated Circuits

			Function Features					Output Driver Type	
Part No.	Tech.	1–2 Outputs	OC Amp.	Soft start	Shut off	Synchr.	LVI	UC Trans.	Totem-pole
(a) Voltage-mode Switching Power Supply									
MC34060	B	1	×				×	×	
NE5560	B	1	×	×	×	×		×	
NE5561/8	B	1	×					×	
NE5562	B	1	×	×	×	×		×	
SG3524	B	2	×		×			×	
TL494	B	2	×		×			×	
SG3523 (MC34023)	B	1	×	×	×	×	×		×
SG3525 (MC34025)	B	2	×	×	×	×	×		×
(b) Current-mode Switching Power Supply									
MC34065	B	2 ea. 1				×	×		×
MC34129	C	1		×	×	×	×		×
SI 91XX	HVC	1			×		×		×
uA78S40	B	1							×
UC384X	B	1					×		×
SG3523 (MC34023)	B	1		×	×	×	×		×
SG3525 (MC34025)	B	2		×	×	×	×		×

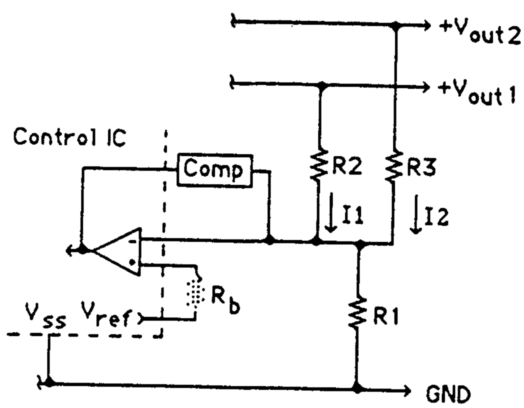
b. MOSFET Driver



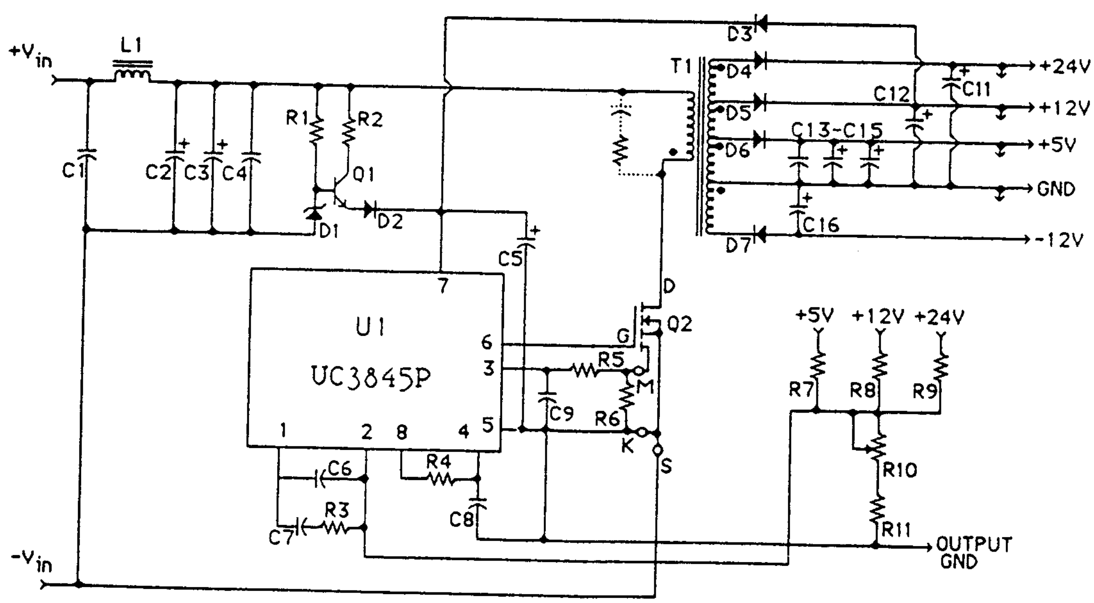
R_G: between 10 and 50 ohms.

The gate of the power MOSFET must be driven by 10 V at V_{GS} to reach full I_D. The gate capacitance is usually 2nF, so large peak currents are drawn.

c. Multiple Sensing



The multiple-sensing method.



Schematic for design example 3.15.2. A 28 W current-mode, flyback dc-to-dc converter.

When we are using one PWM circuit to create multiple outputs we need to control all of them, but it is cheaper to sense the outputs in a weighted fashion. The weight assigned to each output depends on the system level decision on which output needs tighter output regulation.

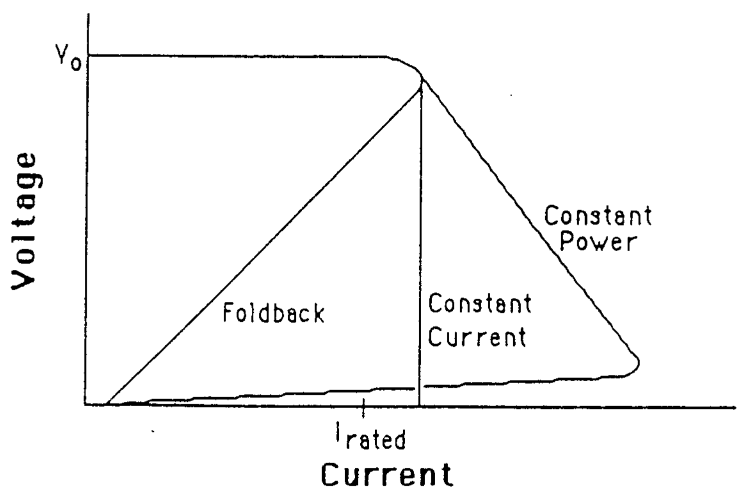
R_2 and V_2 provide a current to R_1 that is properly weighted as do R_3 and V_3 with their contribution. In total the current through R_1 will add so that the voltage across R_1 is equal to V_{ref} in equilibrium.

A more complex system with four outputs is illustrated with only three weights as the + and – 12 volts are similar.

d. Over current Protection

We want to protect against failures in the load, like an inadvertent short. There are three types of overcurrent protection.

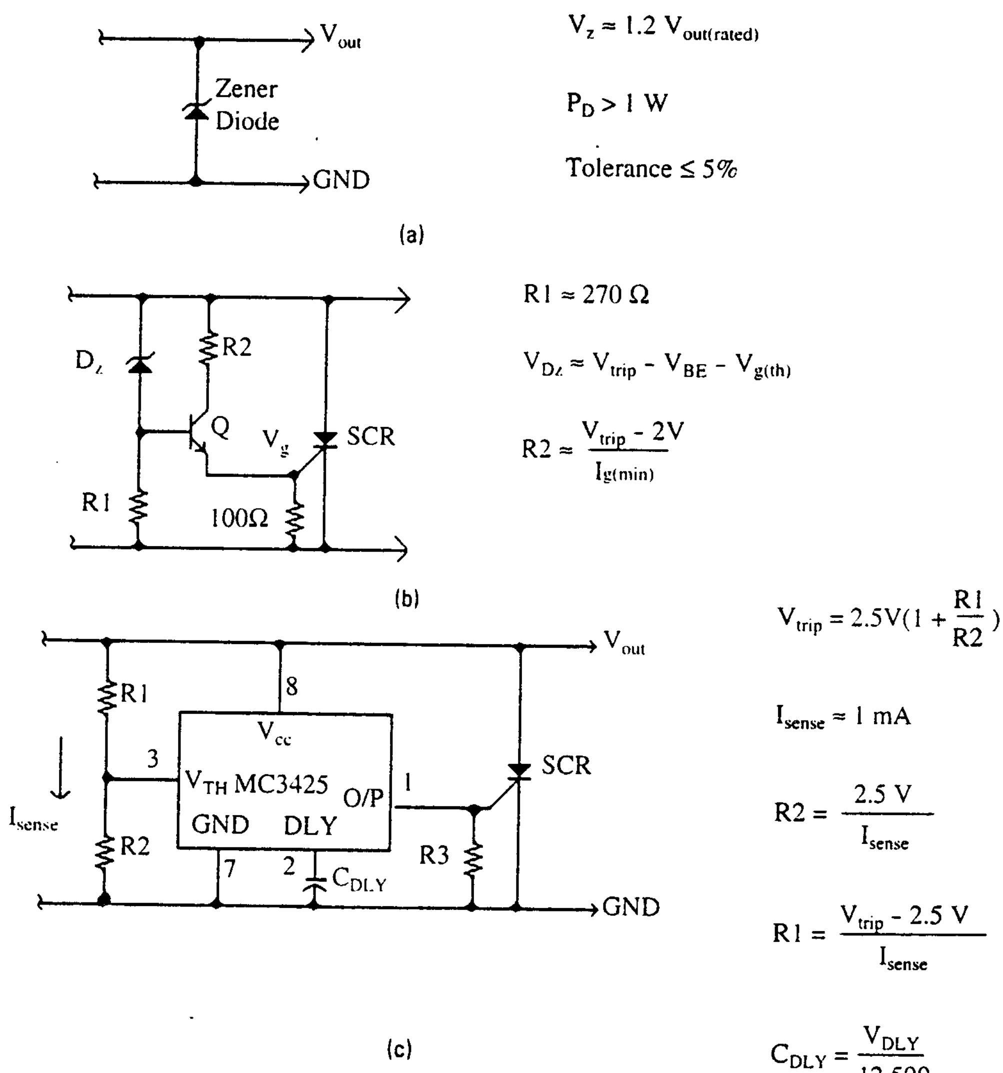
- Constant Power limiting
- Constant Current Limiting
- Foldback Limiting allows V(out) to go to zero



Types of overcurrent protection.

e. Overvoltage Protection

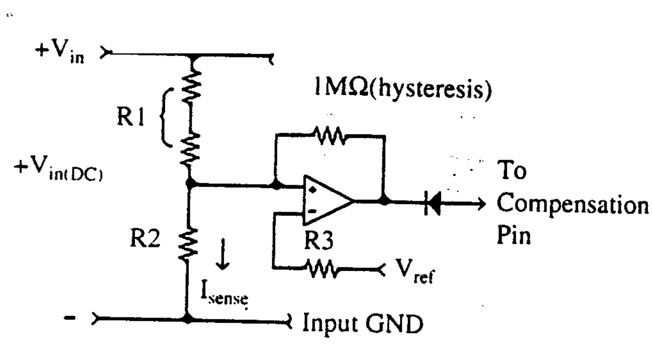
We assume that the feedback loop has opened or the load current on one output has gone to zero causing the voltage to rise above the maximum specification. In this case we need separate hard wired output sensors and a separate comparator to activate override of the error amplifier as shown below via three approaches



Overvoltage protection schemes: (a) Zener diode clamp; (b) overvoltage crowbar; (c) integrated overvoltage crowbar.

f. Undervoltage Shutdown

Here we assume that brownout conditions occur at the input which could inadvertently cause the duty cycle to latch up to unity and lose control. A simple comparator sensing the line input will avoid this case as shown below.



$$R2 = \frac{V_{ref}}{I_{sense}}$$

$$R1 = \frac{V_{in(min)} - V_{ref}}{I_{sense}}$$

$$R3 \cong \frac{(R1)(R2)}{R1 + R2}$$

Op Amp: MC33172P

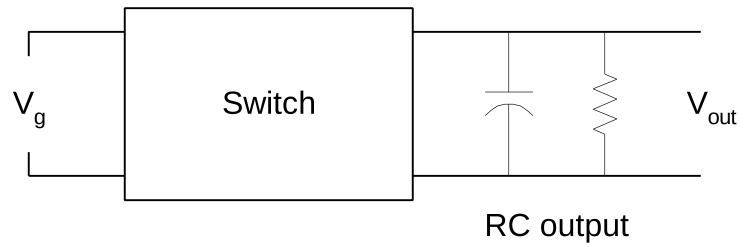
A typical input undervoltage shut-down circuit.

If a logic or microprocessor chip as well as a hard disc drive is driven by a power supply we may also need a POWER ABOUT TO FAIL signal be generated to allow a sufficient time to institute a orderly shutdown. As much warning time as possible is desired. This is beyond today's discussion.

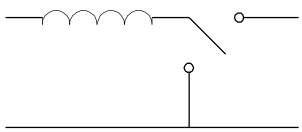
III. Transient Effects

There are two separate effects we will consider. One is the isolated turn-on of the converter which has a long transient time to reach steady-state output. During this time the control chip and driver circuits may not be powered up in time. If this occurs, we may not be able to drive the switch properly and we can destroy the expensive power switch. The second is the fast switching at each T_s which causes losses as we try tomaintain the output.

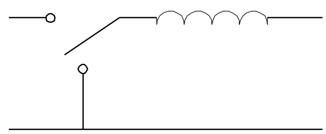
A. Slow turn on vs. steady state



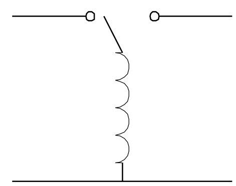
Boost



Buck



Buck-Boost



Consider buck case:

Apply V_g switch at f_{sw}.

Turn-on requires: @ $t = 0$, $i_L = 0$; @ $t = \infty$, $i_L = I_{out}$

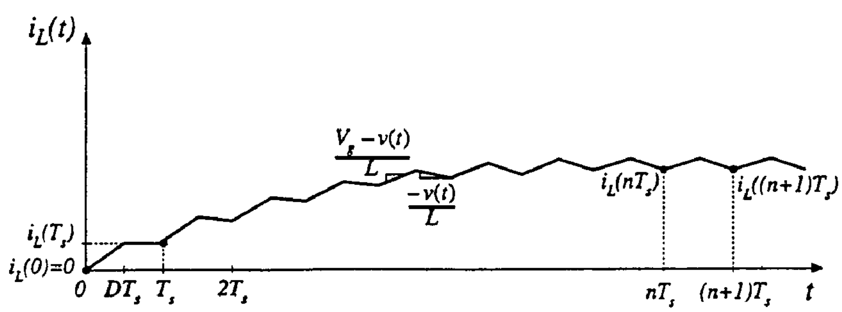


Fig. 2.11. Inductor current waveform during converter turn-on transient.

(1) Turn on:

Up-ramp slope @ $t = 0$: $s_u = \dfrac{V_g - 0}{L}$

Up-ramp slope @ $t = \infty$: $s_u = \dfrac{V_g - V_{out}}{L}$

Whereas the downslope ramp is always: $s_d = \dfrac{-V_{out}}{L}$

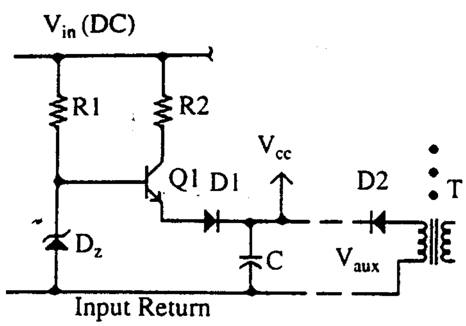
In both cases V_{out} varies from 0 to V_{out};

V_{out}(buck s.s.) = DV_g regardless of f_{sw}

Steady-state does have ac and dc for dc-dc converters

$v_{out} = V_{out}(dc) + v_{out}(ac) \leftarrow$ ac part is 0.1 to 10% at f_{sw}

We need a separate power supply IC when the input voltage is above the range for the control chip itself so that we can power up the control chip and the drivers BEFORE the power switch is toggled.Otherwise we could cause switch failure See one implementation using a linear regulator chip below.



R1: $R1 \le \dfrac{V_{in(min)} - V_{DZ}}{I_{DZ(min)}}$

R2: $R2 \approx \dfrac{V_{in(min)} - V_{DZ}}{I_{start}}$

D1: 1N4148 D2: MUR1X0

Dz: 500 mW, > $V_{cc(min)}$ of IC

Q1: $V_{CEO} > V_{in(max)}$, $I_C \approx 300$ mA

The high-voltage linear regulator bootstrap start-up circuit (used only at start-up and foldback periods).

(2) Steady state conditions for DC-AC converters or DC converters with feedback

(a) DC-AC converter case

(1) General case

By modulating the duty cycle at a frequency w_m we can change V_{out}, but only if $\omega_m < \omega_s$. That is from DC V_{in} we can get an AC output centered around a dc value.

$V_o = DV_g$, let $D = \cos \omega_m t \Rightarrow V_o = V_g \cos \omega_m t$.

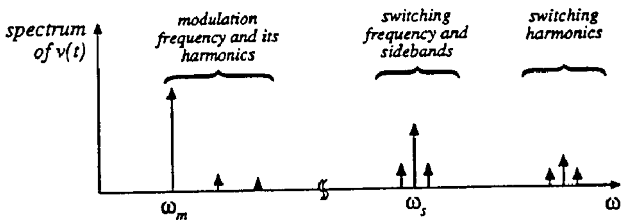


Fig. 7.3. Spectrum of the output voltage waveform $v(t)$ of Fig. 7.2.

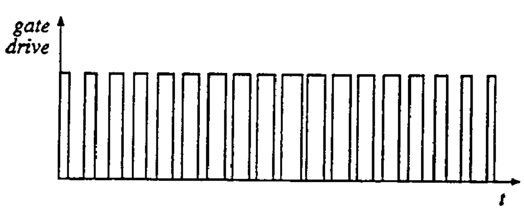
Fourier spectrum for

$D = \cos \omega_m t$

if $\omega_m << \omega_s$

RC output filter is chosen so it passes signals $\omega < n\omega_m$ and stops signals $\omega > n\omega_m$

For fixed D the $V_o = V_{in} M(D)$ is at a dc value. Next we let D vary with time as shown below.



For $D \sim \cos \omega t$ we can get ac output around an effective DC value by:

This sinusoidal D(t) will cause a sinusoidal $V_o(t)$.

vout ~ -cos ωt

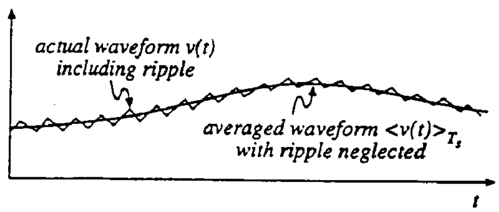


Fig. 7.2. Ac variation of the converter signals: transistor gate drive signal, in which the duty cycle varies slowly, and the resulting converter output voltage waveform. Both the actual waveform $v(t)$ (including high frequency switching ripple) and its averaged, or low-frequency component, $< v(t) >_{T_s}$ are illustrated.

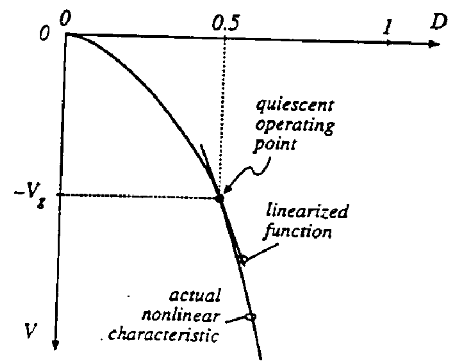


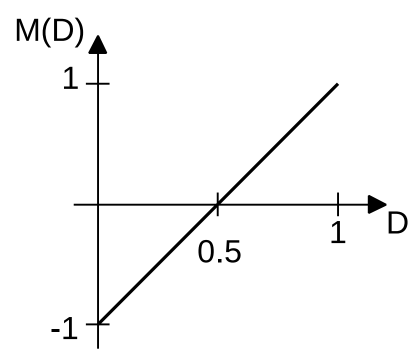
Fig. 7.5. Linearization of the static control-to-output characteristic of the buck-boost converter about the quiescent operating point $D = 0.5$.

How could we get a sinusoid centered about zero volts?

(2) <u>Bridge-inverter case</u>: voltage fed, not current fed

In a fixed D operation we find $V_{out} = M(D)V_{in}$.

$$\frac{V_{out}}{V_g} = 2D - 1$$



Noting that the output is symmetric about 0.5. We set D=0.5 and V_o=0. Add a time varying component $D = 0.5 - \Delta d\cos \omega t$ to achieve sinusoidal output around zero volts.

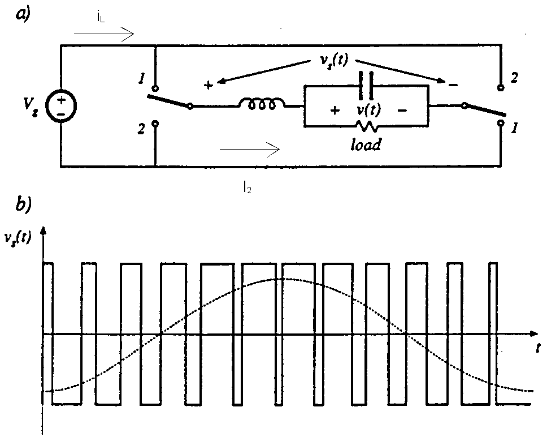
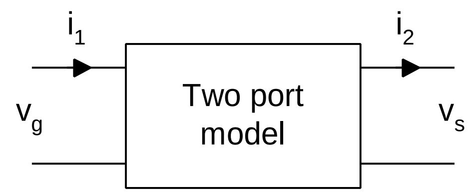


Fig. 1.13. A bridge-type dc-1øac inverter: (a) ideal inverter circuit, (b) typical pulse-width-modulated switch voltage waveform $v_s(t)$, and its low-frequency component.

Later we will model the two synchronized SPDT switches by a switch averaged two port model.



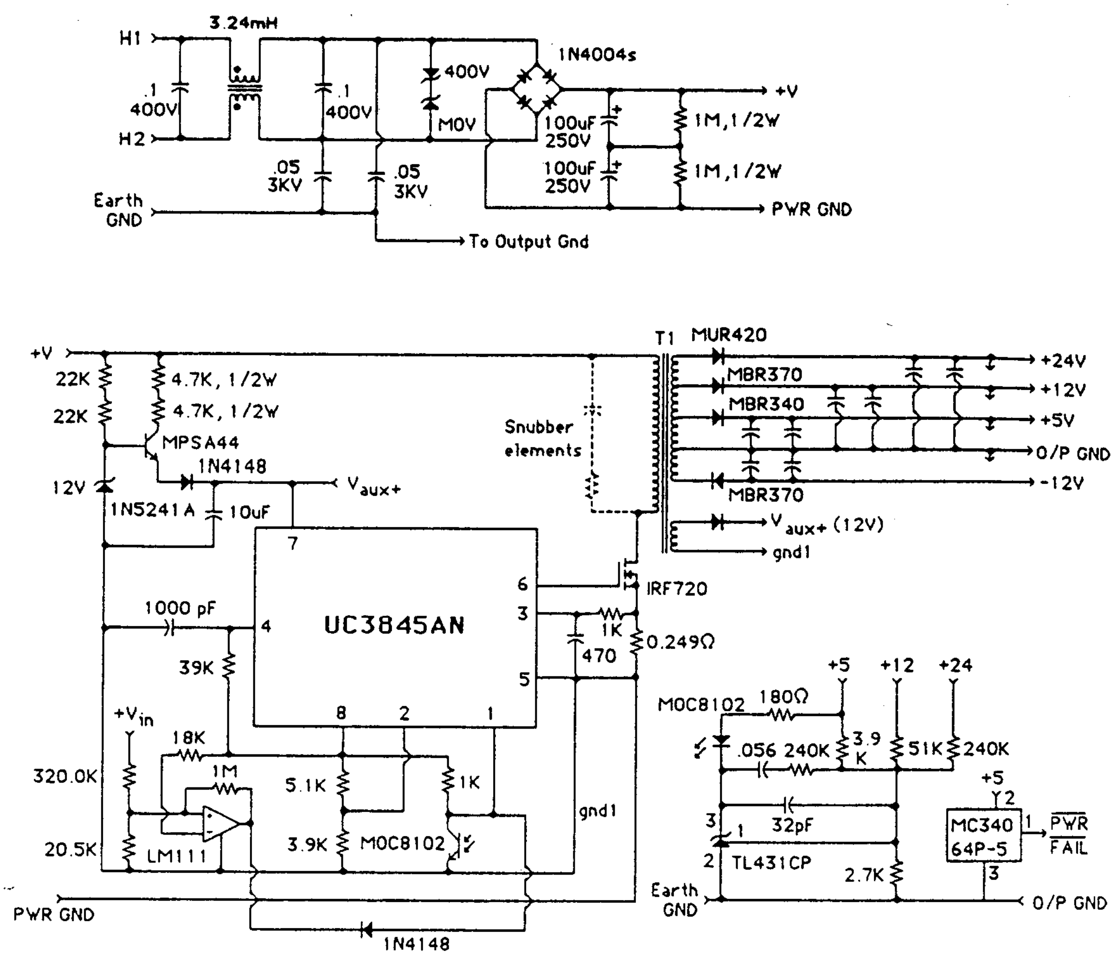
(b) DC-DC converter with feedback

To better stabilize DC-DC converters, we use feedback that looks at a fixed V_{ref} compared to the changing V_{out}, which sets the proper D for desired V_o dynamically. If V_o varies for whatever reason then the on duty cycle D varies to stabilize V_o back to the desired value.

D will become a function of time rather than a constant and the transfer function of the inverter becomes the output voltage divided by the duty cycle $\frac{V_o}{\hat{d}}$ will be valid.

On the following page is a full schematic for a flyback converter. **FOR PRACTICE** look through the schematic to find the peripheral circuitry in a PWM:

- Input filter and rectifier circuit block
- Various Outputs
- Control and PWM Circuits



65 W, off-line flyback converter.