LECTURE 10

Summary Loss Free
Pulse Width Modulated Converters and
Introduction to Losses

I. Summary DC-DC PWM Converter
   A. Single Inductor Converters With Only Source Resistance losses

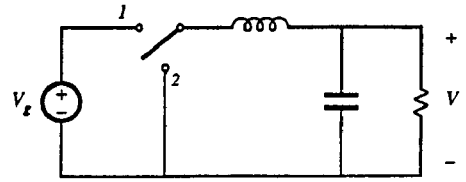
II. Two inductor Converters
   A. General
   B. CUK Converter DC Transfer Function Analysis: M(D)

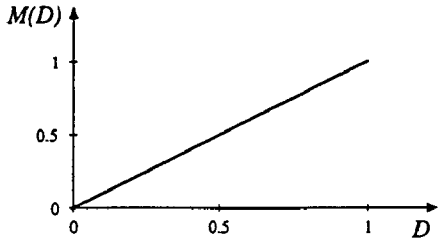
III. Static and Dynamic Switching Loss Effects in PWM Converters
   A. General Switch Issues
   B. Static Converter Losses
   C. Power Loss Switching at f_{sw} Due to Finite SwitchTimes
      1. General Considerations
      2. Easy Switch Analysis : Transistor Off and Diode on
      3. Complex Switch Analysis: Transistor on and Diode Off
         a. With Diode Stored Charge
         b. Inductor Current Switching

I. Summary - PWM single inductor converters

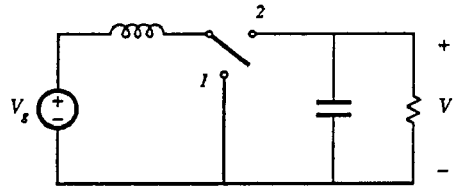
A. Eight circuit topologies and DC transfer functions M(D) where $M(D) \equiv V_o/V_g = f(D)$. Its crucial to emphasize that we assume LOSS LESS CIRCUITS BELOW.

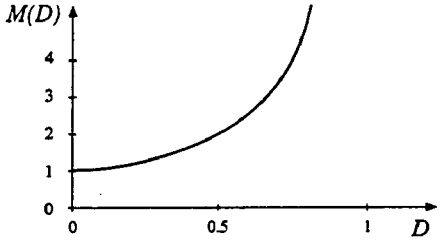
1. Buck $M(D) = D$



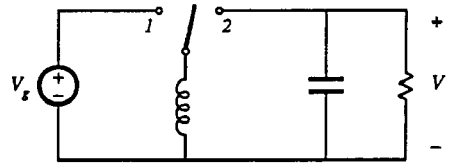


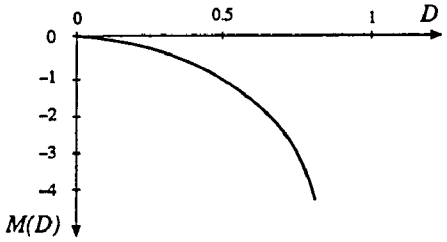
2. Boost $M(D) = \frac{1}{1-D}$



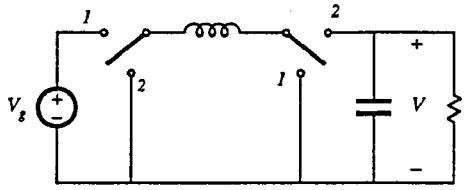


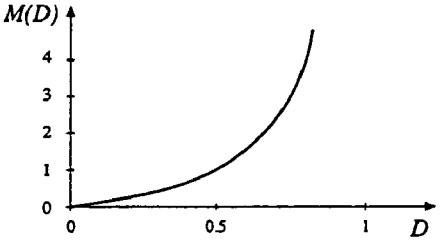
3. Buck-boost $M(D) = -\frac{D}{1-D}$



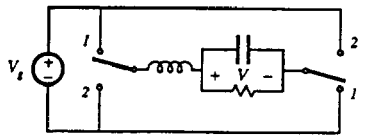


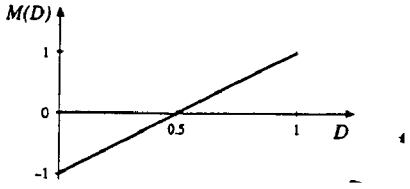
4. Noninverting buck-boost $M(D) = \frac{D}{1-D}$

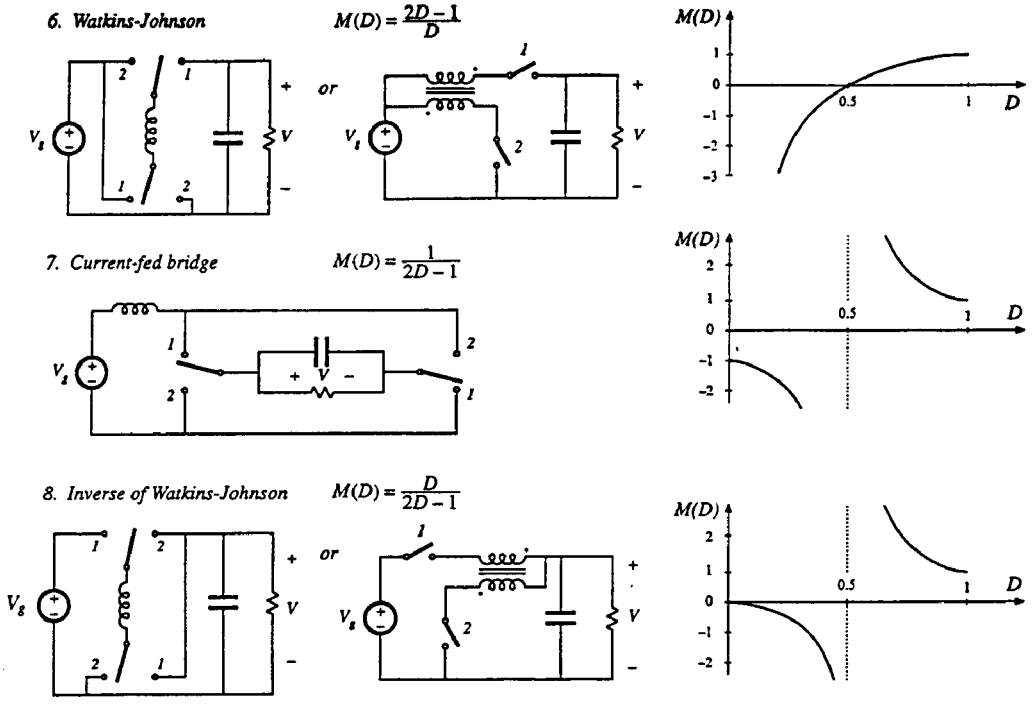




5. Bridge $M(D) = 2D - 1$







All $V_o/V_g = M(D)$ above were obtained using D+D'=1 or the continuous conduction mode approximation.

a. Charge balance on C_{out}: $\frac{I_{on}}{C}D + \frac{I_{off}}{C}D' = 0$

b. Volt-sec balance on L: $\frac{V_L(on)}{L}D + \frac{V_L(off)}{L}D' = 0$

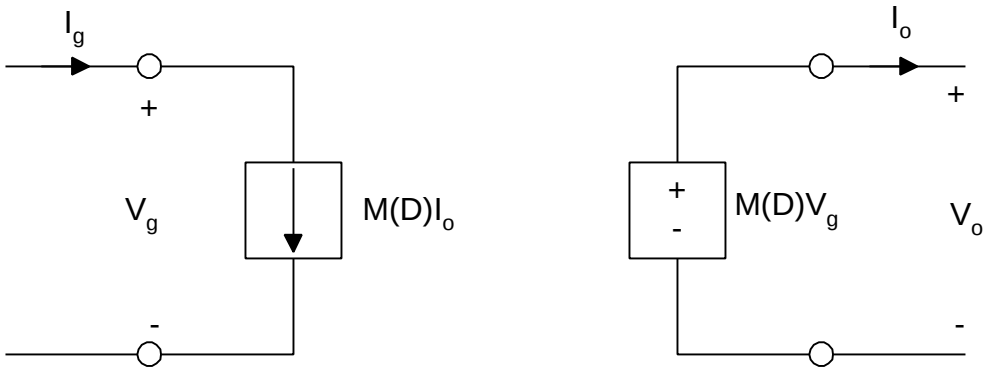
<u>Power Conservation</u>

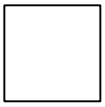
Given that for steady state conditions $V_o = M(D)V_g$, one must realize that simple power conservation arguments then demand:

$I_g = M(D)I_o$

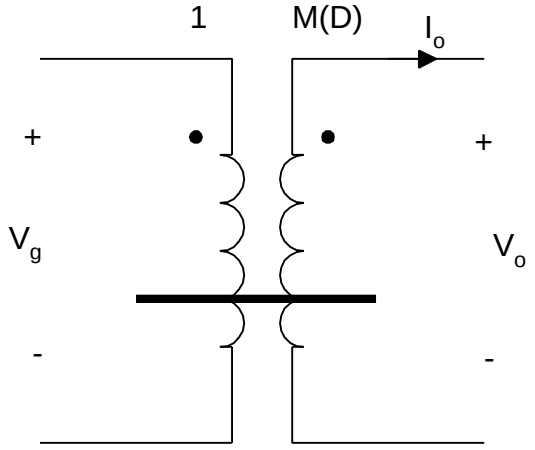
Clearly, $p_{in} = p_{out}$

In a lossless converter, since $P_{in} = P_{out}$:



Where the symbol  is a dependent source, either V or I

By analogy with the familiar ac transformer we can represent this as an effective DC transformer as shown below with a turns ratio of M(D). The model development flow is then: (a) actual converter, (b) DC transformer, and (c) simplified DC circuits can then be made using transformer rules.

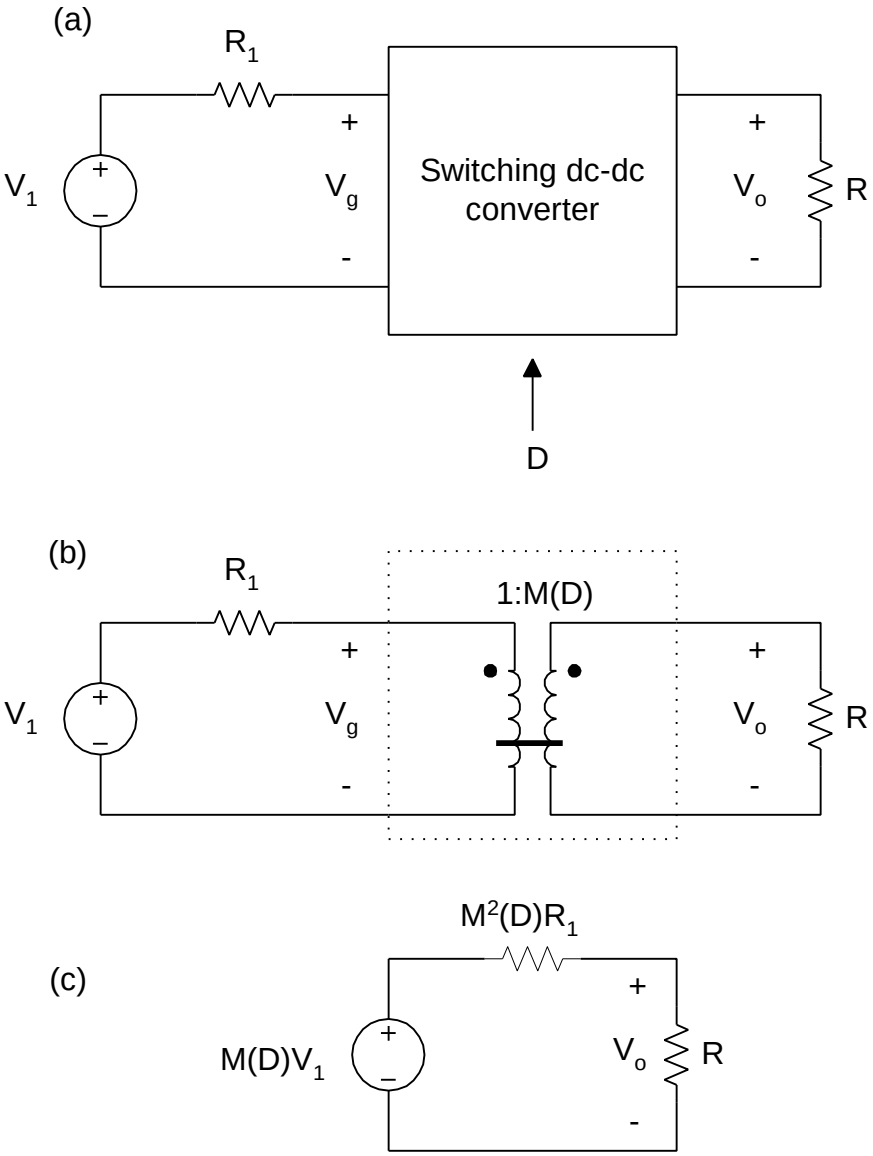


<u>Lossless DC Transformer</u>

Effective turns ratio

1:M(D)

Next we will simply add a source impedance to the DC source to the converter and see how this effects V(out) by employing transformer rules.



Example of use of the dc transformer model: (a) original circuit; (b) substitution of switching converter dc transformer model; (c) simplification by referring all elements to secondary side.

Including source impedance R_1 we get:

$$V_{out} = M(D)V_1\left(\frac{R}{R + M_2(D)R_1}\right) \leftarrow \text{Voltage Divider}$$

$\Rightarrow$ For big values of M(D) be careful of innocent R_1 as it may surprisingly effect the DC output. This occurs, for example, in a converter for a flash camera that goes from 1.5 V to 1500 V. That is M=1000 magnifies even small R_{source}

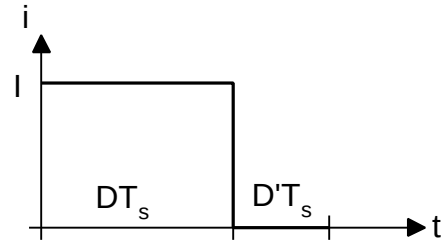
M(D) lossless itself will change only when we include lossy L and C inside the converter itself. See section III below.

C. RMS Values for Converter Waveforms

1. Square and Ramp Waveforms

i waveforms

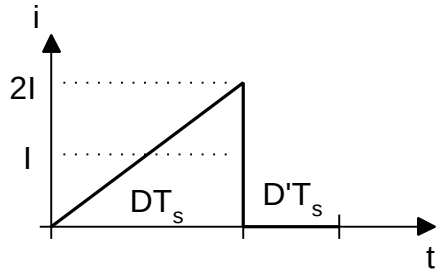
Typical Transistor Waveform



$$I_{rms} = \sqrt{\frac{1}{Ts}\int_0^{T_s} I_s^2 dt}$$

$$I_{rms} = I\sqrt{D}$$

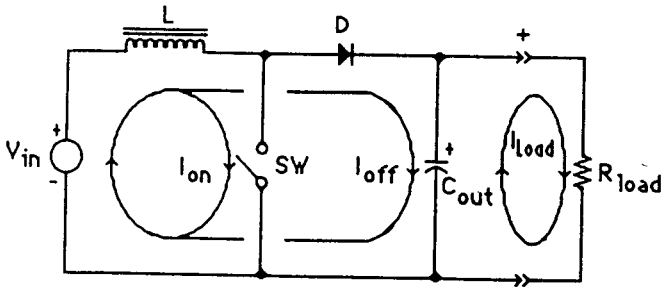
Typical Diode Waveform



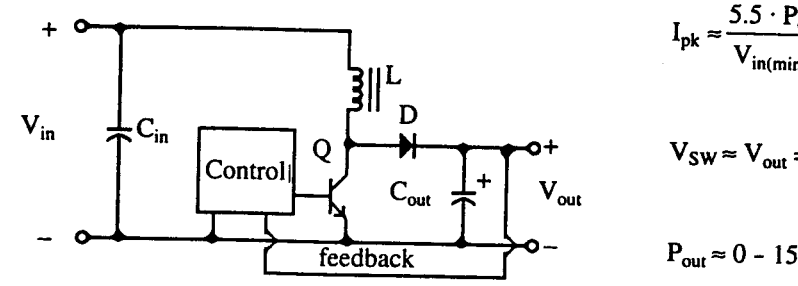
$$I_{rms} = 1.15I\sqrt{D}$$

The two above are among the simplest cases. Recall that in the big three circuits we have even more complex AC wave forms as those shown below from Lecture 4. We repeat only one BOOST circuit waveforms from lecture 4 below but the point is made that each waveform has a unique RMS value that I_{rms} is a function of the duty cycle D.

On the next pages we also review the converter topologies as well as the current flows in each switch position so that the full waveform is developed. It is left to the student to match waveforms to RMS calculations using Appendix 1 of Erickson.



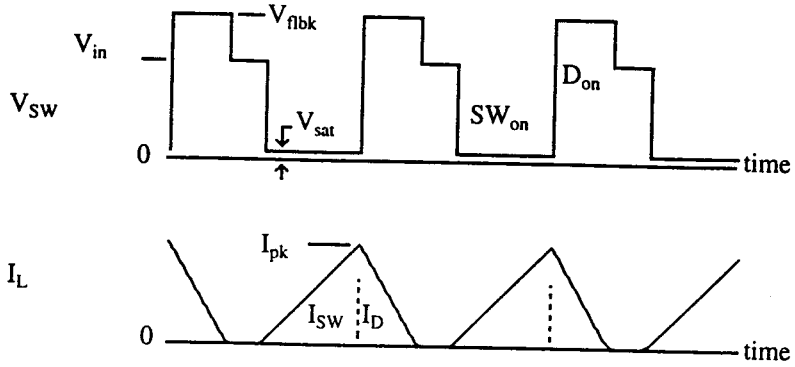
A basic flyback-mode converter (boost converter shown).



$$I_{pk} \approx \frac{5.5 \cdot P_{out}}{V_{in(min)}}$$

$$V_{SW} \approx V_{out} = V_{flbk}$$

$$P_{out} \approx 0 - 150\ W$$



The boost regulator topology.

II. Summary of 2 inductor, 2 capacitor PWM converters

A. Overview

Clearly converter topologies exist with two L's and two C's. We will restrict ourselves to those two L/two C topologies with only two active switches. The extra L and C allow for better filtering of $V(f_{sw})$ as well as better protection from KVL and KIL violations. Analysis of the circuits for the DC

transfer function follows the same principles. All provide V_{out} from 0 to nV_g.

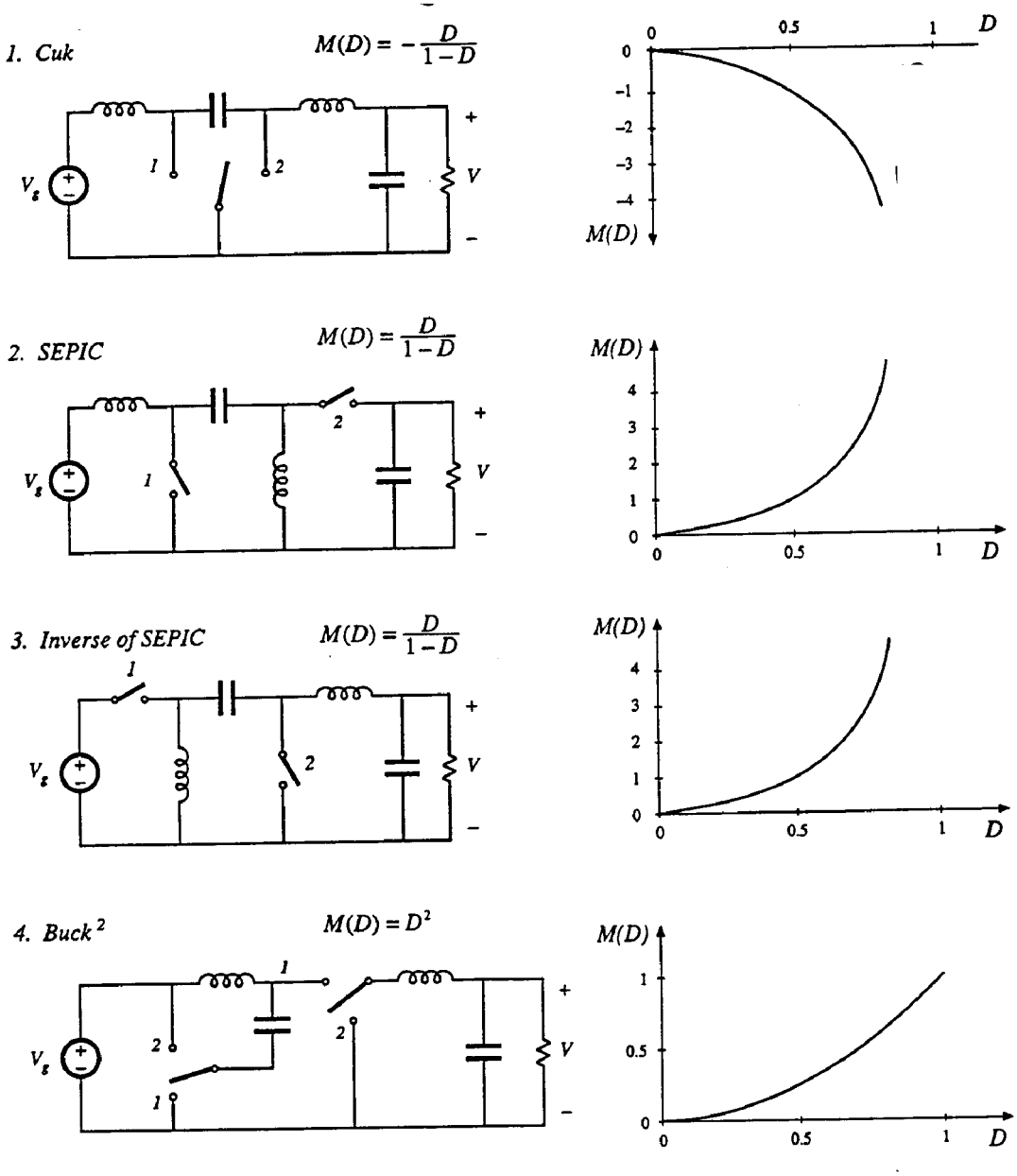


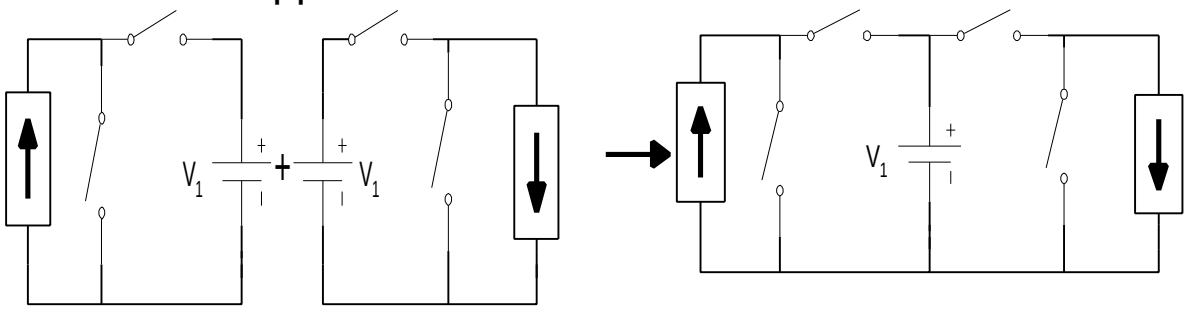
Fig. 6.16. Several members of the basic class of single-input single-output converters containing two inductors.

Note: Of the above, only Cuk has negative V_{out} w.r.t. V_g and V_{out} varies from 0 to $M(D)V_g$ for all of the double L/C converters.

B. Lossless Cuk converter M(D) analysis

This is a series cascade of a boost converter driving a buck circuit as shown below. Polarity reversal occurs between input and output. Cuk is the inventor of this 1970's circuit.

Note: 1. V_1 is the voltage across C_1.
2. Upper series switches are redundant.

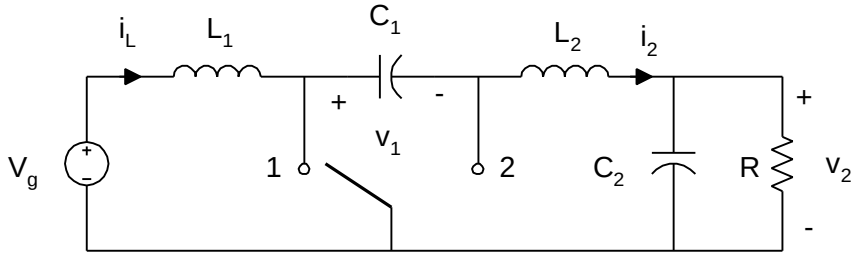


Boost converter supplying a buck converter

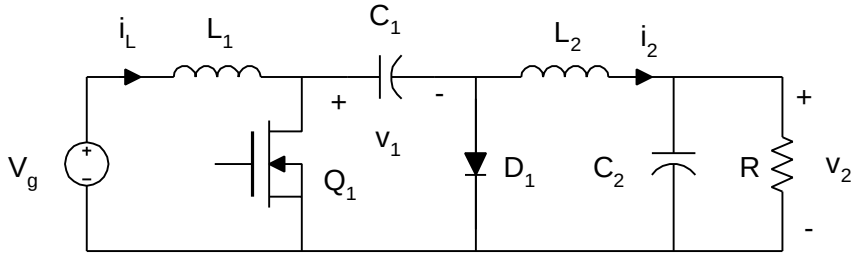
The top series pair of switches is redundant and are employed as shown below:

Polarities below are for analysis only

- Use Volt-sec balance on L_1 and L_2
- Use charge balance on C_1 and C_2.



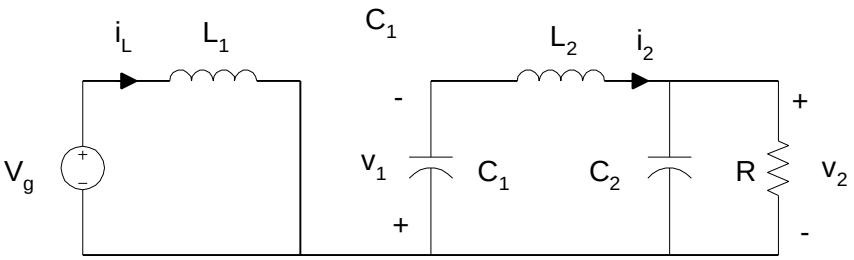
Ideal Switch Circuit



Transistor/ Diode Switch Implemen-tation

Actual Cuk: $V_o = -V_g \Rightarrow$ we will find $V_o = -f(D)V_g$

Case 1: D when Transistor on and diode off has one circuit topology

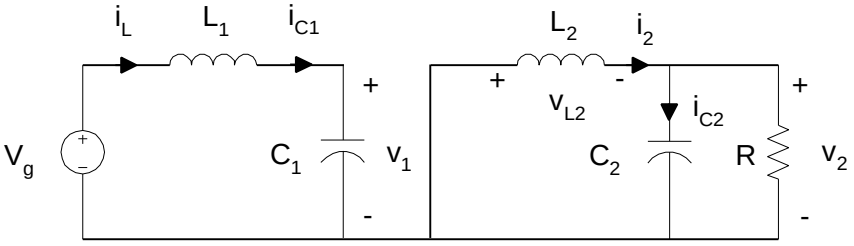


D: SW position 1

Q_1 on & D_1 off

In: Energy stored in L_1 via $I_L = I_1$
Out: Transfer energy from C_1 to C_2 via I_2

Case 2: D' when transistor off and diode on has a second, separate circuit topology



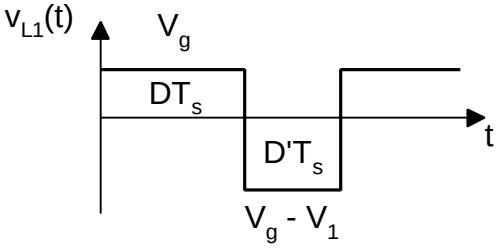
D': SW position 2

Q_1 off & D_1 on

In: Energy stored in C_1 via I_L
Out: Transfer energy from L_1 to C_2 via I_2

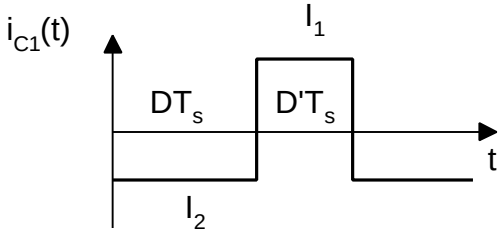
DC analysis conditions

Inductor volt-sec waveforms

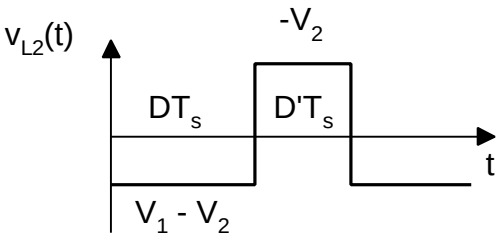


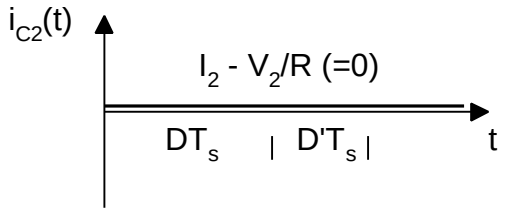
$DV_g + D'(V_g - V_1) = 0$

Capacitor I-sec waveforms



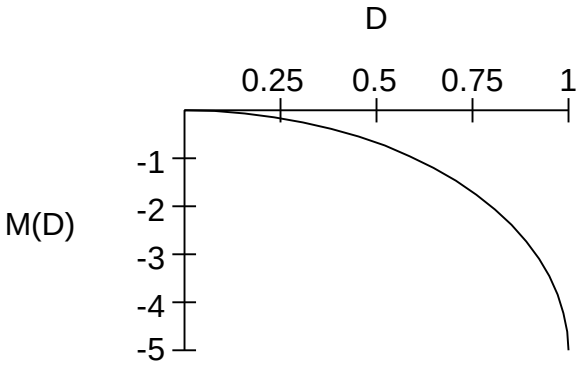
$DI_2 + D'I_1 = 0$





$D(-V_1 - V_2) + D'(-V_2) = 0$ $\qquad$ $I_2 - V_2/R = 0$

Yields $\dfrac{V_2}{V_g} = -\dfrac{D}{D'} = \dfrac{-D}{1-D}$



$$M(D) = \frac{V_2}{V_g} = -\frac{D}{1-D}$$

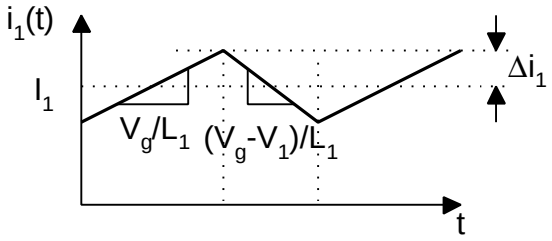
$\Rightarrow$ Inverting V_o from assumed polarity

Again initial polarities I_2, V_2 are assumed for analysis only. Same with I_1 and V_1

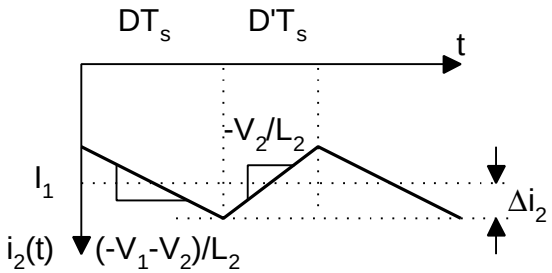
Knowing v_{L1}, v_{L2} vs. time gives i_{L1}, i_{L2}

(steps) (ramps)

i_{L1}:



i_{L2}:



Follows assumed v_L step waveforms

$$\Delta i_{L1} \equiv \frac{V_g}{2L_1} DT_s \text{ or } L_1 \equiv \frac{V_g DT_s}{2\Delta i_{L1}}, \text{ so specify } \Delta i_L \text{ to get L.}$$

$$\Delta i_L = \frac{V_1 + V_2}{2L_2} DT_s \text{ or } L_2 = \frac{V_1 + V_2}{2\Delta i_{L2}}$$

From DC solutions: $V_1 = V_g/D'$ and $V_2 = V_g(-D/D')$

$$L_2(\text{spec}) = \frac{V_g\left(\frac{1}{D'} - \frac{D}{D'}\right)}{2\Delta i_{L2}} DT_s$$

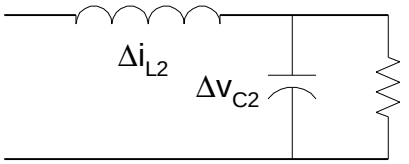
$$\frac{Vo}{V_g} = -\frac{V_2}{Vg} \text{ spec sets } D \equiv \frac{-D}{1-D}$$

$$L_2(\text{spec}) = \frac{V_g DT_s}{2\Delta i_{L2}}$$

Knowing i_{c1}, i_{c2} vs. time gives v_{c1}, v_{c2}.

(steps) (ramps)

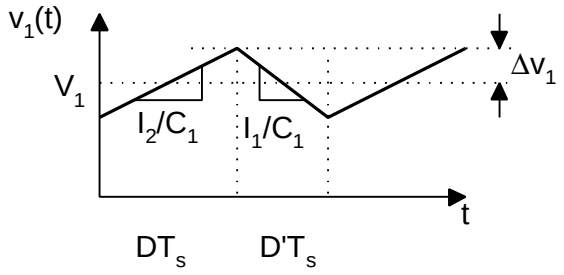
Since $I_2 \equiv v_o/R$ is only DC then Δi_{c2} is non-pulsating, if we also neglect prior Δi_{L2} then Δ **v_{c2} = 0**. This is not true! Actually we <u>cannot</u> do this.



Classic **Double Pole** Low Pass Filter

From Lecture 4, $\Delta v_c = \frac{\Delta i_{L2} T_s}{8C_2}$ and C(spec) = $\frac{\Delta i_{L2} T_s}{\Delta v_{c2} 8C_2}$

Use the I_1 waveforms and integrate:



$$\Delta v_{c1} = \frac{I_2}{C_1} DT_s \left(\frac{1}{2}\right)$$

Now from DC analysis:

$$I_2 = \frac{V_2}{R} \text{ and } V_2 = \frac{-D}{D'} V_g \Rightarrow I_2 = \frac{-D}{D'} \frac{V_g}{R}$$

$$\Delta v_{c1} = \frac{V_g D^2 T_s}{2D'RC_1}, \text{ so } C_1(\text{spec}) = \frac{V_g D^2 T_s}{2\Delta v_{c1} RC_1}$$

III. Static and Dynamic Switch Loss in Real Converters

A. General Switch Issues

Clearly voltage drops across the energy storage inductor,$V_{L,}$ differ in lossless vs. lossy converters.). The equivalent series resistance of inductors and capacitors add losses. In lossy converters efficiency is then a function of load current ,$I_{L,}$ while in lossless converters it is not . Also, s_u and s_d of di/dt in the inductor for lossless converters will not be equal to that of lossy converters. Hence, M(D) changes from the lossless case and becomes M(d,losses)

Switch devices also introduce losses. Thus, for example a diode alone adds both $V_D(on) + I_{on}R_D$ and this changes V_L as well as s_d slope.

Consider both DC and RMS currents and their static effects but neglecting dynamic switching losses:..

1. Static or Non-switching power losses:

Reactive elements:

- Capacitors
- Inductors on cores

In practice parasitic R, L, and C components arising often make up half the circuit model components though they do not appear on the bill of lading.

Resistance effects include:

- R_L of the inductor windings including skin effects.
- R_{on} of the double-pole, double-throw switch devices from device characteristics such as R_{on} of the transistor or R_{on} of the diode.
- ESR of all capacitors = $R_w + \frac{1}{w^2 R_{leak} C^2}$
- ESR effects for L

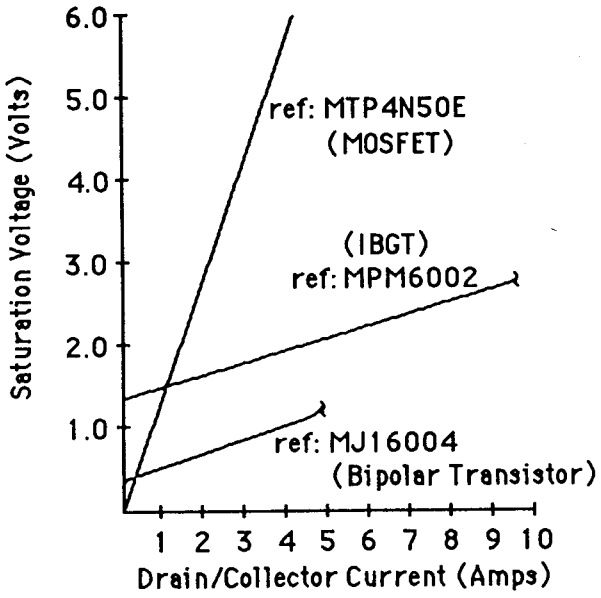
These may appear in input or output circuits depending on converter topology and cause loss of power efficiency, η, from the ideal case where they are neglected.

- Switch Device effects

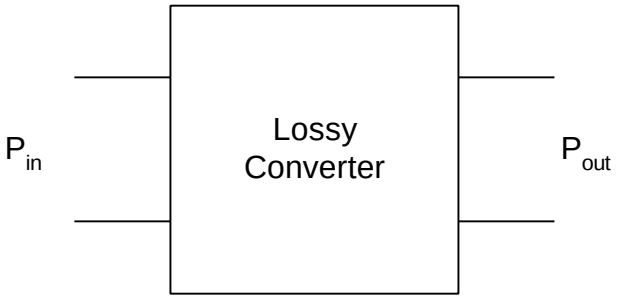
  For example V_{on} and R_{on} of semiconductor devices. See Chapter 5 of Erickson's text

- MOSFET's
- IGBT's
- diodes
- GTO (Gate turn-off Thyristor)
- MCT (MOS-Controlled Thyristor)

Below we show the V_{on} three switches:for MOSFET(highest value, for the IGBT, and for the BJT(lowest value).



Comparison of saturation voltages between MOSFETs, bipolar power transistors, and IGBTs.



$$h = \frac{P_o}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}};$$

typically $85 < \eta < 95\%$

Both resistive and device losses contribute to loss of efficiency. In summary,wire resistance: $I_L^2 R_L$ and $I_{RMS} \neq I_{AV}$
device losses due to V_{on} of the diode and R_{on}(transistor)

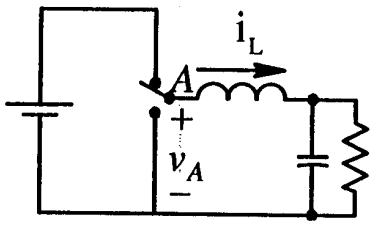
a. Diode V_{on} is fixed at $\approx$ 2V and $P_D(sw) = I_D V_{on}$ (usually R_{on} of a diode is negligible)

b. Transistor $R_{on}(I)$ or fixed and $P_{tr} = I_{tr}^2 R_{on}$ (usually V_{on} of a diode is negligible)

On the next page we show the two extreme switch conditions: cutoff and saturation.

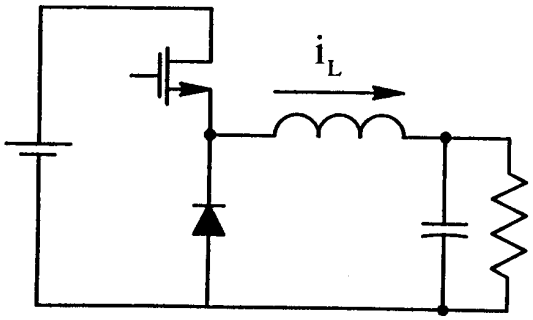
Bipositional Switch Implementation

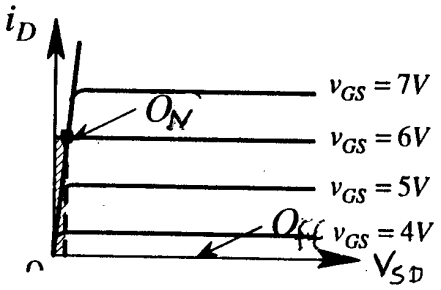
$(i_L > 0)$



$$q(t) = 0$$
$$= 1$$
$$v_A(t) = q(t)V_d = V_d$$
$$= 0$$

- Transistor operates as a switch
  - fully ON (or) $V_{SD} = 0$, $I_D \uparrow$
  - fully OFF $V_{SD} \uparrow$, $I_D = 0$





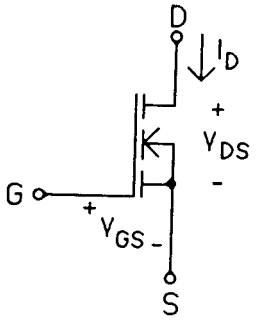
C. Finite Switching Losses at f_{SW}

1. General Considerations

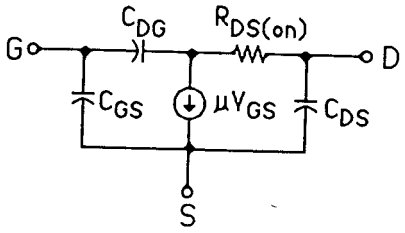
Switching loss is not easily obtained only from a device data sheet and circuit conditions. First, lets recall that static state loss is to a first approximation zero. We also state that for now we will neglect switch drive losses. That is don't forget that we have to drive the switch and this takes energy. The typical switch waveforms including gate drive are shown on the next page. In the ideal zero switching time case there is no loss due to transistor switching as we switch between two zero loss states.

TR on: $V_a = 0$, $I_a = \max$, $P_{tr} = 0$

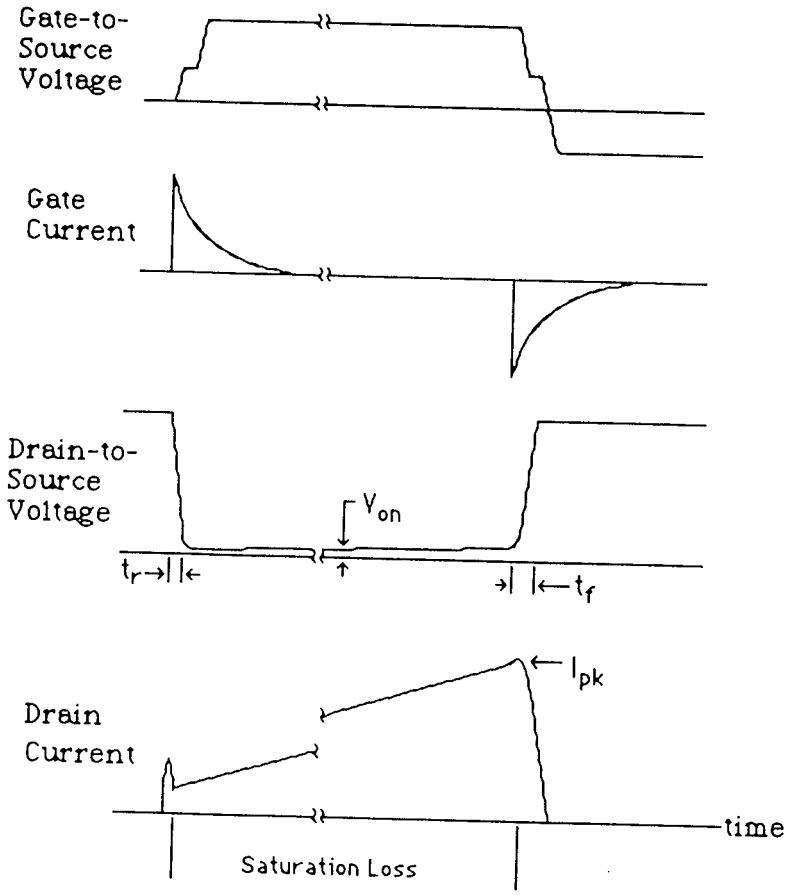
TR off: $V_a = \max$, $I_a = 0$; $P_{tr} = 0$



Symbol



Approximate Equivalent Circuit.



Waveforms for a power MOSFET in a PWM switching power supply.

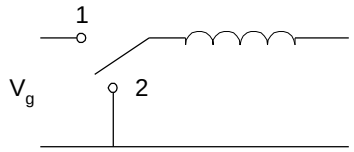
These I_d and V_{ds} waveforms will allow us to calculate switch loss for each switching cycle. The cycle includes two parts as each switch alternates on and off alternatively. We neglect switch driver losses for now.

Simple Two Switch Buck Type PWM Converter

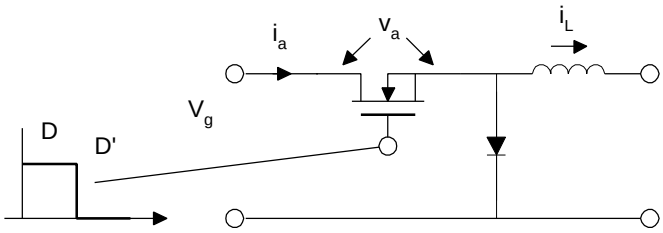
We will go through the switching sequence for the two cases below to recall the differences in each sequence.

1. Overview of the Two Switch Sequences

Ideal Buck Switch



Solid State Implementation



Case 1: SW1 ON

V_g applied for period D to left side of L

Transistor driven by control to be on for "D" period.

Diode off by reverse current flow and no active control is used to shut the diode off. The circuit shuts it off.

$P_{tr} = i_a v_a$ = ? Ideally if on $V_a = 0$, if off $I_a = 0$. So $P_{tr} = 0$ for the on/off states. However, during transitions between on/off we briefly go through $P_{tr} \neq 0$ states.

Next lecture we account for $V_{on}I_{on} = P_{on}$(loss for Tr).

What is missing in turning a diode off??

We will see that there are additional currents in the transistor when the diode is turned off due to storage charge. This will make the current waveforms

change from the ideal linear slopes we will first employ to one's closer to real waveforms.

Case 2: SW2 ON	Transistor is driven off by control after on time DT_s.
Left side of L is grounded for $D'T_s$	Diode switches on by current flow in the output circuit required
	Diode is on for $D' T_s$ period

We assume that there will be no or little storage charge in the transistor when it is shut off.

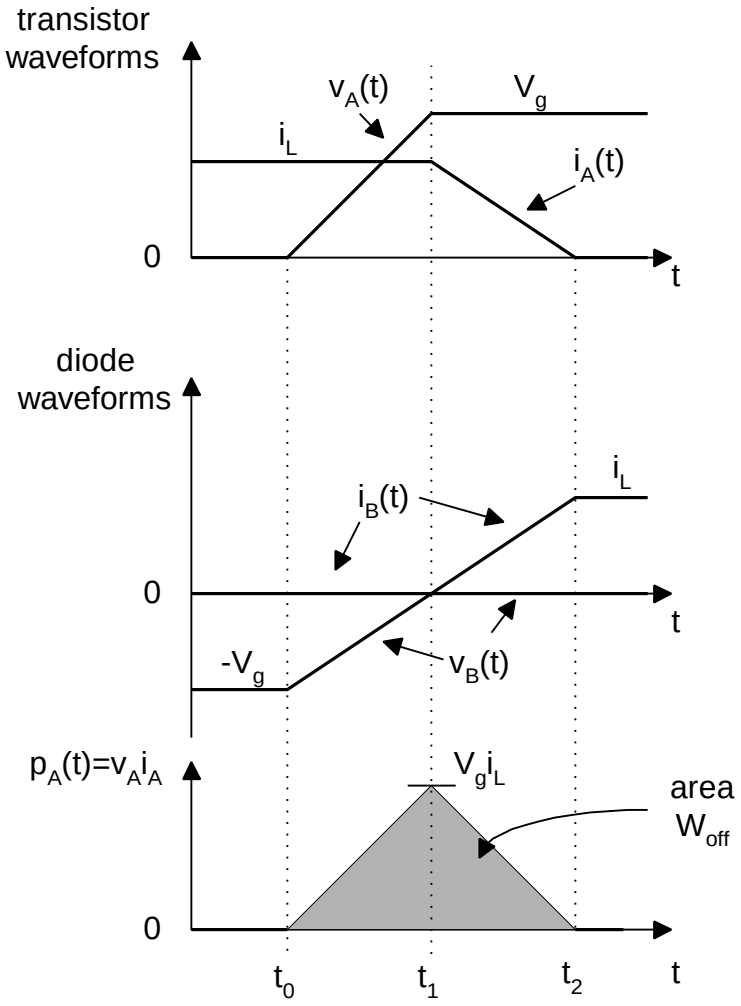
$P_D = i_D v_D$ = ? Ideally if on, $V_D = 0$, if off $I_D = 0$. So $P_D = 0$ for the on/off states. During switching transitions? In lecture 12-13 we fully account for $V_{on}I_{on} + I_{on}^2 R_{on} = P_{on}$(loss for D).

2. Easy Switch Transition: Transistor Off and Diode on

Due to finite switching time from transistor on to transistor off we get a brief interval of time each switching cycle where both i_a and v_a are big. Consider for a first approximation a linear transition between the two static states. This is seen in ideal i_a vs. time and v_a vs. time plots that ramp linearly. This is linear rather than instantaneous switching time introduces losses.

This linear case for switch loss is given on the next page.

Below we calculate energy lost to switching/commutation for both Tr on to Tr off and for Tr off or Tr on. Each transition has unique loss associated with it. We first look at Tr on to off. Here there is no diode stored charge to consider.



In real case during switching:

I_L = constant

$t = t_0 \rightarrow t_2$, (switching time is finite)

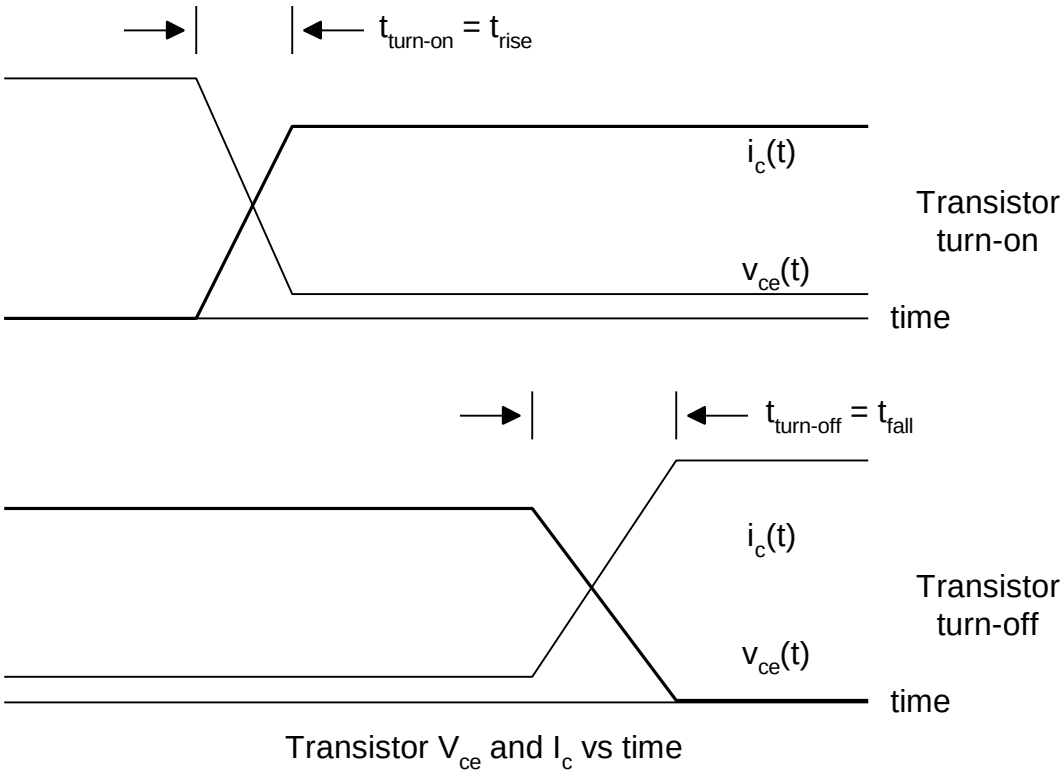
W_a (on/off) is the energy dissipated in transistor switching, calculated by integrating I*v over the switching interval $t_0 \rightarrow t_2$.

The switch operates at f_{sw} so the total switching loss is $P_{total} = f_{sw} W_{A1}$ (on/off)

W_{A1} (on/off) is the energy for going from TR on to TR off.

Piecewise linear switching allows a simple V-I area calculations for P_a and VIDt at calculations for W_A, switching energy per on/off switching event. During the brief (t_2 -t_0) switching interval. We can quantify this.

Given the transistor turn-on and turn-off curves as linear commutation shown below:



Transistor V_{ce} and I_c vs time

For **HW#2**: All students find the total energy lost during both turn-on and turn-off to be:

$$W(total) = (V_{off}I_{on}[t_{on} + t_{off}]) / 6$$

$V_{off}I_{on}$ is the maximum power handling P_{max} at f_s rates capability of the switch.

Therefore, $P(switch) = P_{max}[t_{on} + t_{off}] / 6T_{sw}$.
For example, low switching loss at 100 kHz requires:
$[t_{on} + t_{off}] / T_s \leq 100$ ns / 10 μs = 10^{-2} or 1%.

3. Complex Switch Transitions with Stored charge on diode and Inductor Current Waveforms

We will have to account for the fact that when the diode shuts off it dumps a big non-negligible stored charge. Also the circuit L will not allow V_A(transistor) and i_L(inductor) to change simultaneously as we will see below. In either case during switching we have current flow through devices with finite voltages across devices.

Thus, during the finite switching time power is dissipated in both the diode and the transistor. Various parasitic and circuit elements also store charge or current that may be causing additional switching loss. For example, transformer leakage inductance, wiring inductance and device capacitance's all store energy.

a. Diode Stored Charge

Consider now only the clamp diode of the buck topology which requires a high breakdown voltage, V_{bk}: High $V_{bk} \Rightarrow p\text{-}n^-\text{-}n^+$ and p-i-n devices.

Diode Tradeoffs:

High $V_{bk} \Leftrightarrow$ Low stored charge/Low R_{on}.

The extra n^- or I buffer junctions cause stored charge in the device during the on cycle. This charge must be removed to shut off the diode. High stored charge contributes to the low on resistance of the diode but this current may pass through the transistor causing power loss or high peak transistor currents. Next consider transistor switching loss.

Consider next the distinct case when switching occurs from TR off to TR on. The diode goes from on to off in the same interval. Below we show why this loss in the Buck circuit is unique because we do not have linear switching trajectories.

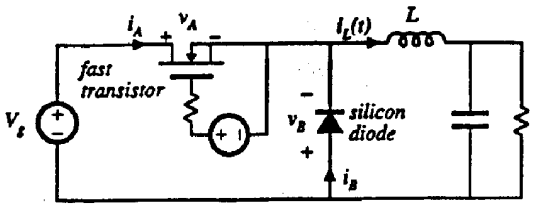


Fig. 4.50. Example, switching loss induced by diode stored charge.

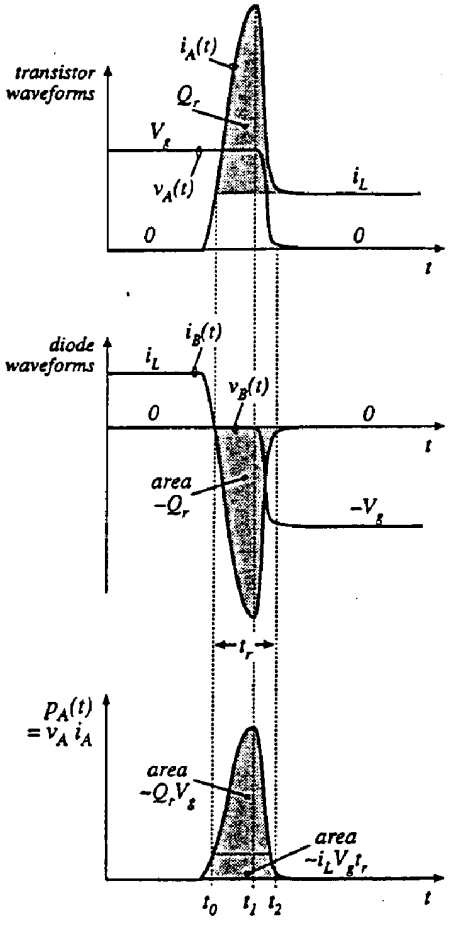


Fig. 4.51. Transistor-turn-on transition waveforms for the circuit of Fig. 4.50.

Usually the active transistor can switch much faster than the passive diode.

⇒ Diode reverse recovery and stored charge causes more switching loss because the peak transient diode current is way above linear transition values.

P_a(with diode) >> P_a(TR alone and no diode)

$v_a i_a \equiv P_{tr} = P_a$ (off/on)
Peak diode current boosts
P_a (off/on) >> P_a (on/off)
due to stored diode charge

Again,
P_{total} (on/off) = $f_{sw} W_A$ (off/on)

W_{A2} (off/on) is the energy for going from TR off to TR on

For high commutation frequency, f_{sw}, transient switching loss can exceed the normal static on/off DC losses . We will not

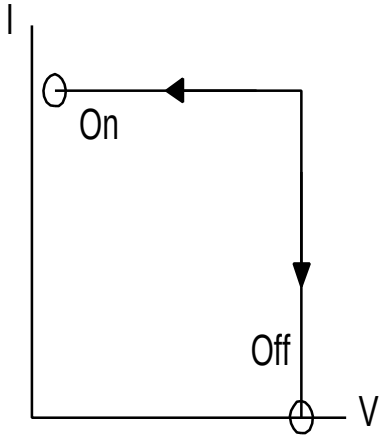
fully deal with these switched commutation losses until later lectures . We just set the stage here.

b. Inductor Waveform Effects

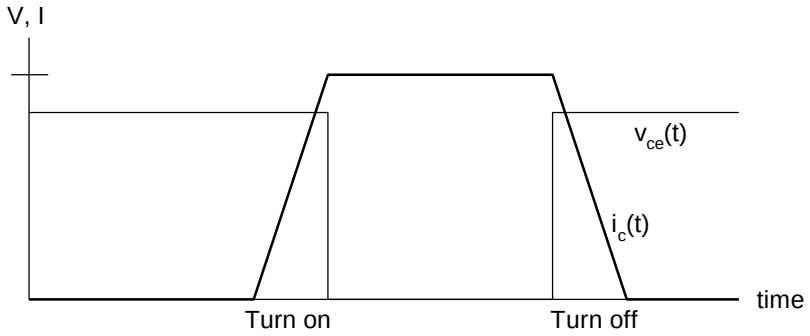
The inductor characteristics cause i_L to maintain its value even as the transistor turns off and v_a approaches V_g. In the plot below switching starts at t_o and ends at t_2; in between voltages and currents are finite at the same time causing power loss during the finite switch time.

For **HW #2**

For a rectangular switch commutation as shown below cause by circuit constraints of inductive loads when a diode clamps negative excursions.



We obtain transistor switching as shown on the next page for clamped inductive switching.



Transistor commutation in a buck converter with ideal diode.

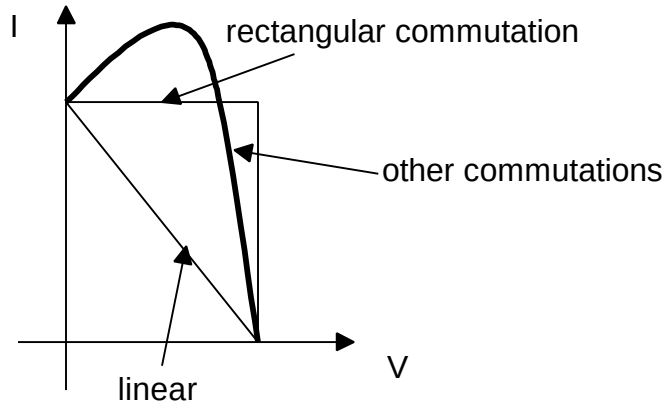
Show that the total energy lost during switching is:

$W(total) = (V_{off} I_{on} [t_{on} + t_{off}]) / 2$

Another problem but only for graduate students.

HW#2

Finally, for **HW#2** compare quantitatively linear, rectangular and other switching trajectories as shown below to derive a general relationship.



$W(total) = (V_{off} I_{on} [t_{on} + t_{off}]) / a$

a in the linear case is 6 but decreases as we saw to 2 in the rectangular switch commutation. Estimate a for the case of diode storage charge.

For HW#2 Due in 1 week:

1. Answer Questions asked throughout lectures 3-4.
2. ERICKSON Chapter 3 Problems 6 and 7.

Finally for **Extra Credit** but not required The non-ideal diode behavior causes the following measured waveforms and switch trajectories for a real buck converter.

First turn-off in a real Buck:

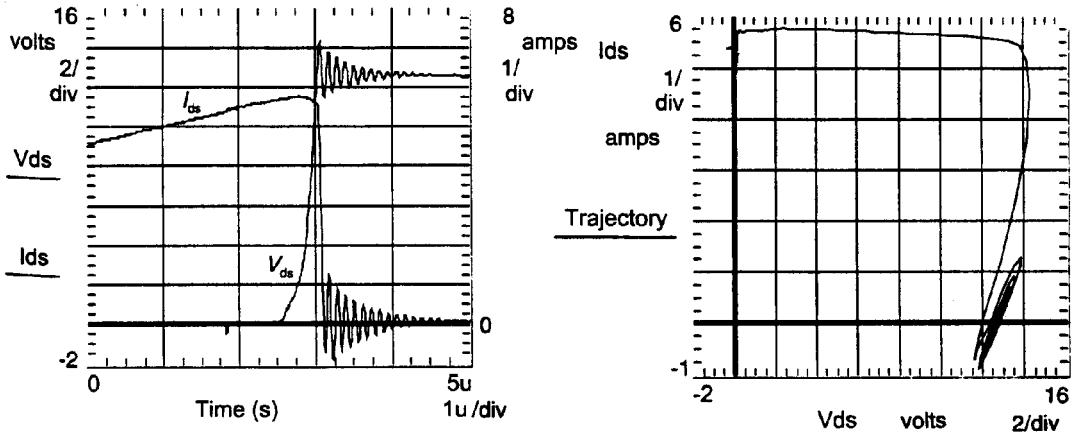


Figure 13.20 Turn-off time waveforms and trajectory for a real buck converter.

Explain what is occurring due to a non-ideal diode.

Next turn-on in a real Buck:

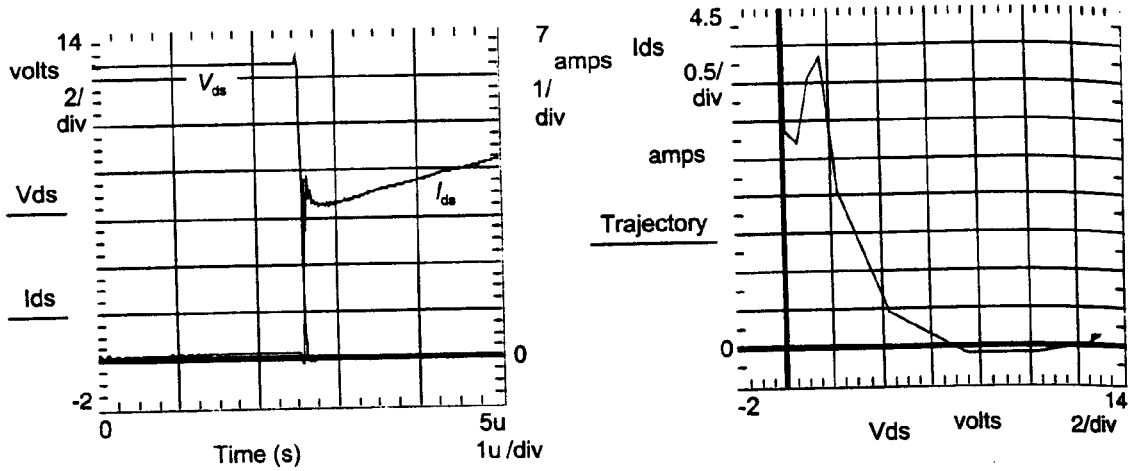


Figure 13.21 Turn-on waveforms and switching trajectory for a real buck converter.

Explain in detail why the waveform and trajectory curves are different from turn-off. Is this better or worse for losses?