LECTURE 9

A. Buck-Boost Converter Design
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   2. DC Operating Point via Charge Balance: I(D) in steady-state
   3. Ripple Voltage / "C" Spec
   4. Ripple Current / "L" Spec
   5. Peak Switch Currents and Blocking Voltages / Worst Case Transistor Specs

B. Practical Issues for L and C Components
   1. Inductor: $L = f(I)$?
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      c. Core Saturation above i(crit)
         $B > B_{sat}$, $L = f(i)$
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      b. Dielectric Materials
         (1) $\varepsilon(f_{sw})$
         (2) E(breakdown)

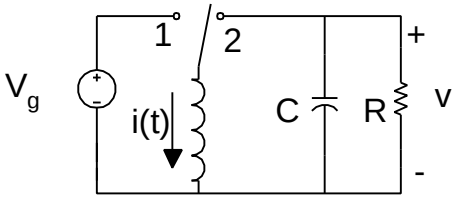
C. Appendix

A. Buck-boost Converter Design

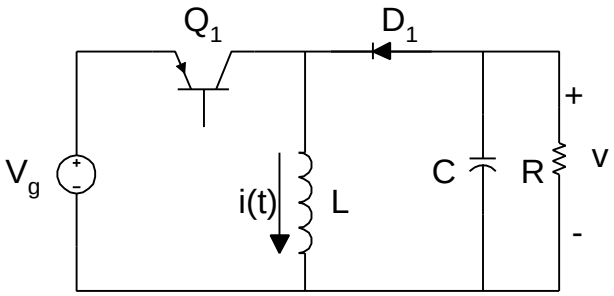
1.Volt-Sec Balance: f(D), steady-state transfer function

We can implement the double pole double throw switch by one actively controlled transistor and one passive diode controlled by the circuit currents so that when Q_1 is on D_1 is off and when Q_1 is off D_1 is on.

General form



Q_1-D_1 Switch Implementation

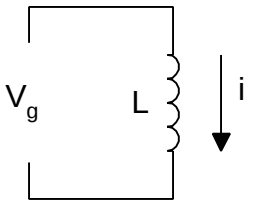


Two switch cases occur, resulting in two separate circuit topologies.

Case 1: SW 1 on, SW 2 off; Transistor Q_1 is on

Knowing V_{out} is negative means diode D_1 is off and load is not connected to input. This is a unique circuit topology as given below. Only Q_1 is active turned on/off by control signals.

Input Circuit
Topology:

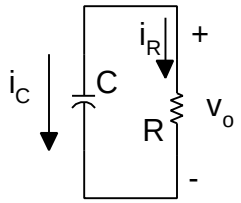


Q_1 is on; V_{on} small (2V) compared to V_g.

V_g is across L.

Output Circuit

Topology:



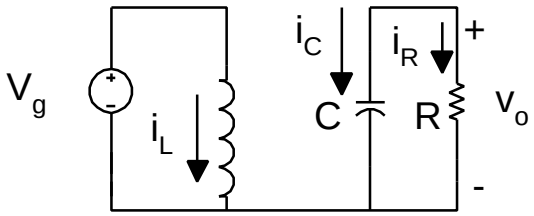
$i_C + i_R = 0 \Rightarrow i_C = i_R$

$|i_C| \equiv |i_{R|}|$ as they form a loop. Later we will see that actually v_o is negative.

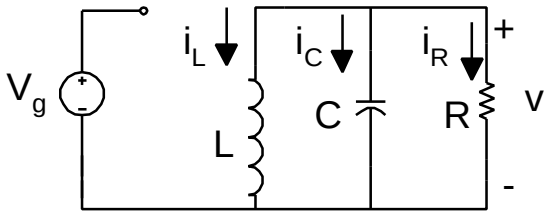
Case 2: SW 2 on, SW 1 off; Transistor Q_1 is off as set by external control signal applied to Q_1. This is a second circuit topology given on the next page.

Knowing i_L cannot change at switch since $i_L = \frac{\int v_L dt}{L}$, no need to actively control the diode with any control signals. It is automatically turned on by i_L flow to the left. The diode is automatically turned off by current flow to the right.

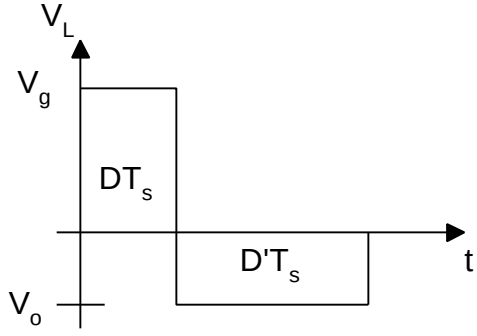
For DT_s, SW in 1:



For $D'T_s$, SW in 2:



We calculate the DC Transfer Function f(D) via V_L vs. time and volt-sec balance over both DT_s and $D'T_s$.



$V_g DT_s + V_o D'T_s = 0$

$$\frac{V_o}{V_g} = \frac{-D}{D'} = \frac{-D}{1-D} = f(D)$$

This is the Buck-Boost DC transfer function

By symmetry and power conservation $I_o/I_{in} = D'/D$ so that

$P_{in} = P_{out}$ neglecting losses.

Example: For a buck-boost circuit topology.
$V_o = -20$, $V_g = 30$. Find D and D' in steady state.

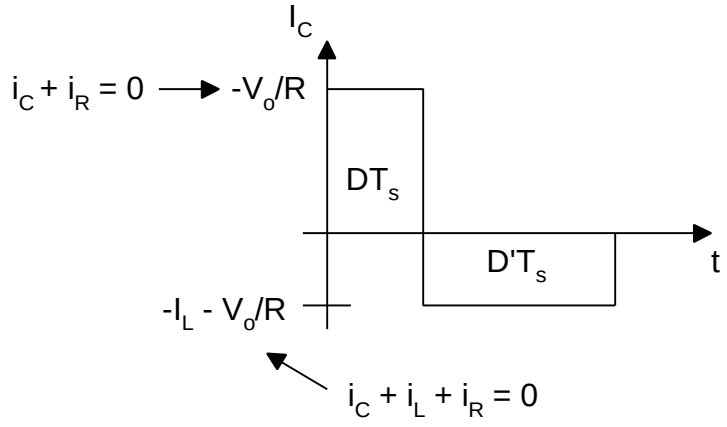
$$\frac{V_o}{V_g} = \frac{-D}{1-D} \Rightarrow D = \frac{V_o}{V_o - V_g}$$

$$D = \frac{-20}{-50} = 0.4 \text{ and } D' = 0.6$$

Clearly D would vary with other PWD circuit DC - DC converter topologies even for the same V_g and V_o.
If we further specified R_L as 4Ω then Iout = 20V/4Ω = 5A.
$P_{out} = I_{out}V_{out} = 5*20 = 100$ W. for a lossless converter
$P_{in} = 100$W and $I_{in} = 100/30$. What is i_L? Is it I_{in} or I_{out}?
Actually I_L will be the sum of I_o and I_{in} or 8.33 A as shown below. This trips up new students!

2. DC Current Operating Point in a Buck-boost circuit via Capacitor charge balance

We will show below by separate calculation that $I_L = I_o + I_{in}$.



We find that the inductor current is:

$$I_L \equiv -\frac{V_o}{RD'}$$

and / or

$$I_L \equiv \frac{V_g D}{(D')^2 R}$$

Example: $V_o = -20$V, $V_g = 30$V and $R = 4\ \Omega$.

$$I_L = \frac{-(-20)}{(4)(0.6)} = 8.33A$$ which is $I_{in} + I_{out}$

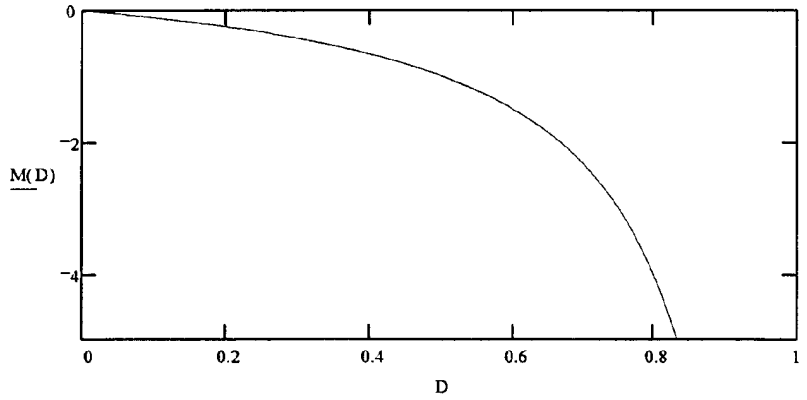
Plots of the DC voltage transfer function M(D) and I(D) shown below are not dependent on our choice of the switching frequency explicitly. Again a jitter in the switching frequency Δt can cause big changes in V_{out}.

$D := 0, 0.01 .. 0.99999$

$$M(D) := \frac{-D}{(1-D)}$$

Output is inverted!

M(D) is the transfer function relating the input Vg and the output V.

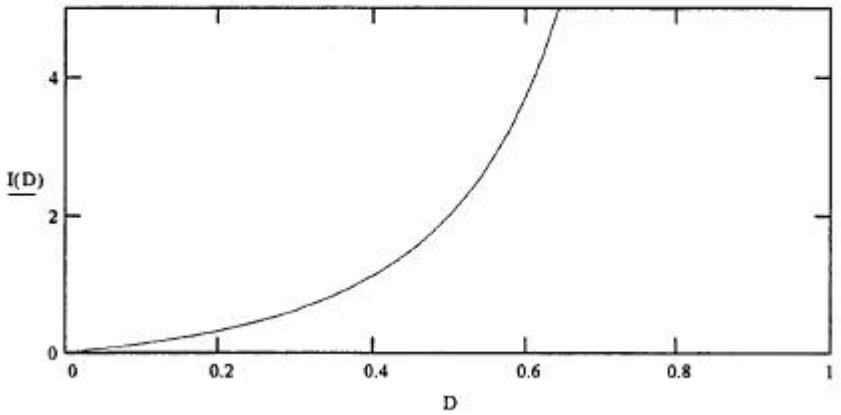


$$\frac{V}{V_g} = M(D)$$

As $D \rightarrow 1$
$M(D) \rightarrow -\infty$
(Won't occur in practice)

$$I(D) := \frac{D}{(1-D)^2}$$

I(D) is the function I / (Vg /R).



$$\frac{I}{Vg/R} = I(D)$$

As $D \rightarrow 1$
$I(D) \rightarrow +\infty$

Won't occur in practice

N.B. for **HW #2**, **how valid is the claim that M(D) and I(D) are <u>not</u> f(f_{sw})? Be specific and quantitative.**

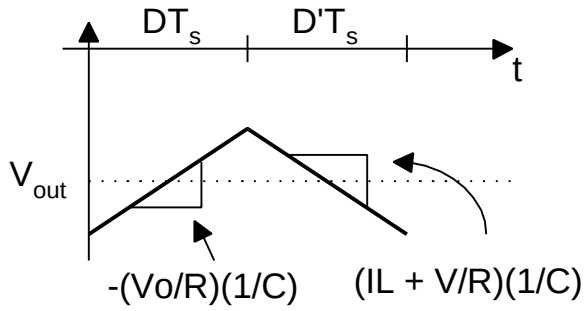
What about M(D) or f(D) being sensitive to the level of the load current?

For **HW #2**, also explain how simple power conservation can tell us that I(in) = M(D) I(out) as we outlined.

3. Choice of C value via ripple voltage spec across C

Choice of C value via ripple voltage spec across C is $\Delta v_C = \frac{\int i_C dt}{C}$.

Knowing charge balance occurs in steady state. Again V_o is inverted with respect to V_g.



$$2\Delta v_C = \frac{V_o D T_s}{RC}$$

$$C \equiv \frac{-V_o D T_s}{2\Delta v R}$$

C required to employ in order to have specified V_{out} ripple

Example: V_o = -20, Δv = 1/2%

Here we have a tighter Δv spec of 0.1V.

C required for various f_{sw}

f:	40KHz	400KHz	4MHz
C:	250μF	25μf	2.5μF

Which C is smaller and cheaper?
What are the practical f limits for capacitors?
Do capacitors have any losses?

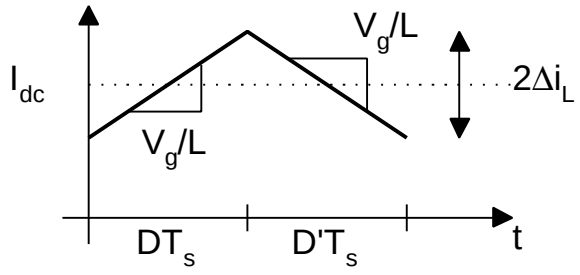
Finally, all capacitors have parasitic inductance associated with them due to wire leads on the capacitors. This introduces resonant frequencies. A typical case might be the 25 μF capacitor with L(lead

parasitic) = 20 nH (usually 5nH/cm of lead wire) of f_R = 225 kHZ ($w_R = \frac{1}{\sqrt{LC}} = 2\pi f_R$).

What occurs if f_R is close to the switching frequency f_s?

4. L value requirement via ripple current specification for quasi-static conditions.

The ripple current through L is $\Delta i_L = \frac{\int V_L dt}{L}$, and knowing volt-sec balance occurs in steady state.



$$2\Delta i_L = \frac{V_g D T_s}{L}$$

$$L \equiv \frac{V_g D T_s}{2\Delta i_L}$$

L required for given i_L ripple is a function of f_{sw}

Example: I_{DC} = 8.33A, ΔI = 10% = 0.83 A, D =0.4

	L required at f_{sw}		
f:	40 kHz	400 kHz	4 MHz
L:	179 μH	17.9 μH	1.79 μH

Which L is smaller and cheaper? What limits the f_{sw} for inductors? Do inductors have losses?

5. Peak currents and voltages versus transistor specs

The peak on current / peak off voltage specification must be met by the switches. Δi_L values effect maximum values of I_{peak} in the switches employed. i > i(critical) kills a solid state switch in nanoseconds. When switches turn-off peak stand-off voltages can also damage switches. Δv(ripple) sets V(peak) values.

Transistors are rated by both

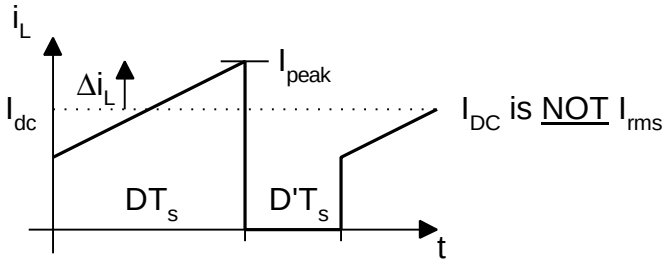
I_{DC}(max) - Depends on heat sink and power in TR.

I_{peak}(max) - If this is exceeded, TR is dead. No second chances

As well as by maximum rms values.

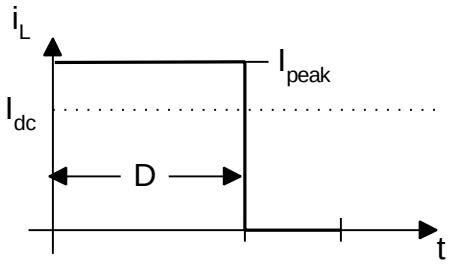
Diodes are the same as regards i > i(critical).

Consider the i_L waveform given below vs. time.

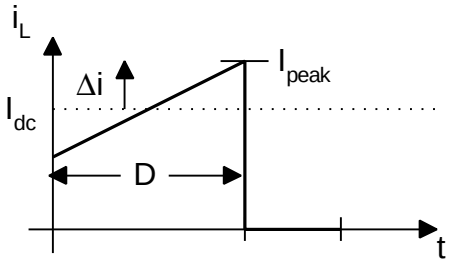


For complex waveforms Δi_L is measured from the I_{DC} baseline and is so defined throughout.

Some typical waveforms and rms values:



$$I_{rms} = I_{peak}\sqrt{D}$$



$$I_{rms} = I_{dc}\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{I_{dc}}\right)}$$

Fortunately, in Appendix I of Erickson's text (pgs. 703-707) there are summarized many common waveforms and associated RMS values. Hence, the definitions of peak currents, effective DC currents, and rms are all unique. Likewise manufacturers spec sheets for devices will give all three current spec's.

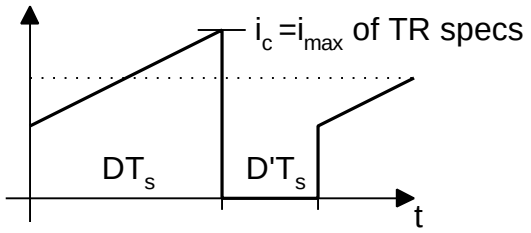
$I_{peak} = I_{DC}$(during DT_s) + Δi(during DT_s) ← 10-60% of I_{DC}

Device loss: $P_{av} = I_{rms}V_{on,rms}$ ← per cycle

Note: I_{DC} above is not I_{rms}

$P_{av} = f_{sw}P_{rms,cycle}$

Now we are using "D" to vary V_o via duty cycle control of applied voltage V_g. Later, in Chapter 11, we will introduce current control of PWM dc-dc converters. One nice feature of current control is that we can limit i_{peak} by $i_{control} \equiv i_{max}$. That is, if $i_{control}$ is exceeded the transistor is turned off and peak current damage can never occur.



Example:

- DC operating point P_{out} of buck-boost for V_o = 20V and R = 4 Ω is 100W.

  $\Rightarrow I_{dc} \approx 8.33$ A

- Consider these ac conditions during DT_s:

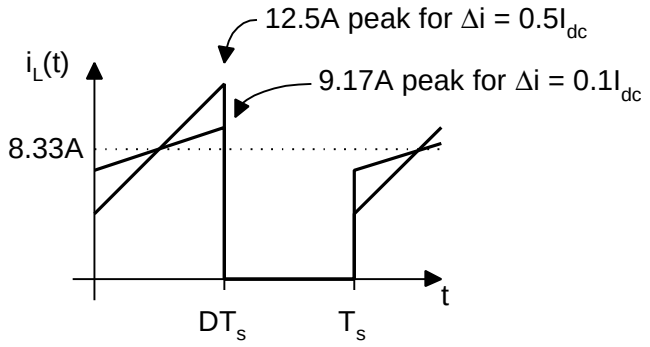
10% ripple	50% ripple
$\Delta i = 0.833$ A	$\Delta i = 4.17$ A
$I_{pk} = 9.17$ A	$I_{pk} = 12.5$ A

What about the cost of transistors and diodes to handle the peak currents?

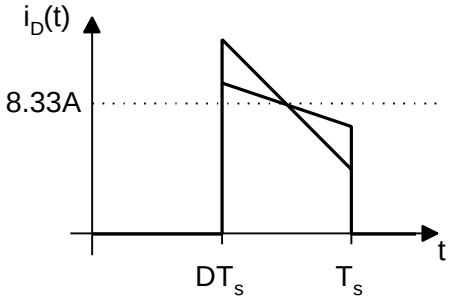
vs.

The cost of additional value inductors to reduce I_{pk}?

In this buck-boost circuit is I_{pk} the same for the diode and the transistor?



Inductor current



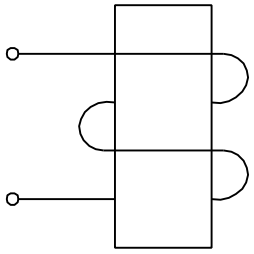
Diode current

B. Practical Issues for Inductive and Capacitive Components

We talked briefly about skin effect in wires at high frequencies in lecture 3. Now we briefly talk about capacitors and inductors at high frequencies. It is worthwhile to know early that the circuit elements are not what we first imagine but are rather very complex in their behavior due to parasitics and non-linear effects.

1. Inductors (costs, saturation, materials)

Copper wire is wound around a magnetic core



N turns

$$L = \frac{\mu N^2}{\mathcal{R}}$$

$\mathcal{R} = \frac{\ell}{\mu A}$ magnetic reluctance of flux path in H^{-1}

$$\Rightarrow L = \frac{\mu N^2 A}{\ell}$$ It appears $L \neq f(i_L)$

For a fixed L we can trade the amount of copper wire (N^2) for the amount of iron core (A) to achieve a desired value of L. We can also trade copper wire vs. core material choice depending on the size, weight and cost requirements. Core permeability itself varies with

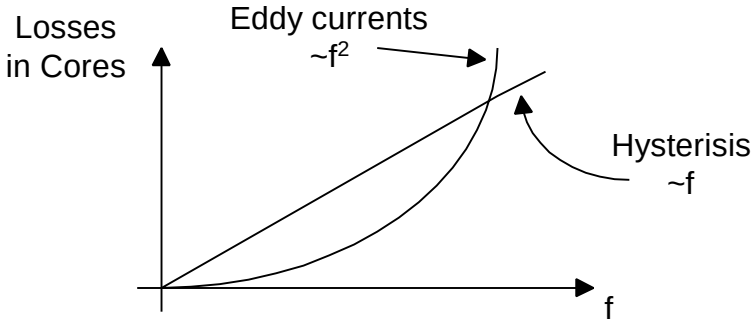
frequency and the term Ni=H. Where N is the number of wire turns on the core and I is the current in the wire.

a. Big L costs material and money:

(1) N^2 - number of turns of wire: costs in copper.
(2) A/ℓ - Area of magnetic material/length ⇐ costs in core size. Note you can trade core for copper to the extent we don't saturate the core.
(3) Higher μ material at given frequency costs. No materials have high μ above 1 MHz.

b. Various core materials for f_{sw}:

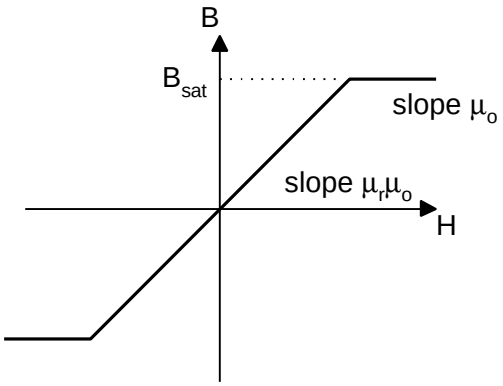
(1) 60 Hz - 20 kHz Iron cores are O.K., μ = 1000
(2) 20 - 80 kHz powdered iron, metal-glass, μ = 100
(3) 80 - 400 kHz use ferrite cores, μ = 10 - 100



These losses limit upper f_{sw} to 0.5 - 1 MHz for present cores. Perhaps with time low loss cores which operate at 10 Mhz can be found.

c. Saturation of flux

Actually the inductance $L(i_L)$ at high currents and for i > i(critical) L will suddenly decrease precipitously. This may cause higher currents and these kill solid state devices as well that are in series with the inductance.



We want to operate at H < H(critical) or B below B(saturation).

$\mu = \mu_r\mu_0$ only if $B < B_{sat}$ with B_{sat} units $Wb/m^2 \equiv$ Tesla;

Core Material	Maximum B_{sat}	f_{sw}(max) due to losses
Iron	~1-2 Tesla	kHz
Powdered iron	~½ to 1 Tesla	40 kHz
Metal-glass	~½ Tesla	100 kHz
Ferrite	~¼ - ½ Tesla	MHz

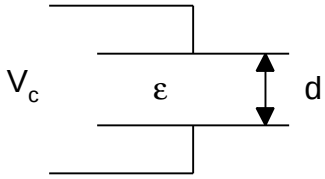
There is an apparent $B_{max}*f_{max}$ product that no core materials will exceed today. See chapters 12-14 in Erickson. Finally, in any analysis of magnetic materials try to include parasitic inductor effects as well due to flux leakage from the core. That is flux will leak out from a transformer core, for example, and cause parasitic inductor that is located before the ideal transformer. This causes lots on unexpected voltages in transformer circuits due to LEAKAGE INDUCTANCE.

2. Capacitor is $\frac{eA}{d} = f(f_{sw})$

a. Costs

Dielectric material choice for $\varepsilon(f_{sw})$ to achieve high C values.

Low f caps $\uparrow \varepsilon$
High f caps $\downarrow \varepsilon$
$\Rightarrow C = f(f_{sw})$



$V_c/D \equiv E_c \Rightarrow$ must not exceed break-down of material

Vacuum caps are best but since $\varepsilon = \varepsilon_0$ they are large and costly.

b. Capacitor Dielectric Materials

- $\varepsilon(f)$ matched to f_{sw}
- Material choice for ε is compatible with E(breakdown)
- Loss vs. f

The top circuit in the figure below shows the circuit model for a capacitor including:
R_w (wire losses due to skin effects at f_{sw}) >> R_{wire}
L_w (wire inductance) which is typically 500nH/m or 5nH/cm.

Beware L_w of 5nH/cm with a di/dt = 50A/200ns through a capacitor with lead lengths of only 8cm we can drop 100 V across L_w even before we place any voltage across C. Moreover, we could have a series resonant circuit at

$$w = \frac{1}{\sqrt{L_w C}}$$ if R_{leak} is large.

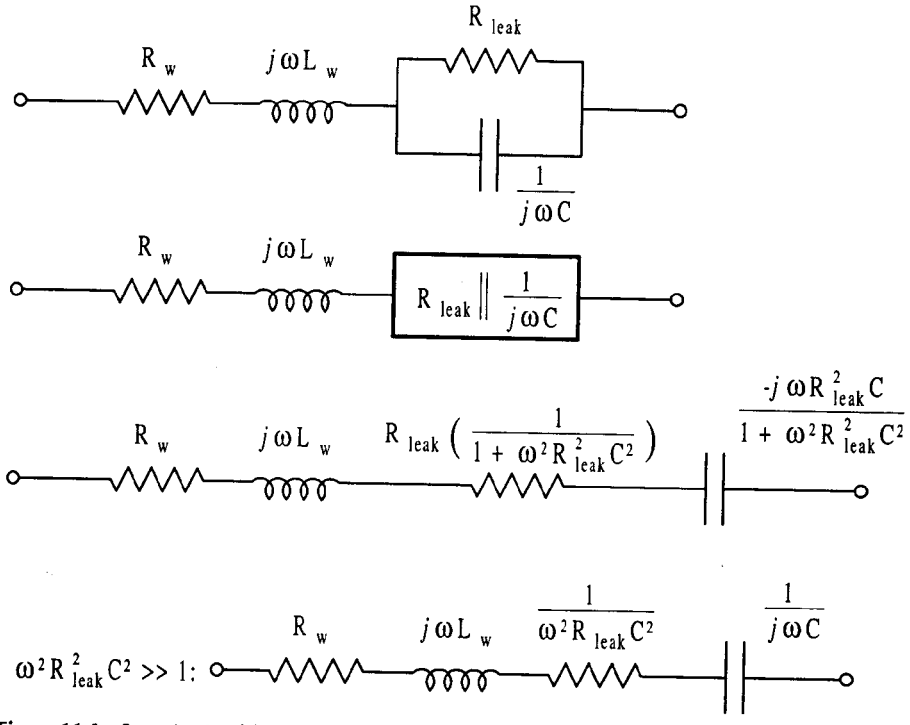


Figure 11.6 Steps in simplifying the equivalent circuit.

By simplifying the model as shown, we can derive the equivalent series resistance (ESR) used by C manufacturers.

$$ESR = R_w + \frac{1}{w^2 R_{leak} C^2}$$

$$\tan\delta = w\,C\,(ESR) \cong \frac{1}{wR_{leak}C}$$

If R_w is small then:

$$\tan\delta = \frac{wC}{w^2 R_{leak} C^2} = \frac{\frac{1}{wC}}{R_{leak}}$$ which measures capacitor loss

In terms of known measurements usually tan δ is specified for a capacitor so:

(ESR) = tan δ/wC

The ESR of a capacitor will decrease as w increases for a fixed tan δ.

Example #1: A 100 μF electrolytic C has 5 cm long leads and internal L of 15 nH. We are given tan δ = 0.2, constant for all f < 100 kHz. Find: w(resonance) of C

L_{total} = 15 + 5 * 5 nH = 40 nH

$w_R = \frac{1}{\sqrt{40 * 100}}$ = 80 kHz

Choose f_{sw} well below w_R, say 20 kHz and find ESR there.

ESR(20 kHz) = tan δ/wC = 8 mΩ

Example #2: A 2 μF C has an L(total) = 25 nH and tan δ = 0.01 is constant from 50 Hz to 200 kHz. Find the resonant frequency.

$w_R = \frac{1}{\sqrt{25\text{nH} * 2m\text{F}}}$ = 0.7 MHz

Calculate ESR at 120 Hz and 120 kHz

ESR(120 Hz) = tan δ/wC = 6 Ω

ESR(120 kHz) = tan δ/wC = 6 mΩ

Again for a fixed tan δ ESR decreases as f increases.

Extra Credit: For Homework #2 please review the properties of practical dielectric capacitors in the range of 0.1 to 1 MHz. Talk about tan δ and realistic **R** for real capacitors.

C. Appendix 1

RMS Values of Commonly-Observed Converter Waveforms

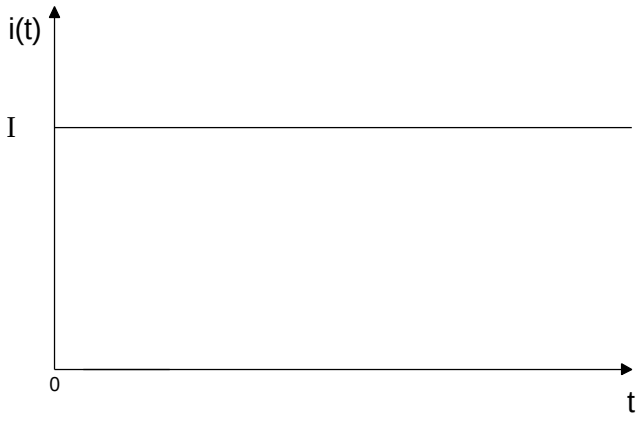
The waveforms encountered in power electronics converters can be quite complex, containing modulation at the switching frequency and often also at he ac line frequency. During converter design, it is often necessary to compute the rms values of such waveforms. In this appendix, several useful formulas and tables are developed which allow these rms values to be quickly determined.

RMS values of the doubly-modulated waveforms encountered in PWM rectifier circuits are discussed in section 18.1.

A 1.1 Some common waveforms

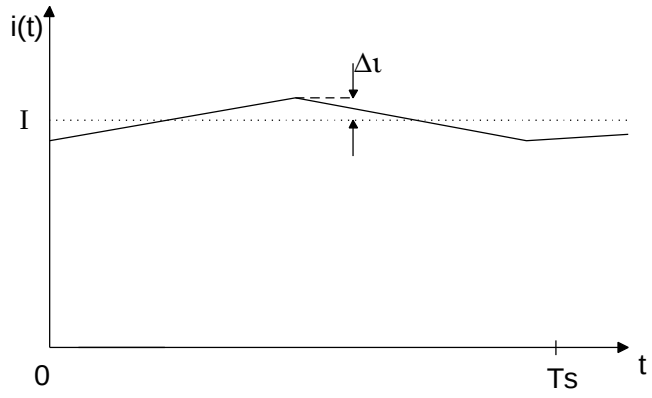
DC, Fig A 1.1:

$$rms = I$$



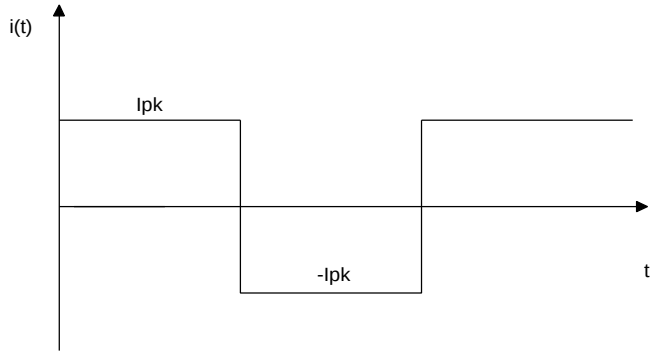
DC plus linear ripple, Fig A 1.2:

$$rms = I\sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{I}\right)^2}$$



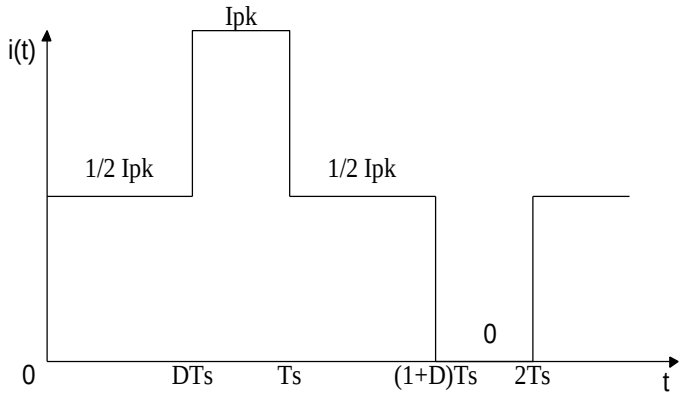
Square wave, Fig. A 1.3:

$$rms = I_{pk}$$



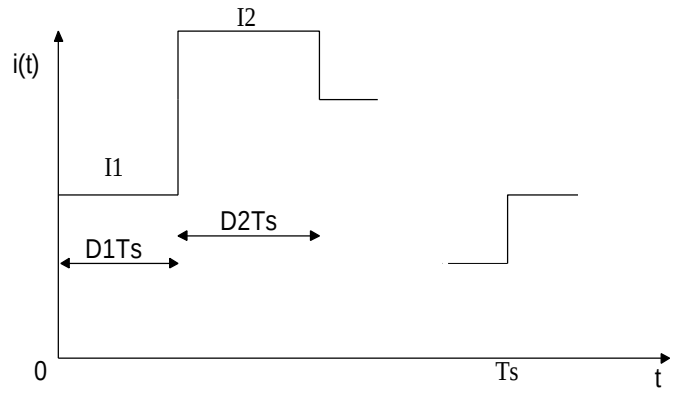
Center-tapped bridge winding waveforms, Fig. A1.10:

$$rms = \frac{1}{2} I_{pk} \sqrt{1+D}$$



General stepped waveform, Fig. A1.11:

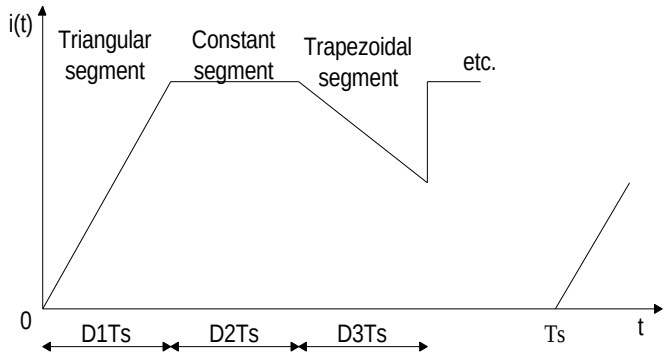
$$rms = \sqrt{D_2 I_1^2 + D_2 I_2^2 + \ldots}$$



A 1.2 General piecewise waveform

For a periodic waveform composed of n piecewise segments as in Fig. A 1.12, the rms value is

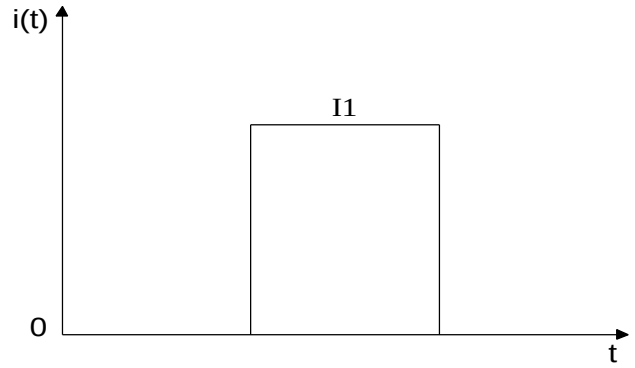
$$rms = \sqrt{\sum_{k=1}^{n} D_k u_k}$$



Where D_K is the duty cycle of segment k, and u_k is the contribution of segment k. The u_k's depend on the shape of the segments — several common segment shapes are listed below:

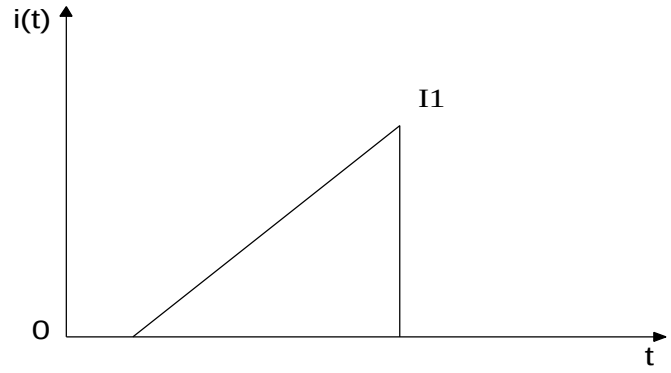
1. Constant segment, Fig A 1.13:

$u_k = I_1^2$



2. Triangular segment, Fig. A 1.14:

$u_k = \frac{1}{3} I_1^2$



3. Trapezoidal segment:

$D_3 = (0.1ms)(10ms) = 0.01$

$u_3 = (I_1^2 + I_1 I_2 + I_2^2)/3 = 148A^2$

4. Constant segment

$D_4 = (5ms)(10ms) = 0.5$

$u_4 = I_2^2 = (2)^2 = 4A^2$

5. Triangular segment

$$D_5 = (0.2ms)(10ms) = 0.02$$

$$u_5 = I_2^2 / 3 = (2)^2 / 3 = 1.3A^2$$

6. Zero segment

$$u_6 = 0$$

The rms value is

$$rms = \sqrt{\sum_{k=1}^{6} D_k u_k} = 3.76A$$

Even though its duration is very short, the current spike has a significant impact on the rms value of the current — without the current spike, the rms current is approximately 2.0 A.