LECTURE 8

Fundamental Models of Pulse-Width Modulated DC-DC Converters: f(D)

I. Quasi-Static Approximation

A. Linear Models/ Small Signals/ Quasistatic

$$\Delta V = \frac{I}{C} dt \quad \text{Amp-Sec/Farad}$$

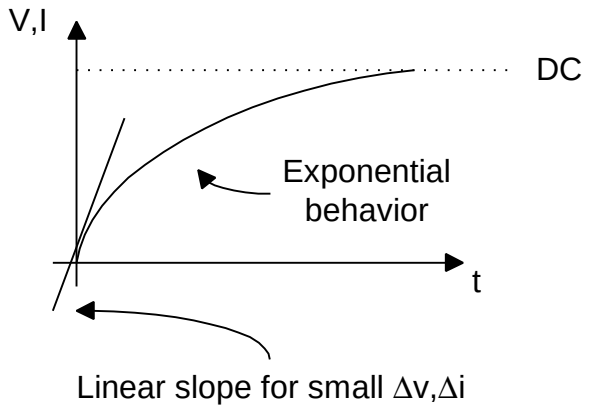
$$\Delta I = \frac{V}{L} dt \quad \text{Volt-Sec/Henry}$$

1. Switched Capacitor Network Dynamics and in Steady-State
2. Switched Inductor Network Dynamics and in Steady-State
   a. General Issues of $i_L(t)$
   b. Buck Circuit Topology
   c. Boost Circuit Topology
   d. Buck-Boost Circuit Topology

B. EXAMPLE OF BOOST DESIGN

I. Quasi-static Approximation

Quasi-static Basic Review: Signals in the quasistatic case



Usually in simple RC and LR circuits there is an exponential change of signals from 0 → V(dc), I(dc)

A useful approximation is: for τ = RC is that the exponential signal reaches a certain percent of final at various nτ.

ln10 * $\tau \rightarrow 90\%$ at 2.3τ

2ln10 * $\tau \rightarrow 99\%$ at 4.6τ

3ln10 * $\tau \rightarrow 99.9\%$ at $(3 * 2.3 = 6.9\tau)$

τ = RC sec for V

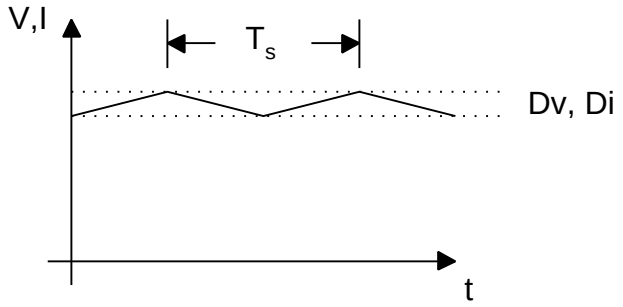
τ = L/R sec for I

But for times much less than τ, linear behavior occurs allowing great simplification. In switching rather than exponential circuits f_{sw} and T_{sw} are chosen such that they are much smaller than the RC and L/R time constants.

A. Small signal linear model

In short, since we usually have in dc-dc converters ac changes that are small, and switching times much faster than circuit time constants we can use simple linear relationships rather than differential equations.

For example the triangle wave ripple about a steady state DC level:



We can linearize time behavior for:

$(\Delta v, \Delta i) << (V, I)$

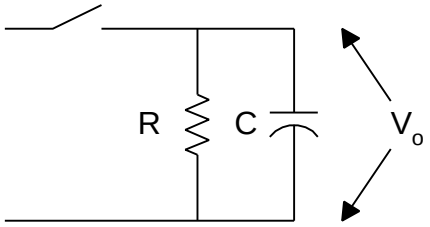
$T_s << (RC, L/R)$

Then capacitor voltage and inductor current signals vary <u>linearly</u> with time, $\frac{I}{C}dt = \Delta v_C$, $\frac{V}{L}dt = \Delta i_L$

1. Switched Capacitor Network: Assume a DC equilibrium exists.

Assume a series switch operating at f_{sw} with on duty cycle D. f_{sw} has a time period T_s moreover, the off time between pulses $D'T_s$ is much less than the RC delay. In short the switch is on for DT_s and off for $D'T_s$.

Drive to RC network is assumed to be a Norton Eq. Current Source



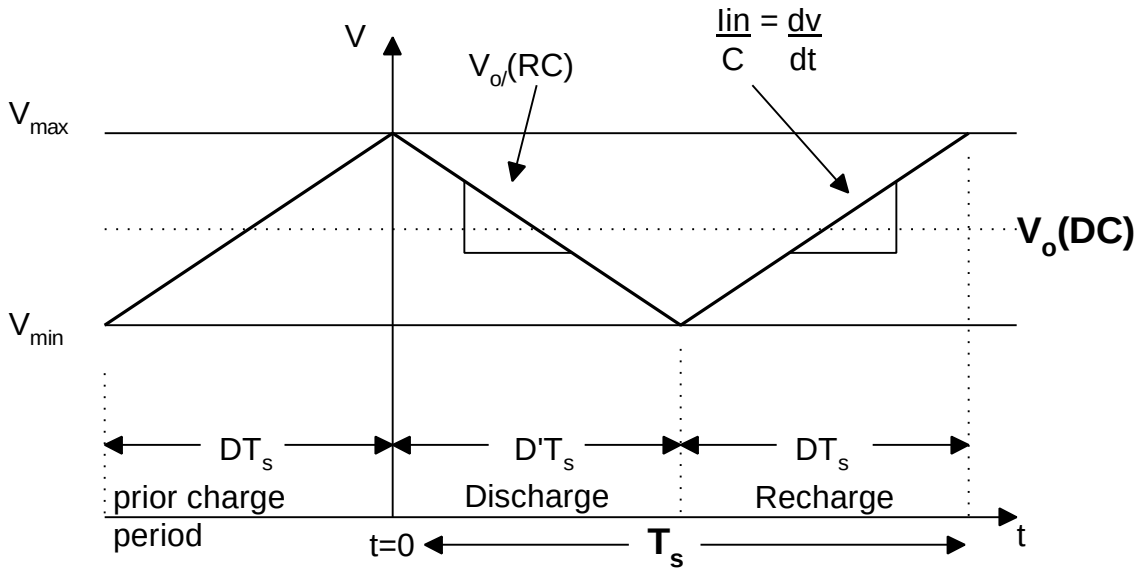
Switch at f_s: Switch Closed for DT_s and RC charges due to supply current.
Switch Open for $D'T_s$ and RC discharges due to load current demands.

a. Consider the switch open: Load discharge period $D'T_s$ During discharge of C by $I_{out} = V_{out}/R$(steady state), we find the voltage drop across C during interval $D'T_s$ is.

$$\Delta V(\text{during } D'T_s) = \left(\frac{V_o}{R}\right)\frac{1}{C}D'T_S$$

Clearly, in a PWM dc-dc converter in steady state during the next switch closed period must recharge C back to V(steady state). So a net current flows to C during the DT_s.

So in equilibrium at the output we have a maximum, a minimum, and an equilibrium DC value as shown below.



For steady state to occur over a switch cycle in a capacitor $V(T_s) \equiv V(0)$. Otherwise V_c grows till dielectric breakdown of C occurs.

Discharge slope over $D'T_s$: $V_o/(RC) = I/C$ appears linear if $RC >> D'T_s$ or $\Delta v << V$

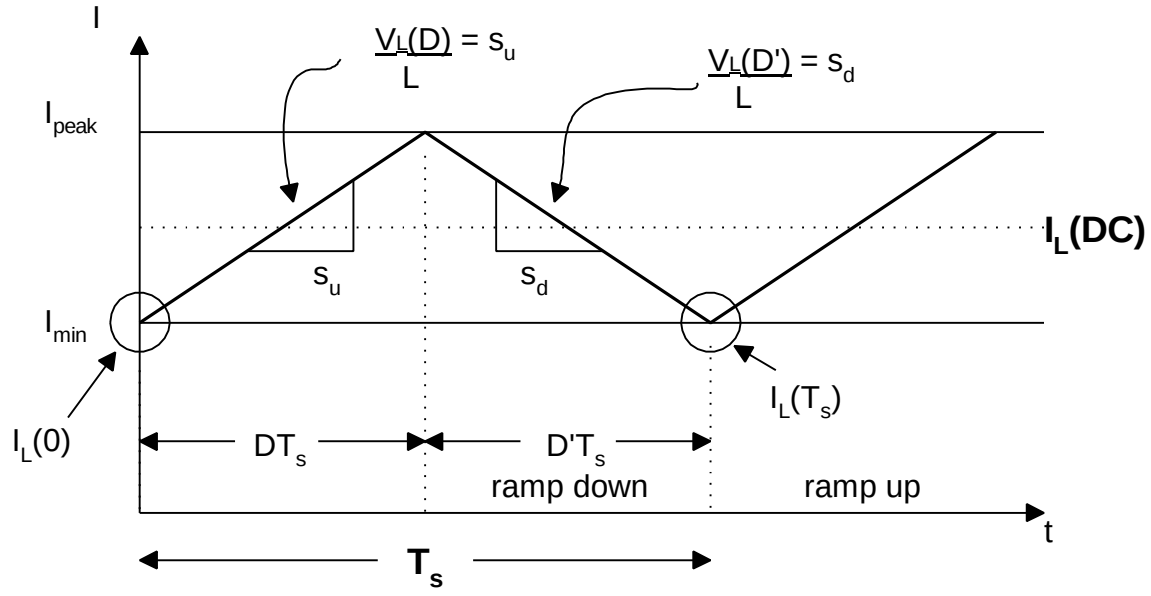
Charge slope over DT_s: I_{sw}(DC component)/C

$I_{sw}DT_s/C$ must equal ΔV lost during discharge for steady state

2. Switched inductor in steady state

We apply a square wave across V_L and see i_L vary as a triangle wave.

a. General i_L vs. time over T_s



Assume v_L during DT_s is positive and that v_L during D'Ts is negative. In the most general case, $|v_L(DT_s)| \neq |v_L(D'T_s)|$ due to different switched topology of circuit during DT_s and $D'T_s$.

$$\Delta i = \frac{1}{L}\int V_L dt \equiv \text{amperes}$$

We repeat that $V_L(DT_s) \neq V_L(DT_s)$ due to different switched voltages.

We assumed that for steady state to occur in an inductor over one switching period $i_L(T_s) \equiv i_L(0)$ or $s_u DT_s = s_d D'T_s$. Otherwise, i_L drifts upwards or downwards until i > i(critical) causing inductor core saturation.

Note: starting at $i_L(0)$ going to $I_L(DC)$ over a time DT_s,

$$i_L(DT_S) = i_L(0) + s_u DT_S$$

$$D = \frac{I_L(DC) - i_L}{s_u T_S} = \frac{\Delta i}{s_u T_S}$$

The proper D value is self-set for steady state to occur, likewise starting at $I_L(DC)$ @ DT_s going back to $i_L(0)$ at T_s takes $D'T_s$ to accomplish.

$$i_L(T_S) = i_L(0) = i_L(DT_S) - s_d D' T_S$$

$$0 = s_u DT_S - s_d D' T_S \leftarrow \text{Volt-sec balance in steady state.}$$

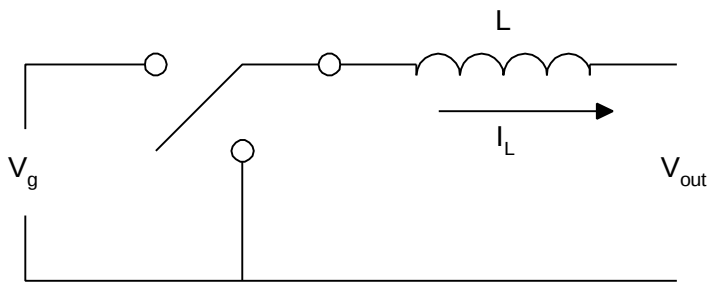
$$\frac{s_d}{s_u} = \frac{D}{D'}$$

That is for steady state to occur the smaller the off fraction D' the larger the discharge slope s_d must be and the bigger the on time D the smaller s_u must be.

b. Buck Circuit Topology

In the Buck the inductor position in the circuit topology of the dc-dc converter varies but it always has the switch attached. To avoid KVL violations we need to have an inductor to buffer the V_{out} and V_{in} which are temporarily connected by the switch network.

Here $V_o = DV_{in}$ and V_o cannot exceed V_{in}.
The right side of L is fixed at V_o which for regulated of feedback supplies is often dead constant. The left side of L is switched from V_g to ground. V_g sometimes varies for raw or unfiltered DC but is usually considered constant as well. Over the period T_s the switch goes up for a time DT_s and down for a time $D'T_s$.



For switch up:

$$s_u = \frac{V_g - V_o}{L}(A/s)$$

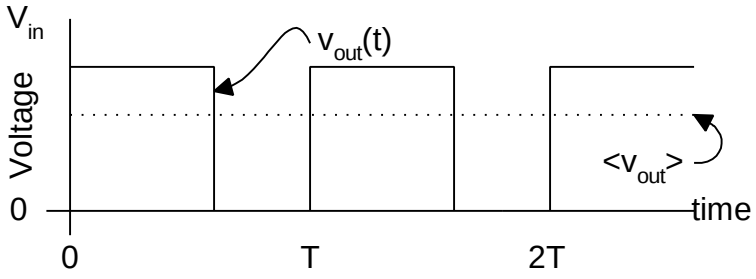
For switch down:

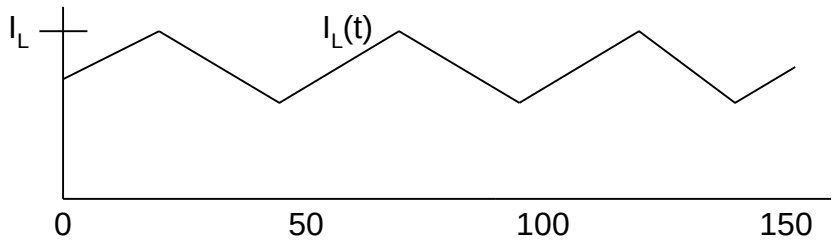
$$s_d = -\frac{V_o}{L}(A/s)$$

a very fixed slope

Buck example: For $V_g = 20$ and $V_o = 15$ we find D = 0.75 for Buck topology.

The v_L and i_L output waveforms for the buck are shown below:

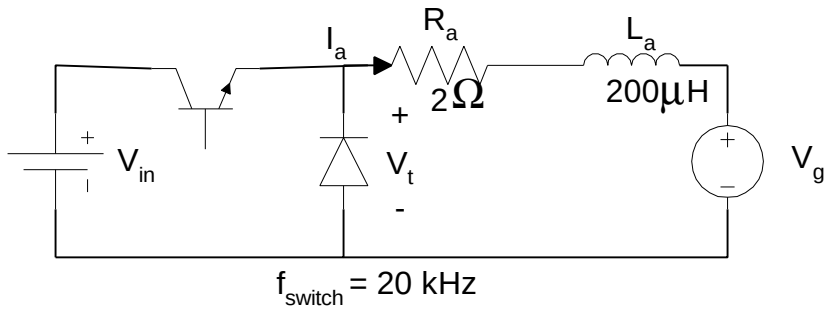




Note: 1. $V_o = DV_{in}$ 2. $I_{in} = DI_{out}$ 3. $P_o = P_{in} = DV_{in}I_{out}$

4. $V_{out}(rms) = \sqrt{D}\,V_{in}$ 5. What is $I_{out}(rms)$?

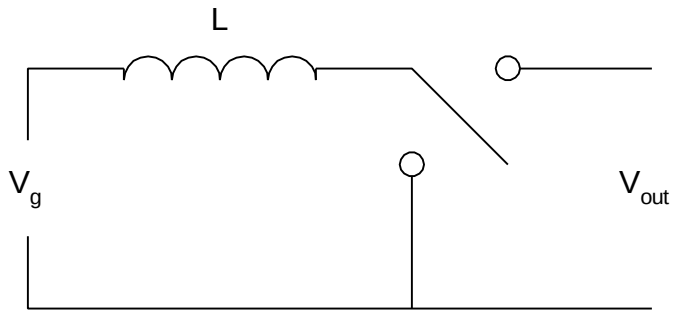
A simple dc motor control is shown below. Recall that $V_g = k_\phi w$(motor rotation). By setting V_T(DC) via D we can determine motor speed.



One can show for R_a small, V_g should be the average value of $V_t = D_1 V_{in}$ hence we can control motor speed by varying either V_{in} or D: w(motor) = DV_{in}/k

c. <u>Boost</u> Circuit Topology

The left side of L is fixed at V_g (raw dc) and the right side of L is switched from V_{out} to ground. Again L keeps KVL violations from occurring during switching.



For the switch to ground:

$$s_u = \frac{V_g}{L}(A/s)$$

For the switch to V_o:

$$s_d = \frac{-(V_g - V_o)}{L}(A/s)$$

Here, $V_o/V_{in}=1/(1-D)=1/D'$. This gives output greater than input.

<u>Boost Example</u>: V_g=20, V_{out}=50

$\Rightarrow V/V_g = 1/D' = 1/0.4$, D = 0.6

↑

Unique f(D) for Boost topology

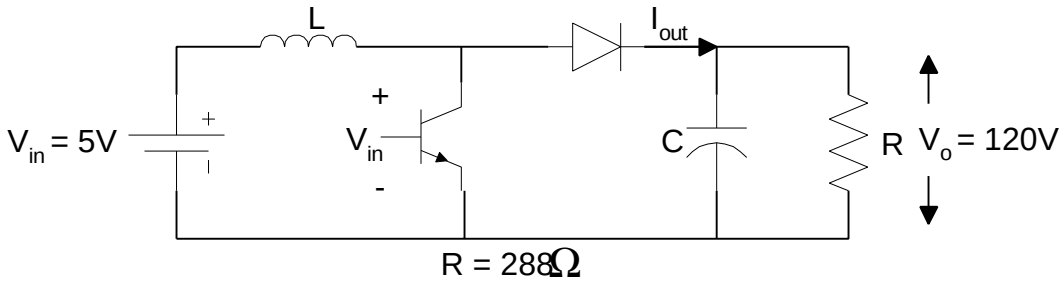
Verify $s_d/s_u \equiv D/D' = 0.6/0.4 = 1.5 = 30/20$

We can consider the l as transforming V_g into a current source input to the switch to achieve:

$V_{out} = V_{in}/(1-D)$ and $I_{in} = I_{out}/(1-D)$.

Note $P_{in} = P_{out}$ both on average and instantaneously, as we assumed zero losses in the converter switches as well as L-C components.

Consider the boost circuit below:



Goal: $V_{in} = 5V$ but I_{in} fixed $\pm$ 0.1%

$V_o = 120V \pm 0.1\%$

$P_{in} = P_o = 50W$

Hence for zero loss $I_{in} = 10A$ and $I_o = 0.42$

f_{sw} is fixed at 20 kHz

or $T_{sw} = 50\ \mu s$

Solution $\Rightarrow$ The off time of the switch transistor is:

$D' = 5/120 = 0.042$ Recall $D + D' = 1$

So the diode is on for $(0.042)(50) = 2.1\ \mu s$ out of 50 μs and the transistor is on for 47.9 μs. This makes sense as we need more time to build from 5V to 120V than to discharge the 120V.

For the lossless operation $I_{in} = 50/5 = 10A$ and we specify $\Delta I_{in} = \pm$ 0.1% = $\pm$ .1A. This Δi specification sets the L choice

$e = L\ di/dt$(on time of transistor)

$5 = L\ (0.2\ A/47.9\ \mu s)$

$L \geq 1.2$ mH to insure $\Delta I_{in} < 0.01$. For lossless operation $I_{out} = 50/120 = 0.42$ A. Our $\Delta V_{out} = 120 * \pm 0.01 = \pm 1.2V$ this ΔV_c sets the C choice

i = C dv/dt(off time of the diode)

0.42 = C 2.4/2.1 μs

$C \geq 83.3\ \mu F$ for $\Delta V_o \leq 0.01$

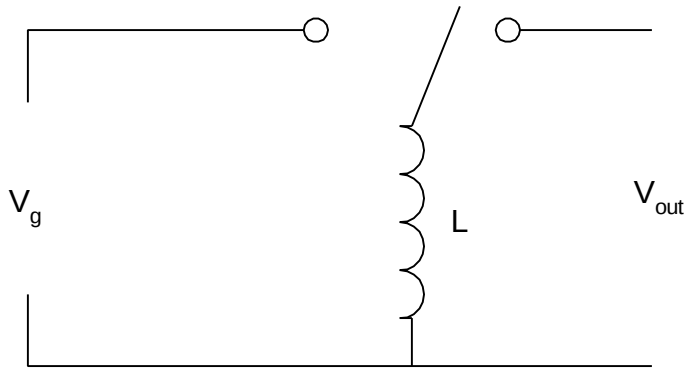
Finally prove to your self that a ± 50 ns time jitter on the transistor switch time causes V_{out} to vary from 117 to 123 V or ± 2.5%.

d. Buck-Boost Circuit Topology

Bottom of L is fixed at ground while the top side switches from V_g to V_o. For the case of feedback in the circuit, V_g could be crude rectified DC and V_o regulated DC.

Here $V_o/V_{in} = D/D'$ and the output is opposite polarity to the input moreover we overcome the $V_{out} < V_{in}$ limitation of the buck and the $V_{out} > V_{in}$ limitation of the boost. No KVL violations occur as each voltage supply only sees L which appears as a current source.

For analysis below we assume both do not vary over T_s.



Switch at V_g:

$$s_u = \frac{V_g}{L}(A/s)$$

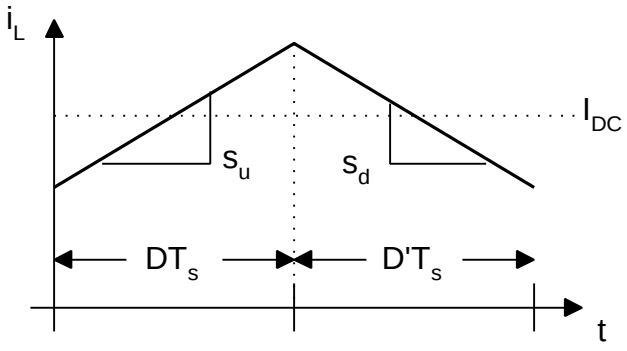
Switch at V_{out}:

$$s_d = \frac{V_{out}}{L}(A/s)$$

s_d very fixed for feedback case

$$\Rightarrow \frac{V_{out}}{V_g} = \frac{-D}{D'}$$

Now, by inspection, a buck-boost has the simple slopes switched since no potential difference occurs in V_L:



Upslope:

$$s_u = \frac{V_g}{L}(A/s)$$

Downslope:

$$s_d = \frac{V_{out}}{L}(A/s)$$

- Buck-boost is easy because there are no complex differences to calculate for v_L since one side of L is <u>always</u> grounded. v_L is either V_g or V_o.
- In contrast for buck and boost circuit topologies one finds for the voltage across L:

  $V_L \sim (V_g - V_o)$ and both relative magnitudes affect Δi slopes.

B.EXAMPLES OF BOOST DESIGN

Below we will go through the flow of a boost design- a flyback converter, which is a subset of the boost topology. The object is to see how much design you are already to do and how much you are not ready to do. Also it puts into better perspective the filter design as part of the whole design process. The input voltage of 18-36 volts is representative of the factor of 2 range of input voltage variation we must deal with. The

multiple outputs at set current levels at each load is also typical. Note in the figure below the single input and multiple output filters as well as the switch transistor Q_2 and its control circuits.

28 W PWM Flyback Converter

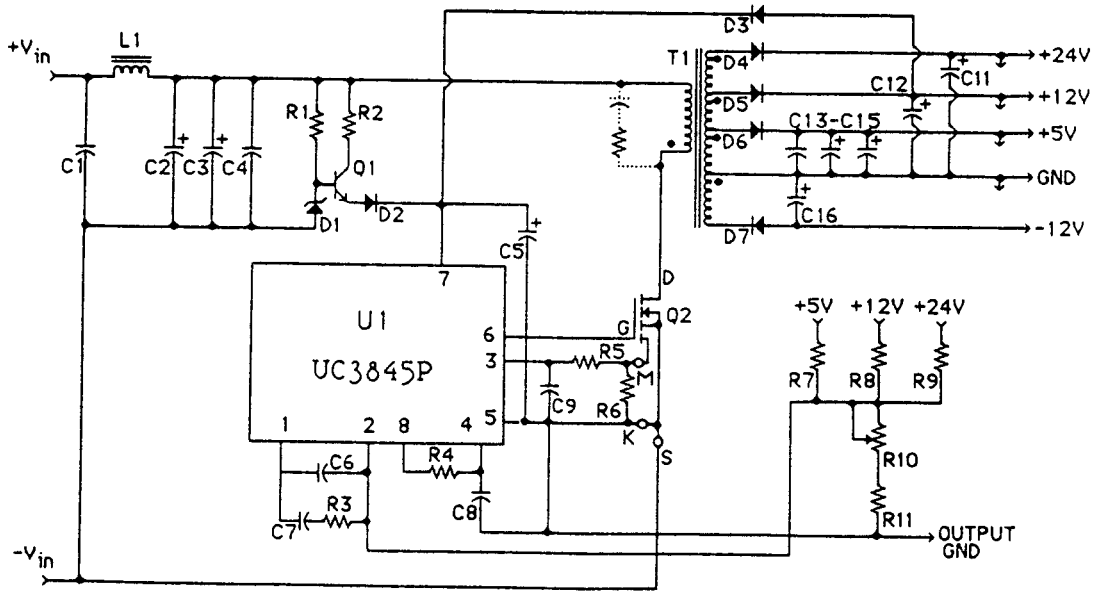
Application

This power supply is to provide power for a piece of process control instrumentation. The instrument receives its power from a +24 V bulk power supply that also provides transformer isolation from the bus voltage to the unit.

Specifications

V_{out}: +5 VDC at 2 A max current, 0.5 A min
+12 VDC at 0.5 A
−12 VDC at 0.5 A
+24 VDC at 0.25 A

V_{in}: 18–36 VDC required operational range
+24 VDC nominal input line voltage



Schematic for design example

Next we do a black-box overview that allows us to find required power, current and wire sizes.

$$P_{out} = (5\text{ V})(2\text{ A}) + (12\text{ V})(0.5\text{ A}) + (12\text{ V})(0.5\text{ A}) + (24\text{ V})(0.25\text{ A})$$
$$= 28\text{ W}.$$

$$P_{in} = P_{out}/\text{effic}_{(est)} = (28\text{ W})/0.75$$
$$= 37.3\text{ W}.$$

$$I_{in(high)} = P_{in}/V_{in(low)} = (37.3\text{ W})/18\text{ V}$$
$$= 2.07\text{ A}.$$

$$I_{in(op)} = P_{in}/V_{in(nom)} = (37.3\text{ W})/24\text{ V}$$
$$= 1.55\text{ A}.$$

This indicates that a #18 AWG wire or equivalent should be used on the primary winding of the transformer.

$$I_{pk} = 5.5P_{out}/V_{in(min)} = 5.5(28\text{ W})/18\text{ V}$$
$$= 8.55\text{ A}.$$

Let us select the frequency of operation of the power supply to be 40 kHz (or $T_{on(max)} = 12.5\ \mu\text{s}$).

$$L_{pri} = V_{in(min)}T_{on}/I_{pk} = (18\text{ V})(12.5\ \mu\text{s})/8.55\text{ A}$$
$$= 26.3\ \mu\text{H}.$$

We arbitrarily choose 40 KHz as the switch frequency to start the design process. This set L_{pri} for the case of lowest input voltage at the peak current for D=1/2.

Next we consider the output DC filter, but only consider the minimum required capacitor, C_{min}.

$$C_{min} = I(load) x dT_{min}/(f_{sw} x V_{ripple})$$

We assume a spec of 150mV for the ripple and for the time interval we assume the smallest time interval of about 0.3 T_{sw}. The rated load current is specified for each output. See next page.

The output-filter section

The values for the output filter capacitors are determined using

$$C_{out(min)} = \frac{I_{out(max)}(1 - \partial_{(min)})}{fV_{ripple(p\text{-}p)}}.$$

$$C_{out(+5\,V)} = 480\,\mu F \text{ at } 10\text{ V}.$$
$$(C_{14} \text{ and } C_{15})$$

Use two each 220 μF at 10 V tantalum capacitors in parallel to reduce height and to reduce the ESR.

$$C_{out(\pm 12\,V)} = 122\,\mu F \text{ at } 20\text{ V}.$$
$$(C_{12} \text{ and } C_{16})$$

Use 150 μF 35 V tantalum capacitor.

$$C_{out(+24\,V)} = 60\,\mu F \text{ at } 35\text{ V}.$$
$$(C_{11})$$

Use two each 47 μF at 35 V.

Note that in practice a high frequency C should be place in parallel with the larger electrolytic capacitors because the big electrolytic's cannot absorb high frequency currents. For this bypass C use a 0.05 ceramic capacitor.

Next we turn attention to the input filter section which is composed of:

- EMI filter
- Start-up current surge limiter
- Bulk Input filter capacitor which is usually aluminum electrolytic as it is rugged to peak surges

It is this filter capacitor to which we turn our attention. The less ripple desired on the input DC the larger the capacitor but this causes large surge currents on start-up. As a guide we state that ripple voltages of 0.5 to 2 Volts are tolerable. Capacitors with low ESR are assumed here so only the C contributes to ripple voltages. One can show that:

$$C_{in} = 2x\ P(\text{input average})/\ f_{sw} x\ (V_{ripple})^2$$

We will assume V_{ripple} is 1 Volt.

The input filter section
C_{in}:

$$C_{in} \cong \frac{2P_{out}}{f(V_{ripple(p\text{-}p)})}$$

$$C_{in} = 2(37.3\ \text{W})/[(40\,000\ \text{Hz})(1\ V_{p\text{-}p})]$$
$$= 186\ \mu\text{F}.$$

Place two each 100 μF, 50 V aluminum electrolytic capacitors *and* a 0.1 μF, 100 V ceramic in parallel.

Finally, in the circuit diagram of page 12 the controller chip provides:

- The settings to make our desired first choice for f_{sw} to be 40 KhZ
- Current mode control circuits we will cover later
- Driver circuits to turn on and off the switch transistor

The switch-mode controller

In attempting to select a controller IC one should make a list of the important features desired for the design. Also make a "nice but nonessential" list.

Essential	*"Nice—but"*
Low parts count	Undervoltage lockout
Current-mode control	Low I_{sense} threshold
MOSFET driver output (totem-pole)	50 percent duty cycle limiting
Single output driver	
Low cost	

After reviewing the list of popular controller ICs, the UC3845P appears to satisfy all the above requirements.

Referring to the data sheet in the Motorola "Linear and Interface Integrated Circuits" data book, the basic schematic implementation is given in the application figures. The designer need only determine the values for the timing resistor and capacitor, and the current-sense resistor. All of the other components are involved with the V_{cc} supply and the feedback compensation, which will be designed later. Looking at the "Timing Resistor vs. Oscillator Frequency" graph and wishing to operate the supply at a nominal 40 kHz, one determines values of

$$C_T = C_8 = 2000\,\text{pF}.$$
$$R_T = R_4 = 10\,\text{k}\Omega.$$

This value will no doubt need to be adjusted during the breadboard stage.