LECTURE 7
ILLUSTRATIVE PROBLEMS AND HOMEWORK HINTS FOR OUTPUT FILTER AC WAVEFORMS

I. ERICKSON PROBLEM 2.9

A. V_{L1} , i_{c1}, input filter vs. time
   V_{L2} , i_{C2} output filter vs.time

B. I (transistor) vs. TIME
   I (diode) vs. TIME

C. L_1, L_2 - volt-sec balance gives steady state voltages
   C_1 ,C_2 - charge balance gives steady state voltages

D. RIPPLE ON INPUT FILTER
   a. C_1 FOR ΔV_{C1} SPEC
   b. L_1 FOR ΔI_{L1} SPEC

II. HOMEWORK PROBLEM HINTS,ANSWER QUESTIONS AND CATCH-UP TOPICS LECTURE

OUTPUT AND INPUT AC WAVEFORMS CAUSED BY SWITCHING

I. ERICKSON Problem 2.9

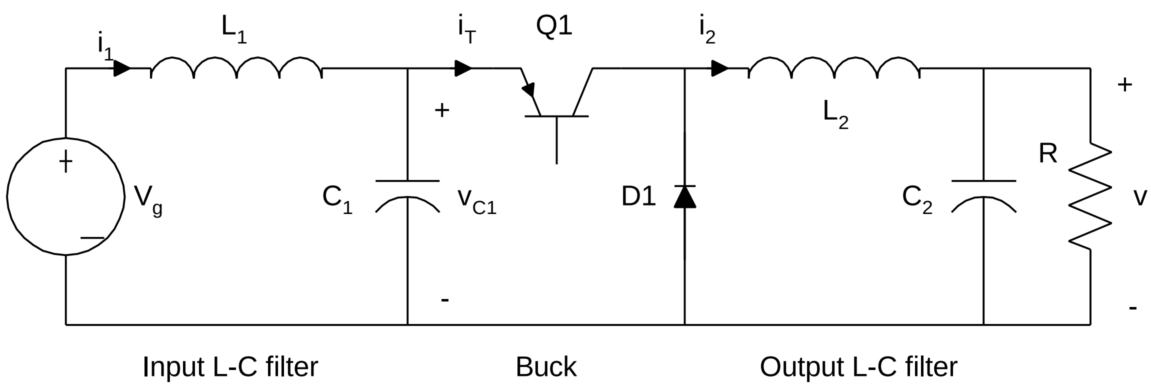


Fig. 2.32

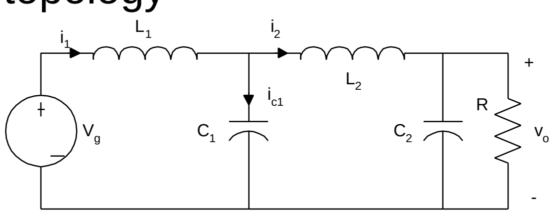
Q1 and D1 form a two position switch for the double pole double throw switch of the Buck topology.

For DT_S(SW on)

D1 is off

Q1 is on

Switch in position 1 circuit topology

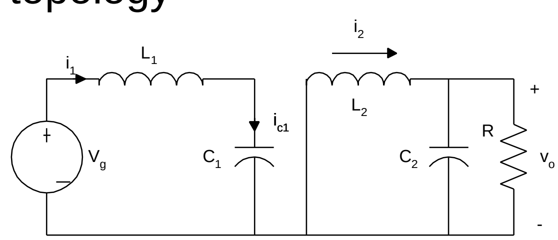


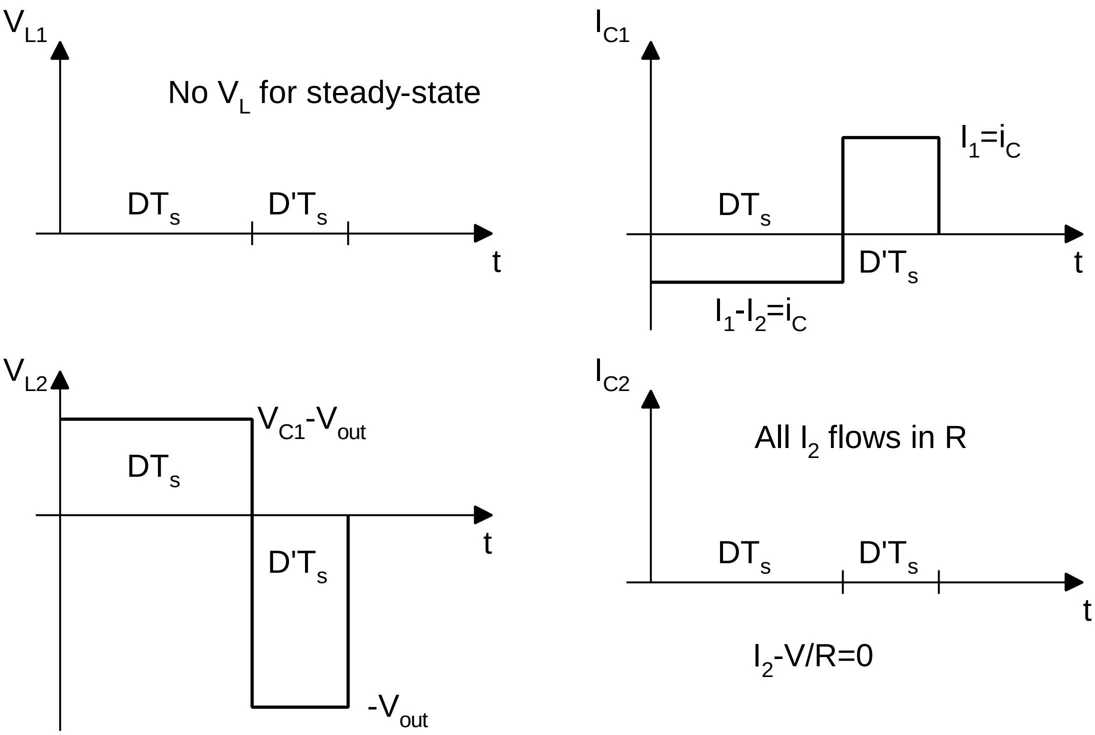
For $D'T_S$(SW off)

D1 is on

Q1 is off

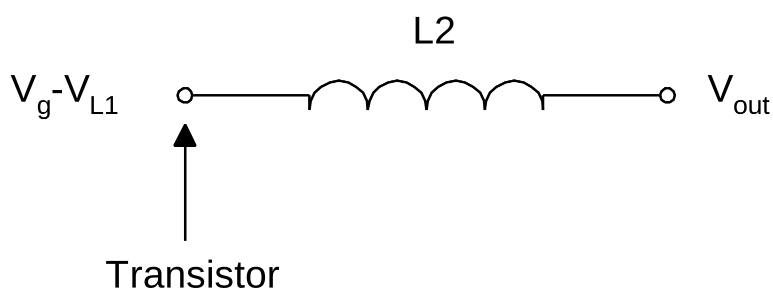
Switch in position 2 circuit topology





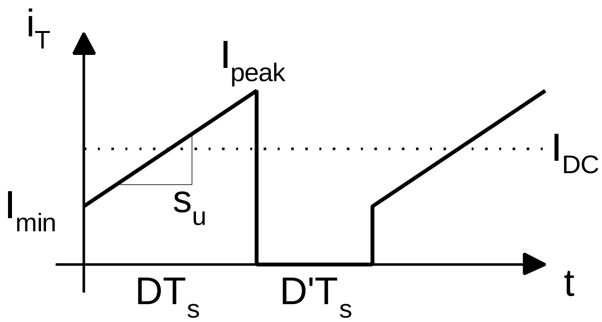
i_T WAVEFORM: V_{ON}(Transistor) $\equiv 0$
I_{out}(DC) = I_T(DC) During DT_S
Δi_{out}(ac) = Δi_T (ac) During DT_s

During DT_s interval transistor is on and assumed $V_{on} = 0$:



$$\Delta i_{L2} \equiv \frac{V_g - V_{L1} - V_{out}}{L_2} DT_S$$

During the $D'T_s$ interval the current is zero because the transistor is off and D1 is on.

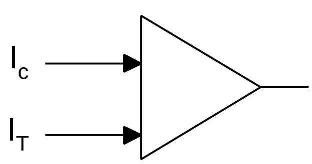


Δi_{L2} is symmetric about I_{DC}

s_u = SLOPE OF i_T RISE = $(V_g - V_{L1} - V_{out}) / L_2$
NOTICE $I_{peak} = I_{DC} + \Delta i_{L2}$
AGAIN IN "D" CONTROL SCHEME I_{peak} DEPENDS ON $I_{DC} + \Delta i_L$. IF Δi_L RIPPLE IS TOO BIG THEN I_{peak} RATINGS OF TRANSISTOR OR DIODE MAY BE EXCEEDED. SOLID STATE DEVICES ARE KILLED FOR i > i(critical) IN nsec.

ASIDE:

CHAPTER 11of Erickson shows a method for current control of a switched converter where the switch transistor current can never exceed a set current. We set the value of i(max) to be below the transistor maximum. at this point the transistor is switched off before it is destroyed.



$I_T > I_c \equiv I_{peak}$ Switch throws to turn off series transistor before $I_T > I_c \equiv I_{peak}$ for transistor

Now apply v-sec balance to all inductors and charge balance to all capacitors.

<u>L_1 VOLT-SEC BALANCE</u>: GIVES STEADY STATE CONDITION

$$D(V_g - V_{C1}) + D'(V_g - V_{C1}) = 0 \Rightarrow V_g = V_{C1} \text{ IN S.S.}$$

$\underline{L_2\text{ VOLT-SEC BALANCE}}$: GIVES f(D) EQUALS "D" FOR A BUCK

$$D(V_{C1}-V_{out}) + D'(-V_{out}) = 0 \Rightarrow V_{out} = DV_{C1} = DV_g$$
(Steady State Buck Converter)

$\underline{C_1\text{ CHARGE BALANCE}}$:

$D(I_1-I_L) + D'(I_1) = 0$

$I_1 = DI_2$

$I_2 = V_{out}/R = DV_g/R \Rightarrow I_1 = D^2(V_g)/R$, I_1 IN TERMS OF V_g

$\underline{C_2\text{ CHARGE BALANCE}}$:

$D(I_2-V_{out}/R) + D'(I_L-V_{out}/R) = 0$

$I_2 = V_{out}/R = DV_g/R$

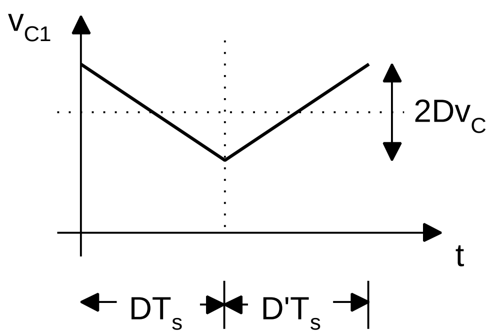
<u>SUMMARIZE STEADY STATE</u>:

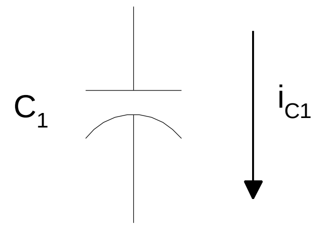
$V_{C1} = V_g$	$I_1 = D^2V_g/R$
$V_{C2} = V_{out} = DV_g$	$I_2 = DV_g/R$

Having all the steady state conditions gives us f(d) the dc transfer function and all operating effective dc values. we next look at ripple. to do so we use the simplified analysis.

CALCULATE RIPPLE VALUES FOR ALL FOUR REACTIVE ELEMENTS.

Δi_{L1} Δv_{C2}	Are two pole cases where ripple from drive not negligible. We must take ripple into account. **<u>Cannot</u>** use the small ripple approximation.
Δv_{C1} Δi_{L2}	Can use the small ripple approximation for these cases.





$s_D = i_{C1}/C$ (during DT_s) $= (I_1 - I_2)/C$
$s_U = i_{C1}/C$ (during $D'T_s$) $= I_1/C$

NOW IN STEADY STATE:

$I_1 = D^2V_g/R$, $I_2 = DV_g/R$ $\quad 2\Delta V_{C1} = (D^2V_g/R)(D'T_s/C_1)$

$2\Delta V_{C1} = s_U D'T_s$
$= I_1 D'T_s/C_1$

$$C_1(\text{to specify } \Delta v_{C1} \text{ ripple}) = \frac{V_g D^2 D'}{2R\Delta v_{C1}} T_S$$

<u>EXAMPLE</u>: BUCK CONVERTER

STEADY STATE SPECS:

$V_g = 48$, $V_o = 36$, $R = 4$, $V_o = DV_g$

$\Rightarrow D = 0.75$ and $D' = 0.25$

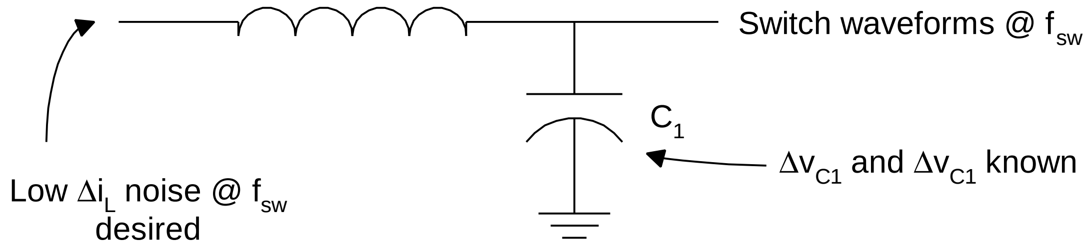
NOW WE HAVE THE INPUT FILTER WITH V_{C1}. LET'S SET $\Delta V_{C1} = 0.02V_{C1}$ (2%) AS OUR MAXIMUM ALLOWED.

$V_o^2/R = P_{out} = 324$ W.

WHAT'S C_1 VALUE WE NEED TO ACHIEVE 2% RIPPLE SPEC?

$$C_1 = \frac{V_g D^2 D'}{2R\Delta v_{C1}}$$

For $f_{sw} = 100$ kHz GIVES $C_1 = 5.86\mu f$
For $f_{sw} = 500$ kHz GIVES $C_1 = 1.17uF$



NEXT CALCULATE L_1 VALUES REQUIRED FOR A GIVEN Δi_{L1} SPECIFICATION

$$2\Delta i_{L1} = \frac{\int \Delta v_{C1} dt}{L}$$

$$dt = \frac{T_s}{2}$$

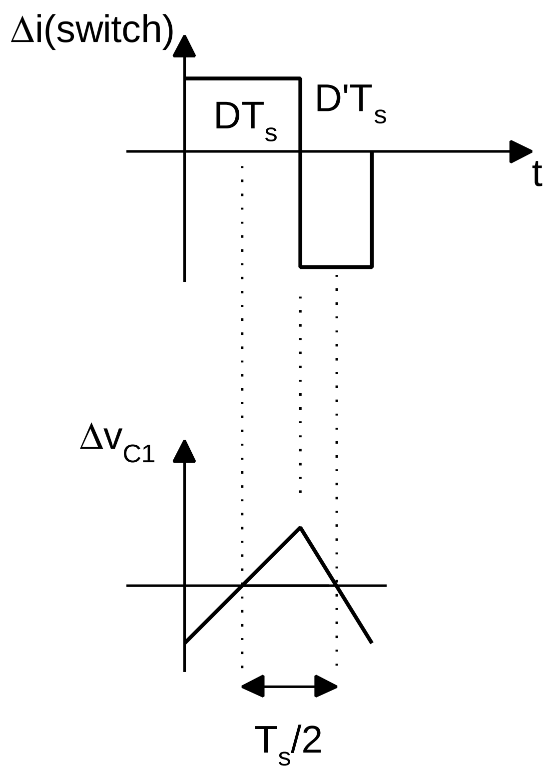
$$\int \Delta v_{C1} dt \equiv \frac{1}{2}\left(\frac{T_s}{2}\right)\Delta v_{C1}$$

$$\Delta i_{L2}(\text{due to } \Delta v_{C1}) = \frac{\Delta v_{C1} T_s}{8L_1}$$

$$\Delta v_{C1} = \frac{D^2 D' V_g}{2RC_1} T_s$$

$$\Delta i_{L1} = \frac{D^2 D' V_g}{16RL_1C_1} T_s^2$$

$$L_1 = \frac{D^2 D' V_g T_s^2}{16RC_1 \Delta i_{L1}}$$



IMAGINE Δi_{L1} IS ALL EMI AND WE WANT TO MINIMIZE IT. SO FOR A Δi_{L1} SPEC OF 20 mA ALLOWED INTO THE MAINS FROM THE SWITCHED NETWORK:

IF f_{sw} = 100 kHz, L_1 = 60 μH

IF f_{sw} = 500 kHz, L_1 = 12 μH

Finally HW#1 Due next week:

1. **Answer Questions asked throughout lectures 1-2.**
2. **Chapter 2 Problems 2, 3, 4 and 6.**

NOW SOME HINTS TO THE HW