LECTURE 6
ASSOCIATED OUTPUT AND INPUT FILTER AC WAVEFORMS CAUSED BY SWITCHING

I. **SELECTING INDUCTOR AND CAPACITOR VALUES TO MEET RIPPLE SPECIFICATIONS** FOR A GIVEN DUTY CYCLE - L(D) & C(D)

a. **L(D)** FOR SPECIFIED Δi_L ,GIVEN V_L DURING DT_S

$$L = \frac{V_L(\text{during} DT_s)}{2\Delta i_L} DT_s = L(D)$$

b. **C(D)** FOR SPECIFIED ΔV_c, GIVEN V_{out} DURING DT_S

$$C = \frac{V_{out}}{\Delta V}\frac{DT_s}{2R}, \quad \frac{V_{out}}{R} = I_{out} \text{ during } T_s \Rightarrow C=f(D)$$

II. DOUBLE POLE LOW PASS FILTERS

A. OUTPUT L-C FILTER $\mathbf{C^1 f(D)}$, $C \propto 1/f_s$

B. INPUT EMI FILTER, $\mathbf{L^1 f(D)}$, $L \propto 1/f_s$

STEADY STATE VOLTAGES C_1 ,C_2 - CHARGE BALANCE GIVES STEADY STATE VOLTAGES

D. RIPPLE ON INPUT FILTER

a. C_1 FOR ΔV_{C1} SPEC

b. L_1 FOR ΔI_{L1} SPEC

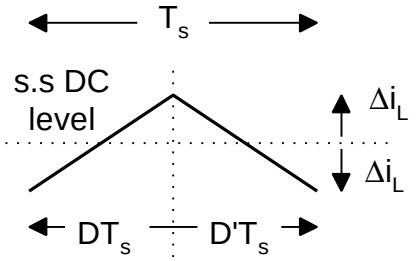
OUTPUT AND INPUT AC WAVEFORMS CAUSED BY SWITCHING

I. SELECTING L(D) AND C(D) IN DC FILTERS FOR PWM CONVERTERS

A.SELECTING REQUIRED L(D) IN AN L-R FILTER

On output filters for DC POWER will outline **two separate meth**ods to achieve SPECIFIED Δi_L LIMITS AND REQUIRED L VALUES AS WELL AS SPECIFIED Δv_C LIMITS AND REQUIRED C VALUES . Clearly $i_L$in a PWM circuit will ramp up and down around its DC level. Lets specify Δi_L limits and find how to select L values to achieve this.

DEFINING: The inductor current is $I_L(DC) + i_L(RIPPLE)$ and having ripple about I_{DC}(steady-state)



We find for both the buck and the boost:

$$\Delta i_L = \frac{V_{DC} - V_o}{2L} DT_s$$

Given in a practical case i_L = 10% of i_{dc}(steady-state) and the v_{dc} - v_o difference as known

L(FOR DESIRED Di_L) = $(V_{DC} - V_o)DT_S/2Di_l$ IS A LINEAR FUNCTION OF D. This is a minimum value of L. Note that L will increase when smaller ripple is required.

$\Rightarrow$USEFUL RELATION TO SELECT L(D) :NOTE THAT L = f(D)

EXAMPLE: For either a buck or a boost:
with: f_{SW} = 100 kHz = 10^5, T_S=10 μsec

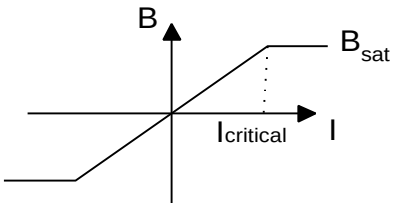
V_{DC} - V_o IS THE VALUE ACROSS "L" DURING "D" the on time of the power switch. Usually D does not exceed 0.9, and its value
IF V_{DC} - V_o = 50V, I_L = 10A & Δi_L = 10%I_L(DC) = 1A

$$L = L(f_{sw}, D, \text{CIRCUIT}) \Rightarrow L = \frac{50}{(2)(1)} D10^{-5} = 250\mu H * D$$

- The proper L value to meet the required ripple spec. is set in either the buck or the boost by required duty cycle, d. L(max) = 250μ H for D=1.
- D WILL BE SET BY: V_o / V_{DC} = f(D) AND f(D) IS UNIQUE TO EACH CONVERTER TOPOLOGY AS SHOWN BEFORE. In short, the required l will vary with d, and d will vary with converter type for specified v_{out} and v_{in}.

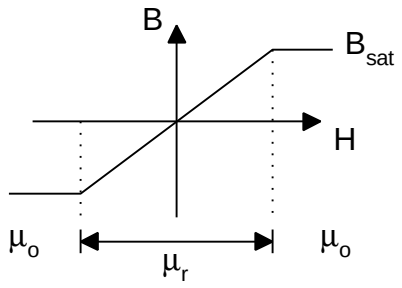
- OTHER L ISSUES: $L \neq f(I_L)$ $\Rightarrow$ only valid when $i_{dc} + i_{ac}$ is limited to below core saturation, i_{sat}.

THE I_{DC} LEVEL MUST BE FAR BELOW I_{SAT} OR Δi_L SWINGS WILL SATURATE THE CORE.



SATURATE CORE—
NOTE: SATURATION OCCURS IF i > i(critical) BE CAREFUL!

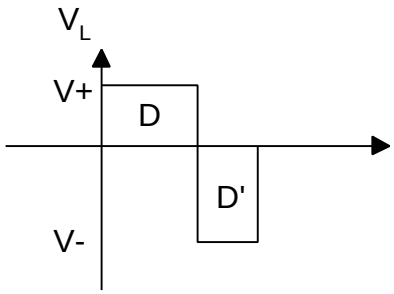
i > i(critical) implies H or I > H(critical) or I(critical) and μ_r changes to μ_o suddenly. Core saturation occurs for big current amplitudes if we are not careful. THIS CAUSES L TO DROP IN VALUE BY 100 OR MORE.



$$L \equiv \frac{m_r m_0 N^2}{R}$$

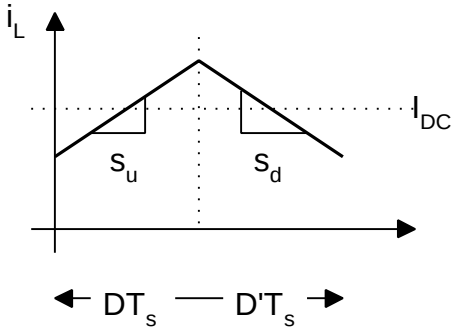
$\Rightarrow$ FOR LARGE μ_r(core)
L WILL BE LARGE

If **b** in inductor core exceeds B_{sat} the L value will decrease by 10-10^3 at B > B_{sat}. This means L(i) variation occurs in a threshold fashion, not gradually. Finally, for steady-state to occur over the full cycle of the switch waveform t_s THE NET $\int_0^{T_s} v_L dt \equiv 0$. THIS MUST OCCUR, OTHERWISE THE INDUCTOR CURRENT WILL GROW EACH CYCLE AND EVENTUALLY REACH SATURATION AND
i > i(critical).



For an inductor in steady-state and well below core saturation, the total integral area $v_L dt$ over T_s is ZERO.

GIVEN THAT IN STEADY-STATE THE INDUCTOR MUST HAVE VOLT-SEC BALANCE OVER T_s:



In many cases the di/dt upward slope (s_u) ≠ downward slope (s_d) in a/sec units. this means that we must choose d and d' so that the integral is indeed zero. That is volt-second balance sets d values to their proper values in steady state.

di/dt SLOPE IN THE INDUCTOR IS SET BY:

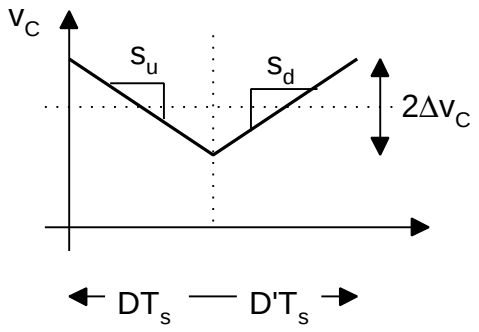
upward V_L/L during dt_s. v_L is the voltage across L during internal dt_s.

Downward V_L/L during $d't_s$. V_L is the voltage across L during interval $d't_s$ which is the switch off time..

V_L differs during dt_s and $d't_s$ because the converter circuit topology differs for dt_s (switch on) and $d't_s$ (switch off) as we will show in more detail below.

B. SELECTING C(D) IN A DC FILTER

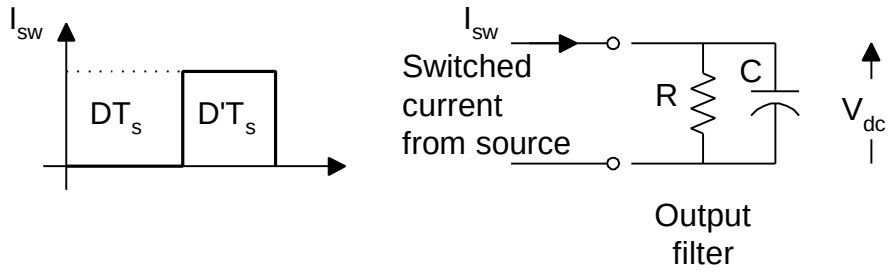
Likewise for capacitors we have "capacitor charge balance". in steady state for any capacitor, V_c is fixed after the switching period t_s and not growing or decreasing in steady state.. V_c has a dc baseline and an AC ripple.



Downward slope is set by I_C during DT_s when the switch is on and the circuit is the on case topology.
Upward slope is set by I_C during $D'T_s$ when the switch is off and the circuit is in the off case topology.

If $s_u \neq s_d$ then D ≠ D' for steady-state conditions to occur.

EXAMPLE: We did the single pole L-R filter now for a R-C filter we assume $v_o = v_{dc}$ was set by the converter f(d) and v_{in} $v_o = f(d)v_{in}$ so that d is known. CONSIDER FIRST A SINGLE POLE R-C LOW PASS FILTER driven by a current source. this could very well be the current from an inductor as we will show later.



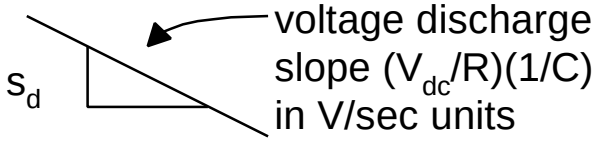
and in steady-state

$$Io \equiv \frac{V_{dc}}{R}$$

FOR A SPECIFIED Δv RIPPLE GOAL, THE VALUE OF C DEPENDS ON f_{sw}, D, V_{DC}, R

First consider an interruption of current with no source current for dt_s:

$i_{out} = v_{dc} / R$ is drained from C initially charged to $v_o = v_{dc}$.



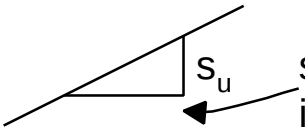
With source current switched back on for $d't_s$ we recharge the capacitor above:

$$\frac{I_{switch}}{C} - \left(\frac{V_{DC}}{R}\right)\frac{1}{C} \Leftarrow$$

assume net positive

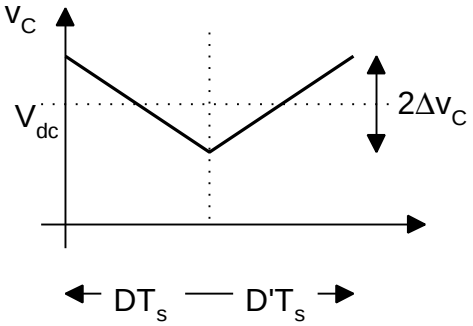
current to recharge C BACK TO $V_o = V_{DC}$

active current drive	load still drains current



slope $(I_{sw}-V_{dc}/R)(1/C)$ in units of V/sec

then the change in V_c is such that:



$$\Delta v_C \equiv \left(\frac{V_{DC}}{R}\right)\frac{DT_S}{2C}$$

GIVEN ΔV_C THIS SETS "C" VALUE C IS A LINEAR D

FUNCTION: $C \equiv \left(\frac{V_{DC}}{\Delta v}\right)\frac{DT_S}{2R}$ **= C(D)**

<u>EXAMPLE</u>: V_{DC} = 20 V, f_s = 100 KHz
ΔV OF 10% = 2 V, R = 4 Ω

$$C = \left(\frac{20}{2}\right)\frac{D10ms}{(2)(4)} = \frac{200}{16}\,mF*D$$

NOTE C IS A LINEAR FUNCTION OF ON-TIME DUTY CYCLE D

- Required value of "C(D)" for specified 10% ripple on v_{dc} depends on D (duty cycle)
- For a given v_{dc} output and v_{in} as well as converter type, D is set by the f(D) for a given converter type.
- v_{dc}/v_g = f(D) yields D to achieve that specific steady state.
- each converter topology has a unique f(d).

again $\int_0^{T_s} v_L dt = 0$. if not, v_c will increase until the dielectric breakdown of the capacitor is reached.

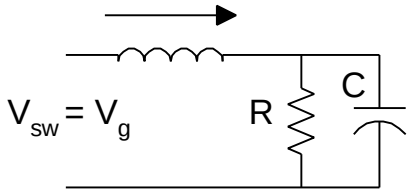
C. DOUBLE POLE L-C LOW PASS FILTERS

Here we are solving the case of a series L in-between input and output and parallel C across the load
At the output, you can calculate similiar current and voltage ripple waveforms for both a series L and a shunt C. Again we assume working converters set d and d' values and are only concerned with the output ripple specifications Δi(ac) and Δv(ac) and how they effect **the choice of L and C in output filters.** L is in series and C is in parallel.

THIS IS A UNIQUE SITUATION WHERE SMALL RIPPLE APPROXIMATION MUST BE USED TO GET CORRECT V vs. t. WE ARE ABLE TO USE THIS SIMPLE APPROXIMATION IF WE DO IT CAREFULLY.

1. First recognize that capacitor voltage ripple is affected by the Δi_L ripple in the series charging inductor:
   $I_L = I_L(dc) + \Delta i_L$ Ü **Δi_L was usually considered zero before for single pole filters**. Now however, Δi_L is <u>not</u> considered zero.

WE SHOW FOR THE CASE BELOW Δi_L EFFECTS Δv_C AND CANNOT BE NEGLECTED.



In fact in steady state at the output we can say to a good approximation:

- I_L(DC) **FLOWS ONLY INTO R** AS C DOESN'T ALLOW I_{DC}
- **Δi_L(ac) AT f_{sw} FLOWS MOSTLY INTO C** AND NOT R IF $Z_C(f_{sw}) << R$. THEN WE CAN SIMPLIFY FILTER ANALYSIS SO THAT Δi_L FLOWS ONLY INTO C. This is often the case in practice.
- **Δi_L º Δi_C Ü ALL "L" RIPPLE Di FLOWS INTO "C"**

So the time analysis sequence of voltage across the series inductor is:

1. $v_{sw} = v_g$ comes on as a step: constant voltage is applied during dt_s to the left side of "L". The right side of L is considered fixed at v_{out}. $V_L = v_{out}(sw) - v_{out}(dc)$ or $v_L = v_g - v_o$

2. i_L appears as a **linear ramp** during dt_s

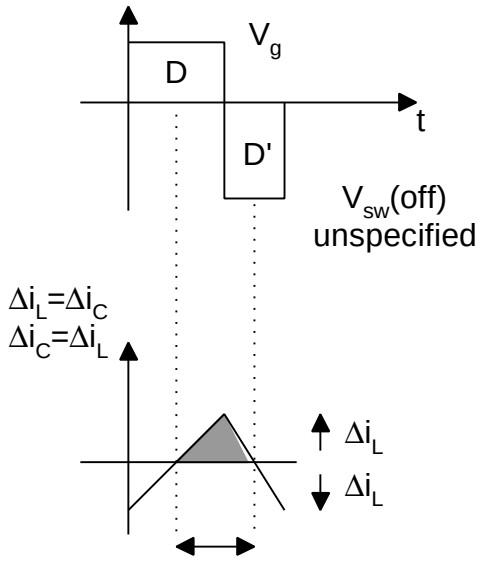
$$\Delta i_L = \frac{v_L}{L} dt \text{ or } i \sim at$$

3. This current flows mostly into C causing v_c to change given $i_c = at$ is a linear function of time (ramp) then $v_c \sim at^2$ during dt_s

$$v_C = \int \frac{i_C}{C} dt$$

WE WILL AVOID THIS COMPLEX ANALYSIS AS FOLLOWS. Consider the v_L waveform as a unisymmetric square wave. then from v_L being a square wave Δi_L will be a ramp -
Δi_L is a linear function of time(at). The area under the i-t ramp is the charge to be dumped on the capacitor.

We will find that the "C" VALUE TO MEET REQUIRED RIPPLE DEPENDS ONLY ON f_{sw} **AND NOT ON D.**



interval $T_s/2$ by symmetry

Assuming v_o varies little, this is the voltage waveform across the inductor v_L for:
v_{sw}(on) (DT_s circuit): $V_L=V_g-V_o$
v_{sw}(off) ($D'T_s$ circuit):
V_L unspecified
This voltage variation across V_L causes a Δi_L flowing through L about I_{DC}
Shaded area under the Δi_L vs t curve shown is positive Q_C during $T_s/2$. This will cause a Δv_C.

THE NET CHARGE
Q(DURING $T_s/2$) = ½*BASE($T_s/2$)*HEIGHT(Δi_L).
This charge change causes $2\Delta v_c$ to vary across the capacitor in the double pole L-C filter.

$$2\Delta V_C = \frac{Q}{C} = \frac{\frac{1}{2}\frac{T_S}{2}\Delta i_L}{C}$$

$$\Delta V_C(\text{Ripple on double pole series L / parallel C output filter}) = \frac{\Delta i_L T_s}{8C}$$

GIVEN Δi_L AND Δv_C AS SPECIFIED BY THE DESIGN OF THE OUTPUT SPEC'S WE CAN WRITE A SIMPLE EXPRESSION FOR C,

$$C \equiv \frac{\Delta i_L}{\Delta v_C}\left(\frac{T_S}{8}\right) = f(f_S) \text{ is the relation to determine C}$$

GIVEN THE REQUIRED Δi_L AND Δv_c RIPPLE VALUES.

NOTE THAT UNLIKE THE PRIOR SIMPLE L-R ANC R-C FILTERS IN L-C DOUBLE POLE FILTERS C ≠ f(D), ONLY f_s, Δi_L AND Δv_C

2. INDUCTOR AFFECTED BY DV_c

Previously we had a series L and parallel C between the switched converter pulsed output and the load. A filter could also be placed between the input to the converter and the mains to reduce emi from entering the ac mains from the switching waveforms at the inverter input. There are now laws concerning emi allowed on mains.

a. EMI and EMC ISSUES

- EMI is typically broken up into 2 primary categories
  - Conducted
    - Undesired signals conducted on interconnecting conductors
  - Radiated
    - Undesired signals traveling through free space
- Each of the two primary categories are further segmented into 2 sub-categories
  - Susceptibility
  - Emissions

Electromagnetic Compatibility (EMC) can be defined as the ability to operate in the intended electromagnetic environment, without introducing disturbances into that environment that are intolerable to other equipment.

Electromagnetic Interference (EMI) can be defined as the degradation in the operational performance of a system or device caused by an electrical disturbance.

In Europe the EU regulation of allowable harmonic pollution of the ac mains is strictly enforced for all switch

mode power supplies. See later lectures for more details. Never the less, a simple parallel C - series L input filter can do wonders for reducing signals at f(switch) from entering the mains.

Why a Filter is required

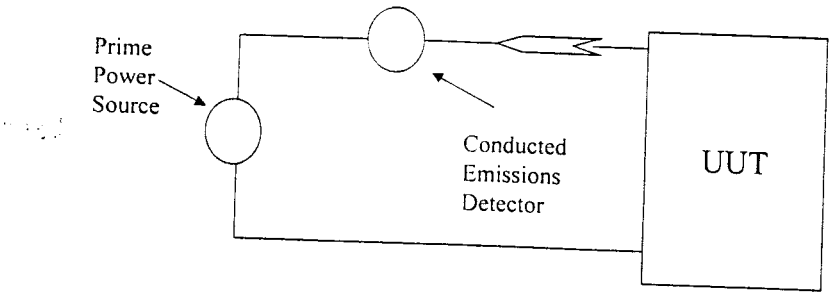
- Power supply operation includes nonlinear processes such as rectification and switching.
- Any nonlinear process generates frequencies other than the source frequency (i.e. harmonic interference).
- The interfering input current frequencies in conjunction with the finite source impedance of the voltage source produce noise and distortion in the voltage source itself.
- An input filter is required to prevent malfunction of equipment connected to a common power bus and to ensure system compatibility.
- Compliance to standards is required in many countries.
  - The general EMC requirements in the U.S. are set by the FCC, while the Food and Drug Administration (FDA) regulate medical equipment
  - Airborne equipment typically comes under DO-160 or MIL-STD-461
- Noise on the power lines may pass through the power supply and interfere with circuitry elsewhere in the product

On the next page we will illustrate both conducted and radiated emissions. Both arise from the switches operating at high frequency and carrying large switch powers.

THIS IS THE **DIRTY SECRET DISADVANTAGE** of the PWM APPROACH

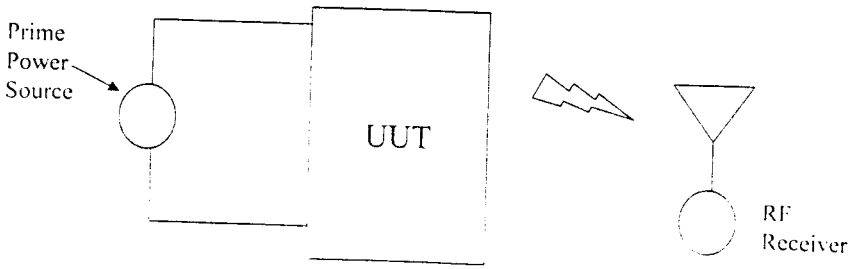
Conducted Emissions

- Conducted power line emissions can become a radiated emissions problem. Test Conducted before Radiated.



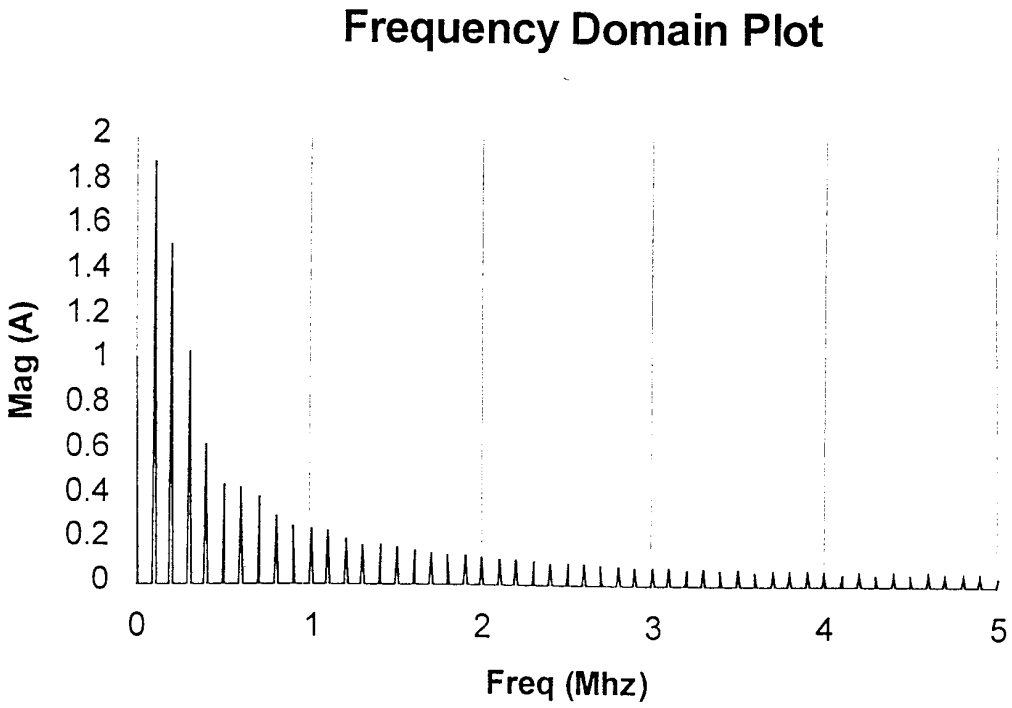
Radiated Emissions

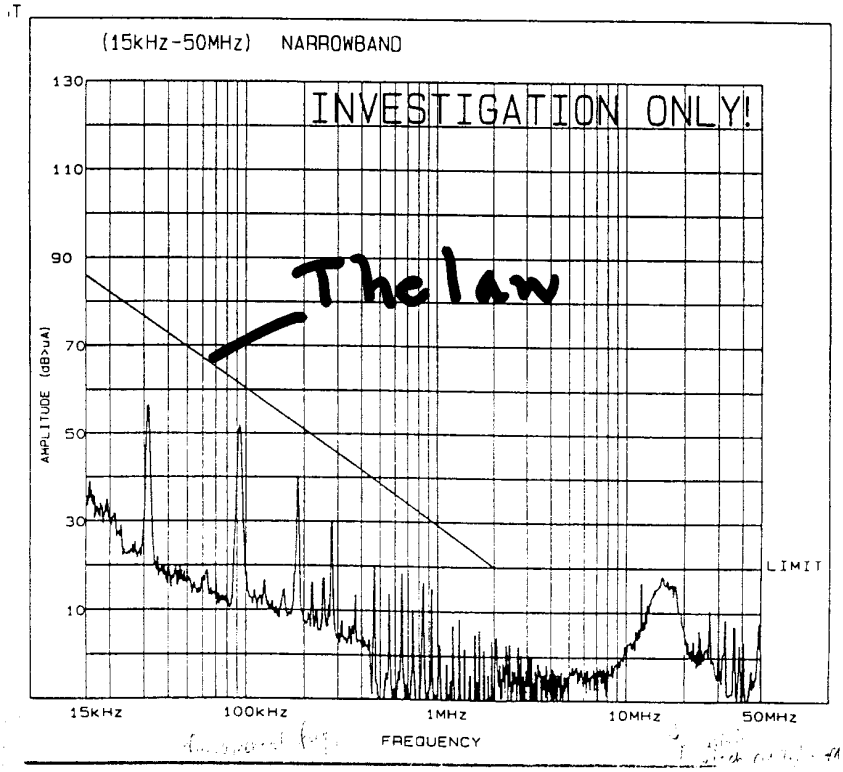
- Radiated Emissions are very hard to predict
- Typically an enclosure issue

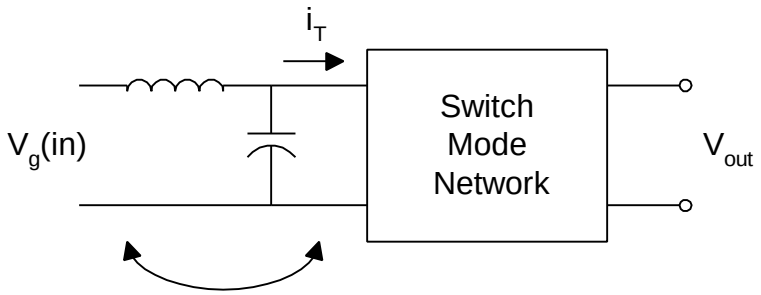


To bring this all to a head we place on the next page some data from the noise generated by a PWM Flyback converter. The noise spectrum is shown as a FFT. Finally, the total EMI signal is compared to that allowed by the law. We repeat that electrical engineers that do not design to regulatory specs are IN VIOLATIOL OF THE LAW.

FFT of a 30W, 100Khz DCCM Flyback

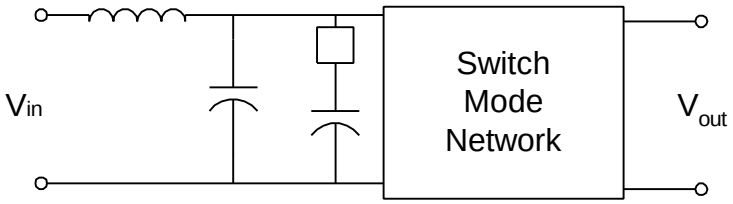




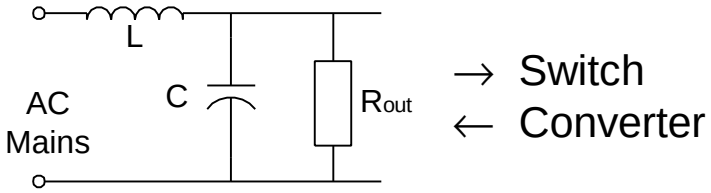


Input filter to keep switching harmonics from entering the mains: EMI noise issue is now a legal one.

Incidentally, some switching signals have very sharp transients that can be better reduced by an RC snubber circuit in addition to the EMI filter as shown:



A simplified equivalent circuit model is given below:



Previously, we saw that for an equal duration square wave (d = d') the **fundamental ac component** of the signal has an amplitude $2v_{dc}/\pi$. We will consider the attenuation of the filter in two ways on the next page:

- A rough transfer function approach
- An intuitive ripple estimate approach

$$V_{out} = V_{in} \frac{\left(\frac{\frac{1}{jwC} \cdot R}{\frac{1}{jwC} + R} \right)}{\left(\frac{jwL + \frac{1}{jwC} \cdot R}{\frac{1}{jwC} + R} \right)}$$

Where $V_{in} = \frac{2}{p} V_{DC} \sin wt$ (for D = 0.5)

Assume a 40db per decade rolloff due to the L-C. If we specify the need for 24db of attenuation at the switch frequency, then the corner frequency of the filter will be at:

$F_C = f_{sw} \times 10^{(24/40)} = 25KHz$

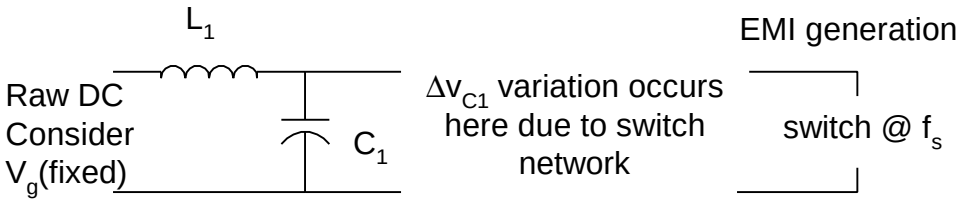
For a 50 Ohm input line impedance and a filter damping factor of .707 the required Land C are given by:

$L = 50 \times 0.707/\pi \times 25KHz = 450\ \mu H$

$C = 1/(2\pi f_C)^2 L = 0.9\ \mu F$

Real commercially available capacitors do not exceed .o5m so, we need to reduce C by 2 and increase L by 2.

THIS IS ONE WAY. WE ALSO GET A ROUGH IDEA AS FOLLOWS:



Δv_{c1} variation at the inverter input causes Δi_{L1} to flow back to the mains. We have a spec. on the maximum Δi_{L1} from the government. Consider v_g for now as fixed instead of a rectified sinusoid. $V_L = v_g(\text{fixed}) - v_{c1} = \Delta v_c$.

Now any change in Δv_c will cause a change in Δi_L.

$$2\Delta i_L 1 = \frac{\int \Delta v_c dt}{L_1}$$

THE TIME PERIOD dt IS $T_s/2$ AGAIN BY SYMMETRY, AND VOLT-sec AREA UNDER $\int \Delta v dt \equiv \frac{1}{2}\Delta v_c \frac{T_s}{2}$

Δi_{L1}(Ripple current due to Δv) $= \frac{\Delta v_C T_S}{8L_1}$. IF WE SPECIFY BOTH Δv_c (known or measured) AND Δi_L, WE CAN WRITE THE L VALUE EQUATIONS AS:

$$L_1\left(\begin{array}{l}\text{value to reduce } \Delta i_{L1} \\ \text{to gov. specification}\end{array}\right) \equiv \frac{\Delta v_C}{\Delta i_{L1}}\frac{T_s}{8}$$

given Δv_c

FOR THE DOUBLE POLE FILTER INCLUDING RIPPLE:

$L_1 \neq f(D)$, $L_1 \propto 1/f_s$

Finally, For HW#1:

1. Answer Questions asked throughout lectures 1-7.
2. Chapter 2 of ERICKSON Problems 2, 3, 4 and 6.