LECTURE 5

PULSE-WIDTH MODULATED CONVERTERS AND ASSOCIATED AC WAVEFORMS

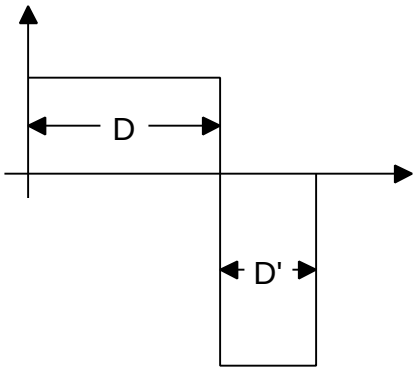
A. **REVIEW** of unregulated ac mains to dc converters: v_{out} control via duty cycle on time "D"; $v_{out} = v_{dc}(in)*f(D)$

   1. DC TRANSFER FUNCTIONS f(D), where D = duty cycle on time, for buck, boost and buck-boost converters

B. TYPICAL VOLTAGE AND CURRENT WAVEFORMS IN SIMPLE L-C OUTPUT FILTERS

   1. **INDUCTORS**: v_L (step) and i_L (ramp) waveforms
   2. **CAPACITORS:** i_c (step) and v_c (ramp) waveforms

   3. Unsymmetric i_l and v_c waveforms of equal integrated area



L: Volt-sec balance

C: Charge Balance

$D[V_{on}, I_{on}] + D'[V_{off}, I_{off}] \equiv 0$

FOR STEADY STATE CONDITIONS

REVIEW OF PULSE-WIDTH MODULATED CONVERTERS AND ASSOCIATED AC WAVEFORMS CAUSED BY SWITCHING

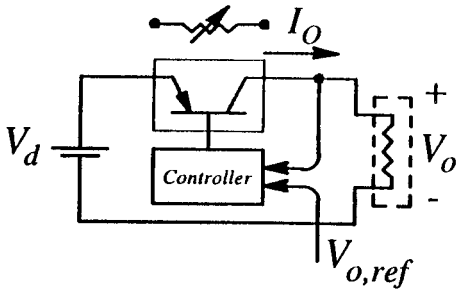
A. UNREGULATED AC MAINS TO DC CONVERTERS:

Linear Electronics Vs Power Electronics

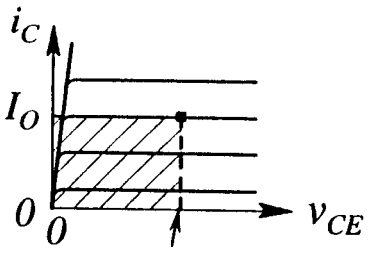
❑ Linear Electronics : Example

V_d : $20Vdc \pm 10\%$

V_o : $12Vdc$ (regulated)



$P_{loss} = V_{CE}\ I_O$



$V_{CE} = V_d - V_o$

❑ Poor efficiency

➳ cost of wasted energy

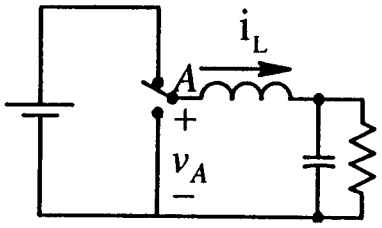
➳ large heatsink

1. Key issues in power electronics are:
   - Energy Efficiency
   - Size/Weight
   - Reliability and Tendency to Instability
   - Cost

On the next page we compare the full on/full off methodology of switch mode methods to supply power more efficiently and the simple trick to achieve bigger efficiency.

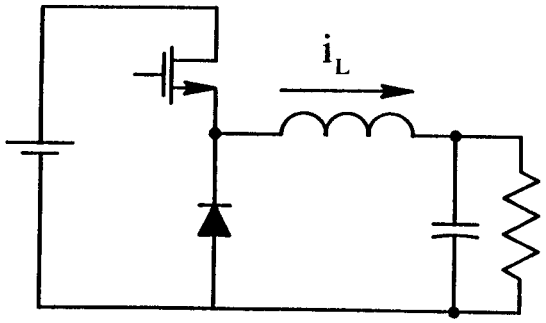
Bipositional Switch Implementation

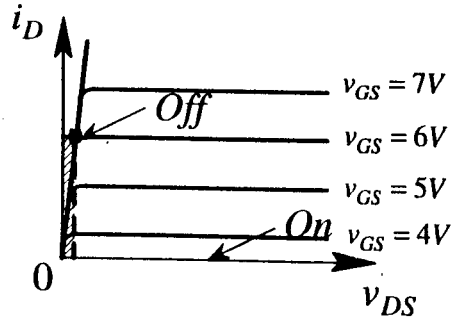
$(i_L > 0)$



$$q(t) = 0$$
$$= 1$$
$$v_A(t) = q(t)V_d = V_d$$
$$= 0$$

- Transistor operates as a switch
  - fully ON (or)
  - fully OFF





2. DC Transfer Functions in Terms of pulsed Duty Cycle

We reduced all the complexity of the switch mode power source by considering only the DC response in steady state and found to a first approximation that:

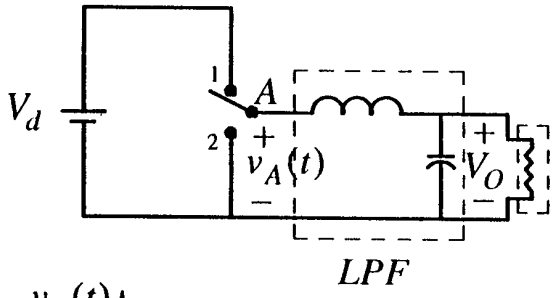
$$\frac{V_{out}}{V_{DC}(in)} = f(D)$$

Last time we gave intuitive arguments and dc transfer functions versus on time duty cycle for v_{out}/v_{in} = f(duty cycle) for three illustrative circuits, where D is the fractional on-time during the switching cycle.

In reality the transfer function will depend on more factors than just DUTY CYCLE-that comes later. But clearly

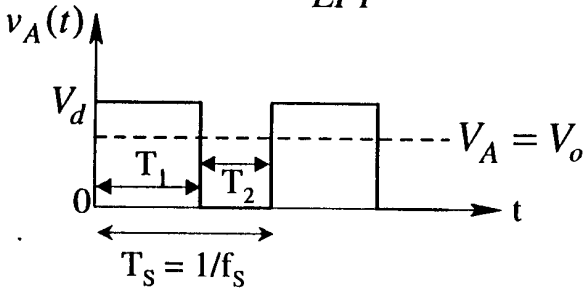
the high frequency switched mode has advantages as summarized below.

Power Electronics



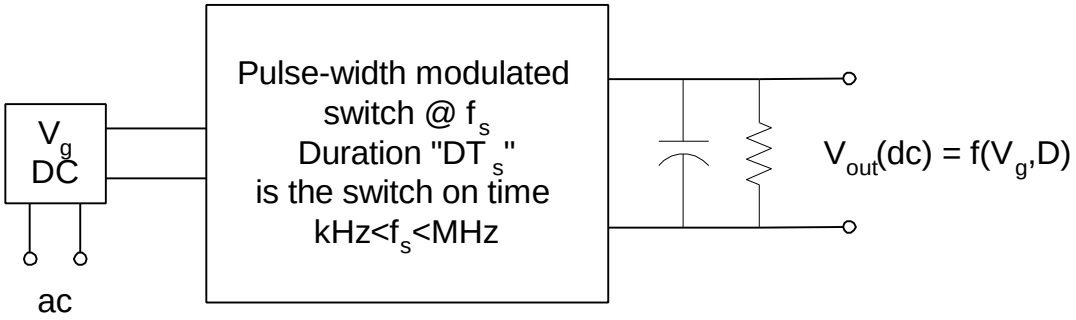
$v_A(t) = V_d$ *with switch in position 1*

$= 0$ *with switch in position 2*



$$V_A = \left(\frac{T_1}{T_S}\right) V_d$$

- *ripple in $v_A(t)$ filtered out by the low – pass filter* $\left[f_{c,filter} << f_s\right]$
- $f_S \uparrow \Rightarrow L\downarrow\ C\downarrow \Rightarrow$ *small size*
- *high energy efficiency*



The switched square wave output has two major components: Large signal DC and small signal ac.

$$V_{out} = V_{dc}(\text{average}) + V_{AC}(\text{ripple}) = V_g f(D)$$

Large Small@f_s

For an equal on/off square wave, D=D'=½, we can show by Fourier analysis that: V_{dc}(average) = V(peak)D.

$V_{AC} = \sum a_n Sin\left(\frac{np}{2}\right)$ and $a_n = \frac{2V(peak)}{np}$

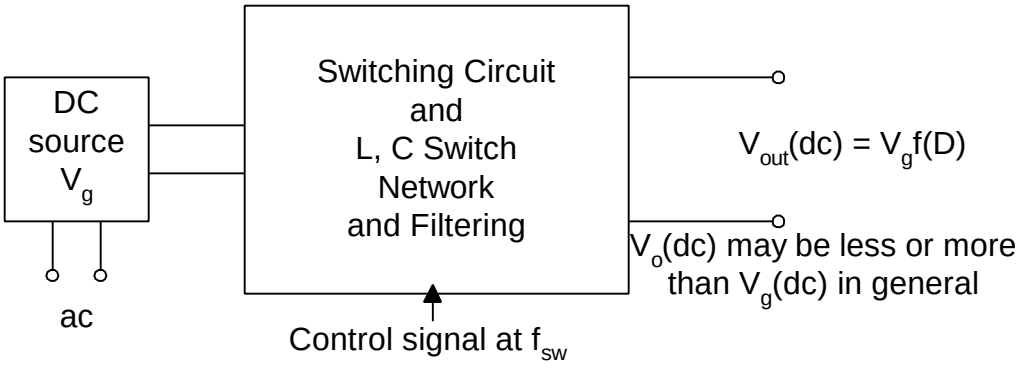
Fourier Components drop-off as 1/n. Fundamental component has $\frac{2V(peak)}{p}$ value.

When we employ a series inductor in the output (not shown) V_{AC} peak to peak at the output is usually reduced to ≤ 10% of the dc V_{out} provided the inductor is big enough.As the switch f_{sw} varies from kHz up to MHz we can use smaller inductors to achieve the same level of ripple.

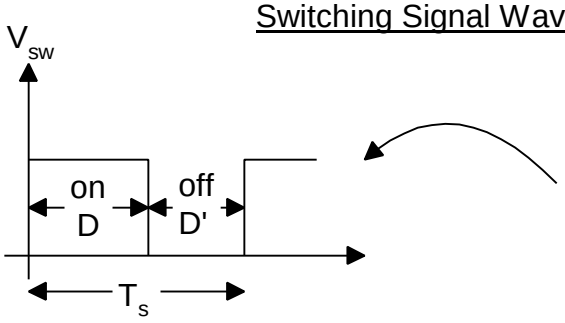
f_{sw} is usually limited to MHz & below because:

- Fast solid state switches at high v and i are still limited to MHz values at high power levels
- magnetic materials don't work well above MHz. Magnetic core losses increase dramatically above 1 MHz due to hysterisis and eddy currents. SEE LATER LECTURES FOR DETAILS.

To reduce the ripple component at f_{sw} we add passive simple R-C or even L-C filters after the switch and before the load with L in series to limit kvl violations and C across the output to reduce ac variations. This double L-C action allows us to reduce the ac ripple on the dc output to designated levels. similar filters are put at the input to prevent switched waveforms from polluting the mains. There are now laws for allowable NOISE YOU CAN CONDUCT ONTO THE AC MAINS that originate in the switch-mode power supply. WE WILL ANALYZE BOTH CASES SEPERATELY LATER. In this lecture we focus only on output DC filters as a first case.

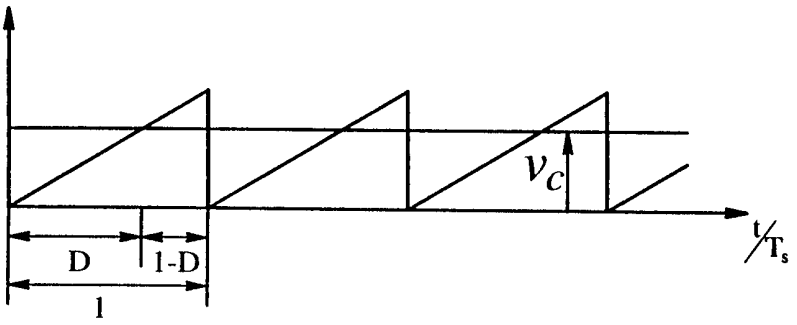


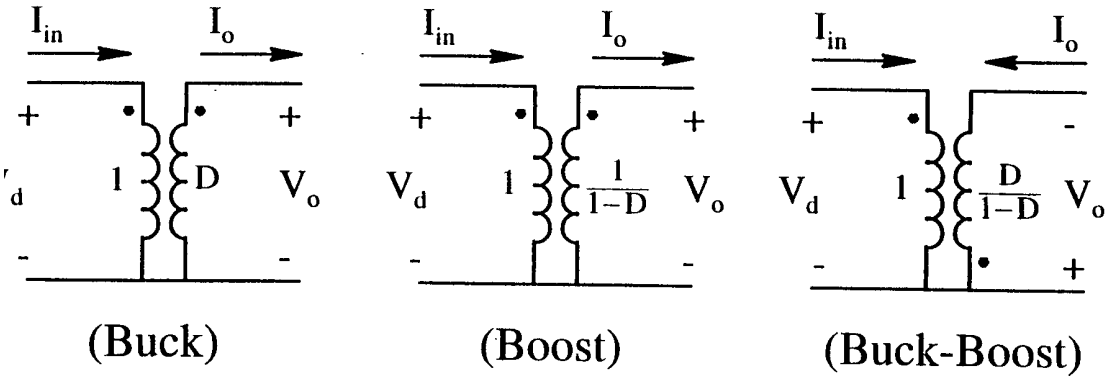
Switching Signal Waveform



Switching
D+D'=1
We actively control
"D", the on time, via
control circuits to vary
$V_{out}(dc)$ to desired
level

Review of Steady state operation (open loop)





TODAYS LECTURE will focus first on the output load where we have a specified v_{dc}(output) and further specify allowable v_{ac} and i_{ac} at the load. This sets the values of the filter components L and C.

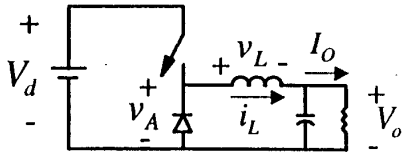
SUPRISE Both L and C required in switched mode designs will vary with d the on time duty cycle employed as well as with f_{sw}. The duty cycle will depend on:

- The chosen topology and the desired output voltage
- The given input voltage

That is D is set by the f(D) functions once topology and output levels are chosen for the given input. Before we can understand filters whose components will vary with D, simple i_L and v_c waveforms will be analyzed.

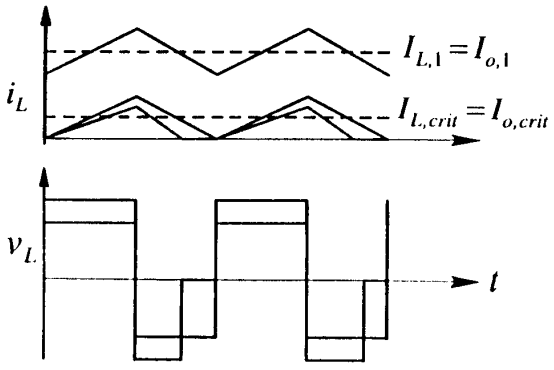
NOTE WELL: The f(D) functions in steady state assume that we are working in the continuous conduction mode. In fact this is not always the case as shown below.

Discontinuous conduction mode



$$D = \frac{T_1}{T_s} \mapsto \text{constant}$$

R changing



- for $I_o < I_{o,crit}$, i_L becomes discontinuous
- $v_L = 0$ while $i_L = 0$
- as shown by the waveforms V_o rises (average $v_L = 0$)

Discontinuous conduction has its own transfer function.

B. TYPICAL VOLTAGE AND CURRENT WAVEFORMS IN SIMPLE L-C PASSIVE FILTERS

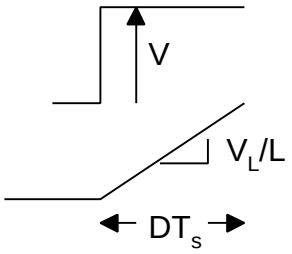
Throughout this lecture we assume a given converter type exists which for v_{in} and v_{out} sets unique values of d and d'. we only ask what are the required L(D) and C(D) values in the load filter given the allowed ripple. That is we specify allowed i_{ac} and find L(D) or specify allowed v_{ac} and specify C(D).

1. **INDUCTORS**: i_L WAVEFORMS VS t

IN CASE v_L IS A STEP $\rightarrow i_L = \frac{1}{L}\int v_L dt$

$\rightarrow$ SIMPLE INTEGRAL RELATIONSHIP

IF V_L IS A STEP DURING DT_S
THEN I_L IS A RAMP DURING DT_S



SLOPE OF RAMP IS V_L/L , WITH UNITS OF (A/sec)

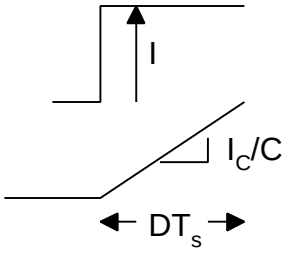
We assume L(D) is fixed and not varying with current I(i). due to core effects L(D) will in fact vary with i, having sudden changes in L(D) occuring usually when a magnetic core saturates. L(D) goes from a large value below saturation to a small value after saturation when i exceeds i(critical). This may make the kvl violations occur in switching.

2. **CAPACITORS**: V_C WAVEFORMS VS t

IN CASE i_C IS A STEP $\rightarrow v_C = \frac{1}{C}\int i_C dt$

$\rightarrow$ SIMPLE INTEGRAL RELATIONSHIP

<u>IF</u> I_C IS A STEP DURING DT_S
<u>THEN</u> V_C IS A RAMP DURING DT_S



Slope of ramp is i_c/c with units of (v/sec)

Note for both i and v to reach steady state after a full period of t_s the following integral relationships must hold:

L: $\int_0^{T_s} v_L dt = 0$

C: $\int_0^{T_s} i_C dt = 0$

For achieving steady-state during the $D'T_s$ interval, we must return to DC levels that started DT_s period. This means the net area under the v_L and i_C curves must cancel. For the L case this is termed "*volt-sec balance*" and for the C case it is termed "*charge balance*."

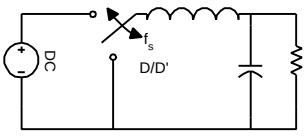
Note as dt decreases when f_{sw} increases the balance is closer to zero in magnitude for fixed v_L and i_C values.

3. DC TRANSFER FUNCTIONS f(D) FOR BUCK, BOOST, AND BUCK-BOOST

Below we again summarize v_{out}/v_{in} = f(d) relations for three basic converters that we will derive later. We will do this repeatedly to allow v_{out}/v_{in} = f(d) to be better understood when we are doing L(D), C(D) and L(D)-C(D) filtering design calculations. Note component choice depends on D values.

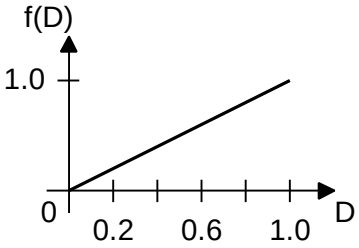
We state again that the inductor or capacitor required to achieve a specified level of ripple on the output of a PWM converted will depend on the operating range of D. Design will have to account for worst case situations, as we will show in detail in Lecture 7

SIMPLE SWITCH MODE CONVERTERS



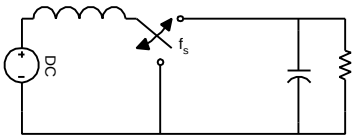
BUCK

The buck is limited in that $V_{out} < V_{in}$ only



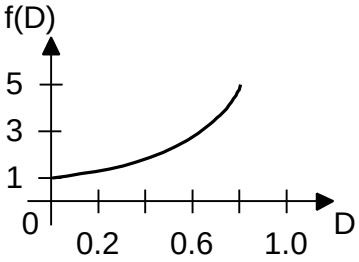
$V_L=V_o$ or $V_{DC}-V_o$

- f(D)=D
- Never get negative output
- $V_o(min) = 0$



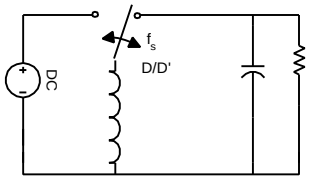
BOOST

The boost is limited in that $V_{out} > V_{in}$ only



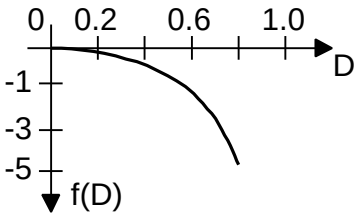
- f(D)=1/(1-D)
- Never get zero output: $V_o(min) \neq 0$

$V_L=V_{DC}-V_o$ or V_o



BUCK-BOOST

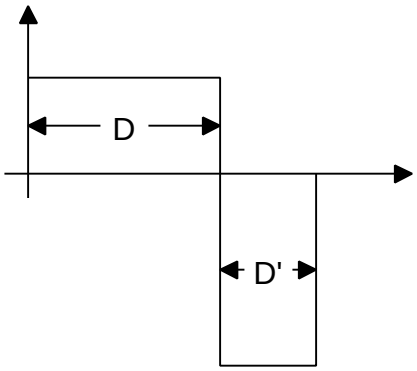
The buck-boost is limited to negative voltages



- f(D)=-D/(1-D)
- Inverting output w.r.t. V_g

$V_L = V_o = -V_{DC}$ for D = ½

4. UNSYMMETRIC i_L AND v_C WAVEFORMS OF EQUAL INTEGRATED AREA IN THE ABOVE THREE CONVERTERS



L: Volt-sec balance
so $i_L \neq \infty$
C: Charge Balance
so $v_c \neq \infty$

SINCE IN STEADY STATE:
V_{DC} AND V_{out} ARE BOTH MOSTLY DC BUT $V_{DC} \neq V_{out}$
During switching pulsed dc steps are applied to the inductor

V_{DC} —ᔓᔓᔓ— V_o

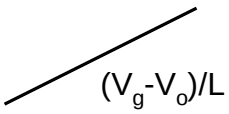
Notice for above three circuits v_L is across the inductor and is unique during the d cycle. It will be either of two possibilities:

$+V_{DC} - V_{out}$ FOR BOTH THE BUCK AND BOOST OR $-V_{DC}$ ONLY FOR BUCK-BOOST AS ON SIDE OF THE INDUCTOR IS AT GROUND. In practice v_{dc} and v_{out} are primarily crudely rectified AC which looks like dc levels to a first approximation.

THUS DURING DT_s INTERVAL WE CAN FIND $i_L(t)$:

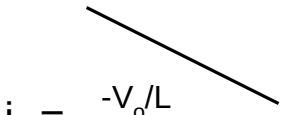
$i_L = \frac{1}{L}\int v_L dt$ where $V_L = V_g - V_{out}$ during DT_s (buck, boost)

$V_L = -V_{DC}$ during $D'T_s$ (buck-boost)

$i_L =$ 

<u>Upward</u> i_L ramp for buck and boost with <u>fixed</u> $(V_g - V_o)$ during D cycle

Note also the polarity of V_{out} for buck-boost can be negative during the $D'T_s$ cycle, so we get down ramp.



Downward i_L ramp for buck-boost for fixed V_o during d cycle.

During the D' cycle i_L ramps up.

Finally, For HW#1 Due in 1 week:

1. Answer Questions asked throughout lectures 1-7.

3. Chapter 2 Erickson Problems 2, 3, 4 and 6.

HOMEWORK is 60 percent of the course grade.

Midterm is 20 percent and the term paper is 20 percent. The paper is due AFTER Thanksgiving break.