LECTURE 4

Introduction to Power Electronics Circuit Topologies: The Big Three

I. POWER ELECTRONICS CIRCUIT TOPOLOGIES

A. OVERVIEW

B. BUCK TOPOLOGY

C. BOOST CIRCUIT

D. BUCK - BOOST TOPOLOGY

E. COMPARISION OF THE BIG THREE

II. TOPOLOGY OF L-C OUTPUT FILTERS

A. C ALWAYS Located ACROSS V_{out}

B. L LOCATED BETWEEN CRUDE UNFILTERED V_{dc} AND STABILIZED V_{out}

1. BUCK
2. BOOST
3. BUCK-BOOST
4. LOW RIPPLE APPROXIMATION FOR OUTPUT SIGNALS AT f_{sw}

a) INDUCTOR RIPPLE:

$$\Delta i = \frac{V}{L} dt(switch)$$

b) CAPACITOR RIPPLE:

$$\Delta V = \frac{I}{C} dt(switch)$$

dt(switch)=(Duty cycle)*T_s(period of f_{sw})

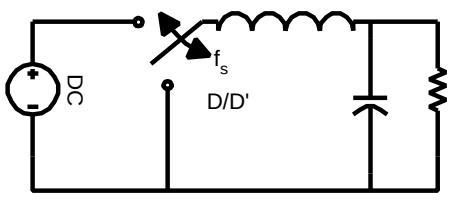
Introduction to Power Electronics Circuit Topologies: The Big Three

A. OVERVIEW

The Inductor in any PWM converter plays the role of a mechanical flywheel in that it stores energy between pulses. The solid state switches pulse energy at the switching frequency into the PWM circuit from the input but the inductor stores energy so that the energy drawn to the load does not appear pulsed at all. We will see below that both the precise location of the inductor in the circuit topology as well as the physical location of the switch on the specific terminal of the inductor are crucial to realize the three major PWM circuit topologies. The inductor –switch combination will have three unique topological locations. In section B, for simplicity, we will use the three major topologies to convert a DC input to various DC outputs that are both below and above the original V(in) in voltage. We will express the steady state transfer function of all converters as a function of the duty cycle: F(D)

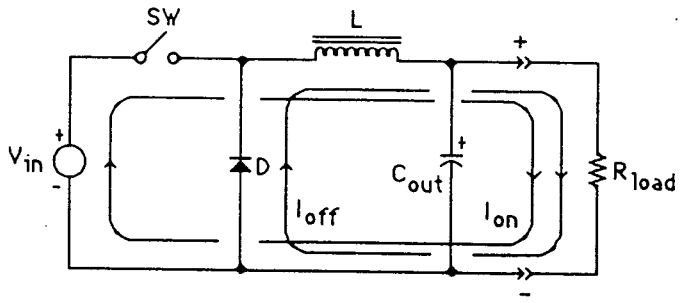
B. BUCK TOPOLOGY

(a) BUCK TOPOLOGY: Inductor attached to c in series. note how l avoids kvl violations for brief periods by acting as a buffer between v_{in} and v_{out} as well as storing energy.

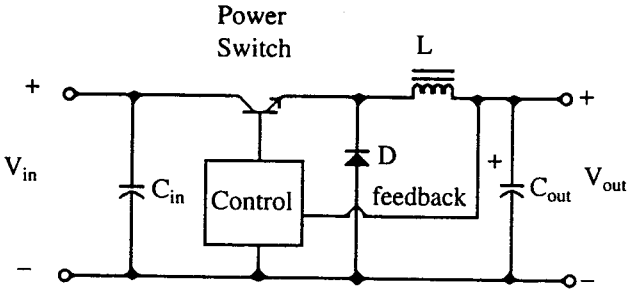


•V_{out}/V_{in} = D(DUTY CYCLE): v(out)) has a linear dependence on d; **v_{out} never exceeds v_{in}**

• Below we qualitatively outline the analysis of the BUCK circuit both for the switch on and off



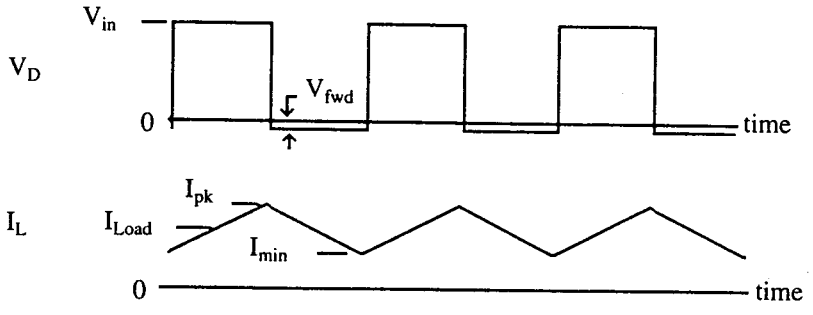
A basic forward-mode converter (buck converter shown).



$$I_{pk} \approx \frac{1.4 \cdot P_{out}}{V_{in(min)}}$$

$$V_{SW} \approx V_{in}$$

$$P_{out} \approx 0 - 1\ KW+$$

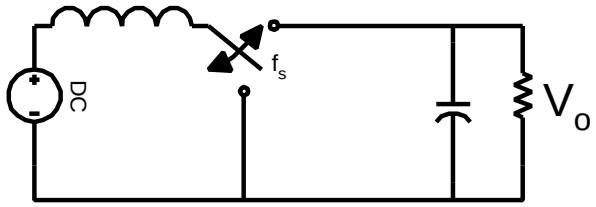


The buck regulator topology.

In lectures 5-7 we will go through this circuit in detail for now be sure to see the very different circuit for the two switch conditions on the bipolar transistor. The diode because of its bipolar nature is a switch that does not need to be actively driven by a gate drive.

B. BOOST TOPOLOGY:

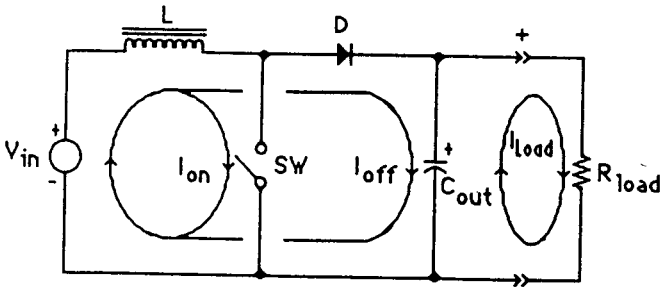
Inductor is attached to crude dc (rectified mains): again note that L is preventing kvl violations during switching as well as storing energy.



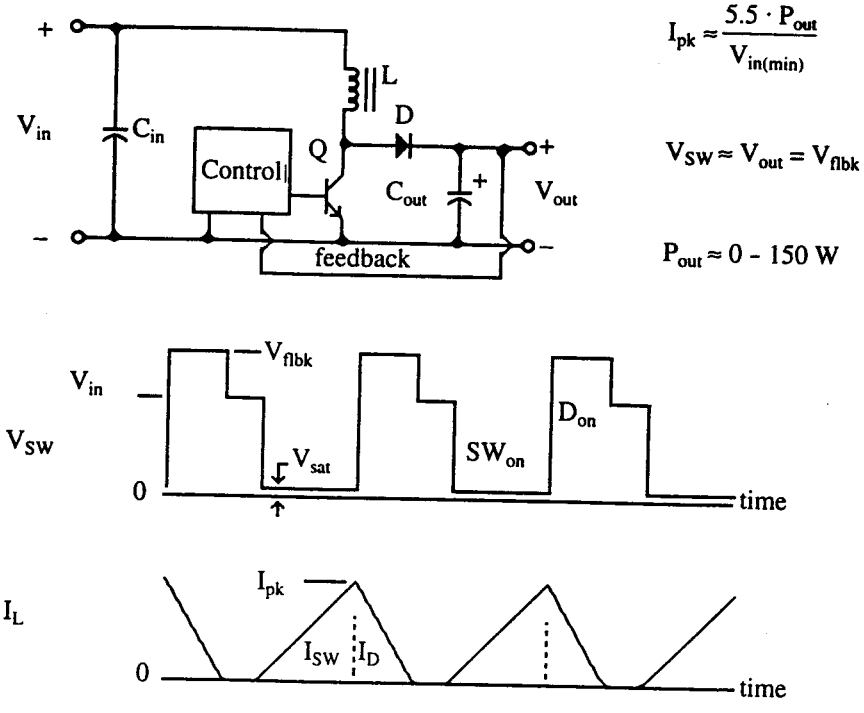
- V_{out} NEVER REACHES ZERO. v_{out}(minimum) = v_{dc} and can exceed v_{dc}
- V_{out} IS UNIPOLAR but can achieve $v_o > v_{in}$
- $V_o/V_{in} = 1 / (1-D)$. non-linear dependence on d will be shown in later lectures
- Note that the input and the output are NOT electrically isolated from each other as we have a common terminal to both the input and the output. How to easily fix this??. Finally, we consider one special case for the duty cycle- D=1/2

Consider the switch duty cycle of ½ and consider the power in the inductor for each switch position.
$p_{in}(av) = v_{dc}i/2$ while $p_{out}(av)=(v_{out} - v_{dc})i/2=p(inductor)$
if no losses occur in switching, wires or in reactive elements: $p_{in}=p_{out}$ which implies $v_o=2v_{dc}$.

On the next page we give a qualitative summary of the boost topology for the conditions of the bipolar transistor switch on and off. Note the very different current paths for the two circuit conditions. Of special note is the inductive kick fron the series inductor which makes the switch voltage exceed V(in) when the transistor is switched off**. Why does this occur??**



A basic flyback-mode converter (boost converter shown).

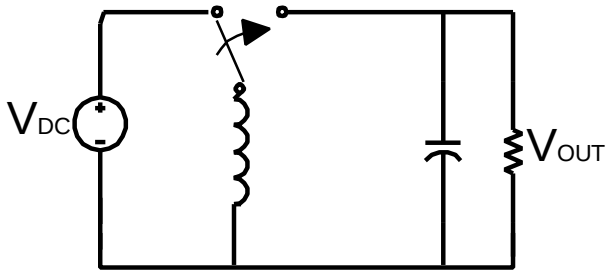


The boost regulator topology.

For now realize that the boost circuit while delivering an output voltage above V(in) does have to ask the solid state switch to handle a **peak current 6 times the nominal** average current when the switch is on. When the switch is off the solid state switch must withstand across itself a voltage up to the full output value.

C. BUCK-BOOST TOPOLOGY:

Inductor is connected in parallel with C which acts as a polarity reverser. Given $+v_{dc}$ as input in we generate $-v_{dc}$ out for a switch duty cycle of ½. Many analog circuits require both + and - v_{dc} supplies and this is an easy way to do it.



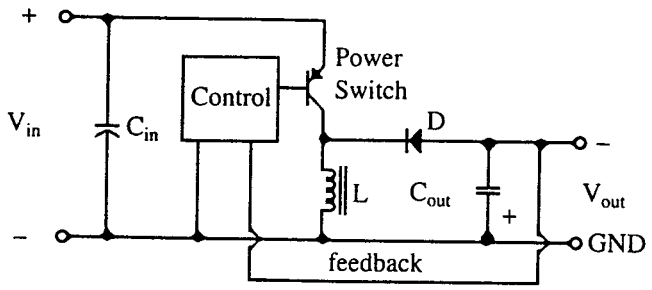
the inductor l again avoids kvl violations by acting as a current source temporarily.

- V_{out}(MINIMUM) IS NOW ZERO
- V_{out} IS OPPOSITE POLARITY TO v_{dc} due to current direction in the inductor that charges the c.
- $\int \frac{V_{dc}}{L} dt = \Delta i_L \Rightarrow i_L$ DOES NOT CHANGE

instantaneously so the capacitor charges negatively.

- FOR BUCK-BOOST EITHER $|V_{out}| > V_{dc}$ OR $|V_{out}| < V_{dc}$ IS POSSIBLE
- $V_{out} / V_{in} = -D / (1-D)$. non-linear dependence on d will be shown in lectures 5-7

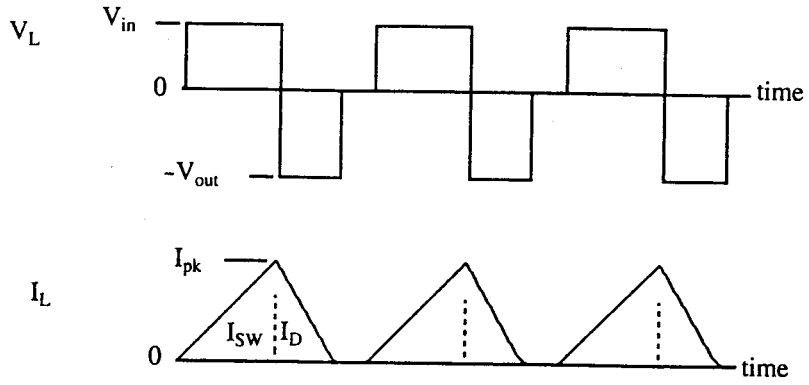
On the following page we show schematically the waveforms for the buck/boost circuit for both the switch on and the switch off. Again the ability to generate voltages above the input voltage comes at the price of expensive solid state switches. With the switch on we need to pass nearly 6 times the average current. With the switch off we need to stand off across the switch V(in) + V(out).



$$I_{pk} \approx \frac{5.5 \cdot P_{out}}{V_{in(min)}}$$

$$V_{SW} \approx V_{in} + |V_{out}|$$

$$P_{out} \approx 0 - 150\ W$$



The buck/boost regulator topology.

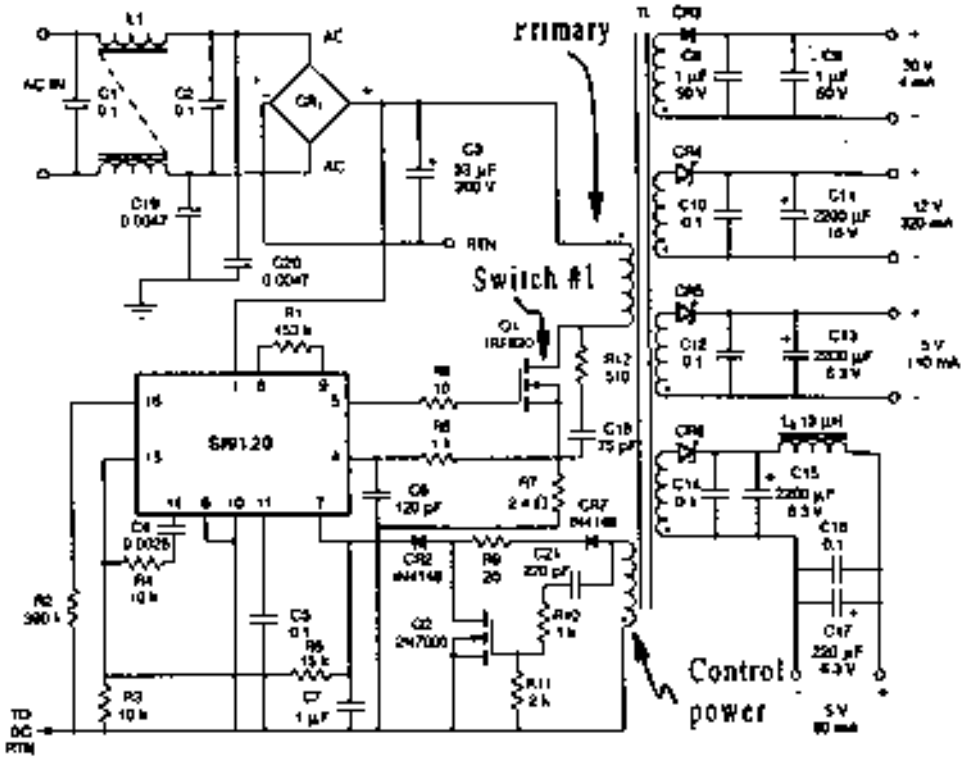
In preparation for your midterm exam, look at the attached schematic on pg. 8 of a flyback converter slowly - don't panic. try to find only the essential power electronics portions.

(1) identify the crude dc generation in the upper left driven by 120 ac mains. this CRUDE DC IS DRIVEN BY THE SWITCH #1 INTO THE TRANSFORMER PRIMARY.

(2) On the right side of the schematic notice the three secondaries of the transformers with the three dc outputs: 5, 12, and 30 v.

(3) Find the cmos transistor Q1 (middle) which is the switching transistor. From the gate of this cmos switch the gate control circuitry may also be found.

We will spend the rest of the semester detailing how such circuits work.



Commercial 5 W flyback converter for 170 V input and multiple outputs. From C. Varga, *Application Note AN90-2*. Santa Clara: Siliconix. 1990. Reprinted by permission.

D. Full Monty Comparison of the Big Three Topologies

Below we place three tables that compare the BUCK,BOOST, and BUCK/BOOST topologies as regards:

·Expected Loss in percent from the three topologies

1. **Rectifers of the output**
2. **The solid state switch**
3. **The magnetic core material in inductors as well as core material in transformers**
4. **Miscellaneous loss such: as wire losses, parasitic losses and radiative loss**

·Estimate the requirements of the switches both when on and when off. Details later!

The "Black-Box" Estimates for Losses Within the Various Topologies

Topology	Power Switch Type: Bipolar	Power Switch Type: MOS	Overall Estimated Efficiency (%)	Estimated Percent of Total Loss ($P_{(\%)}$): Power Switch and Drive (%)	Output Rectifier (%)	Magnetics (%)	Miscellaneous (%)
Buck	×		72	42	48	5	5
		×	76	35	55	5	5
Boost	×		74	55	35	5	5
		×	77	48	42	5	5
Buck-boost	×		74	55	35	5	5
		×	77	48	42	5	5

Estimating the Significant Minimum Parameters of the Power Semiconductors

Topology	Bipolar Power Switch: V_{CEO}	Bipolar Power Switch: I_C	MOSFET Power Switch: V_{DSS}	MOSFET Power Switch: I_D	Rectifier(s): V_R	Rectifier(s): I_F
Buck	V_{in}	I_{out}	V_{in}	I_{out}	V_{in}	I_{out}
Boost	V_{out}	$\frac{2P_{out}}{V_{in(min)}}$	V_{out}	$\frac{2P_{out}}{V_{in(min)}}$	V_{out}	I_{out}
Buck/boost	$V_{in} - V_{out}$	$\frac{2P_{out}}{V_{in(min)}}$	$V_{in} - V_{out}$	$\frac{2P_{out}}{V_{in(min)}}$	$V_{in} - V_{out}$	I_{out}

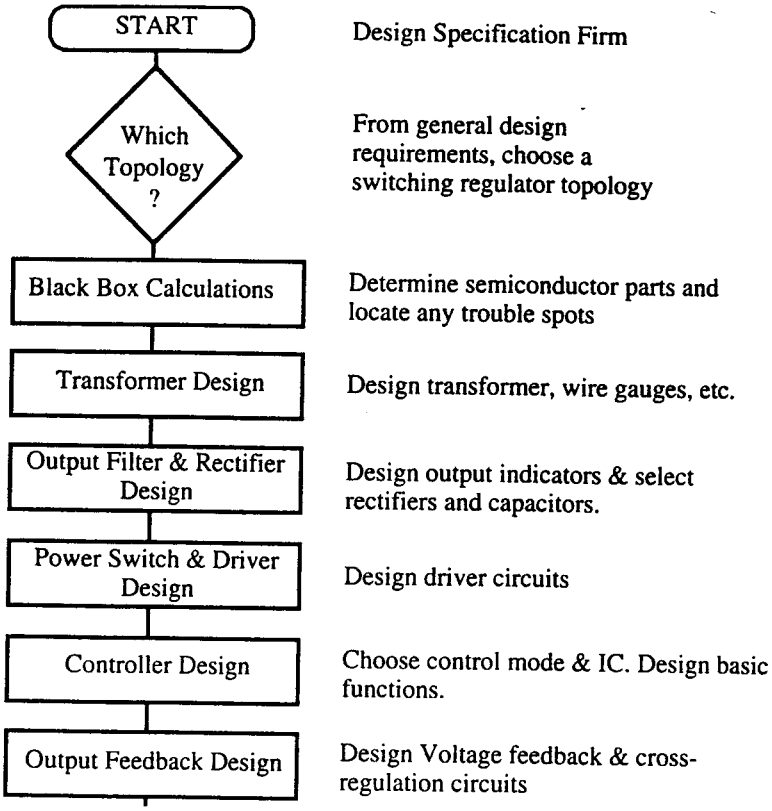
Comparison of the PWM Switching Regulator Topologies

Topology	Power Range (W)	$V_{in(dc)}$ Range	In/Out Isolation	Typical Efficiency (%)	Relative Parts Cost
Buck	0–1000	5–1000	No	78	1.0
Boost	0–150	5–600	No	80	1.0
Buck-boost	0–150	5–600	No	80	1.0

Again the purpose of the above tables is to illustrate that the choice of topology has a major impact on the tradeoffs involved in design. We want to do this as early as possible so one is aware of this from the start. We will in fact derive in later lectures many of the parameters simply given above. Still it is worthwhile to compare even now**.**

Next we outline a building block design approach.

Building-block Approach to Switching Power Supply Design



From the above approach we need to pick a starting point. We will focus next of the output filter design in the remainder of this lecture and in lectures 5 and 6.

E. BASIC TOPOLOGIES OF PASSIVE L-C FILTERS

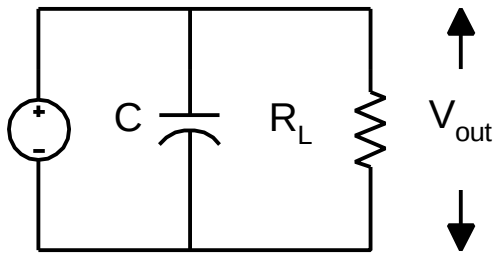
We will use L-C filters both to remove v_{ac} signals lost to conversion and to avoid kvl and kil law violations from the switching.

1. DC OUTPUT REACTIVE FILTER (L-C). This places a series L between two voltages sources v_{in} and v_{out}. It also removes or reduces the switch signal at f_s and passes only dc if designed properly. lets look at the two

pieces of an L-C filter seperately for clarity of each role. first the ouput capacitor.

a. FIXED CAPACITOR LOCATION: C ALWAYS PARALLELS R_L

RAW SIGNAL
$V(f_{SW})+V(DC)$



- C is in parallel with v_{out}
- $\Delta v_{out}/v_{out}$ is the quantitative regulation desired, $i_c = c*dv_c/dt$
- $\Delta Vcap = \int \frac{Iout}{C} dt \Rightarrow V_c$ DOESN'T CHANGE

INSTANEOUSLY. It takes time to do so. The time scale of interest is some function of t_{sw}. $\Delta v \sim i/c\ dt$ which implies for fixed i, Δv is smaller for large CAPACITOR values. for crude estimates of the desired C values, use the linear approximation.
If given or specified the Δv value allowed, i_{out} required, and dt from f_s, we can determine proper "C" in a quick calculation.

b. <u>VALUE OF L DESIRED</u>

- INDUCTOR IS OFTEN IN SERIES WITH V_{dc} AND V_{out} FOR A BUCK CIRCUIT

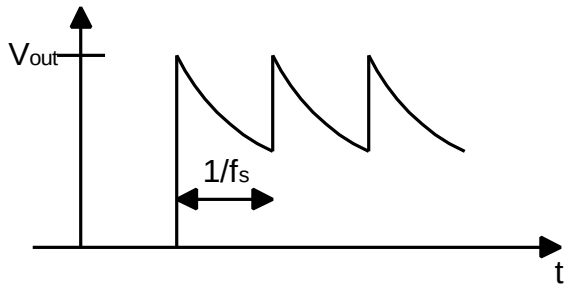
V_{dc} —⌇⌇⌇— V_{out}

$V_L=Ldi_L/dt \quad \int \frac{V_{dc} - V_{out}}{L} dt = \Delta i_L$

It is a fraction of t_s - Δt_s or $d't_s$
given v_{dc} - v_{out} (fixed) and dt (switch) for a specified Δi_l variation we fix l.Over a cycle of f_{sw} the $\Delta i_l/i_{out}$ can be specified. We can then fix the required "l". Higher f_s and smaller dt allows for smaller "L". For compact and light power supplies small L is a desired goal.

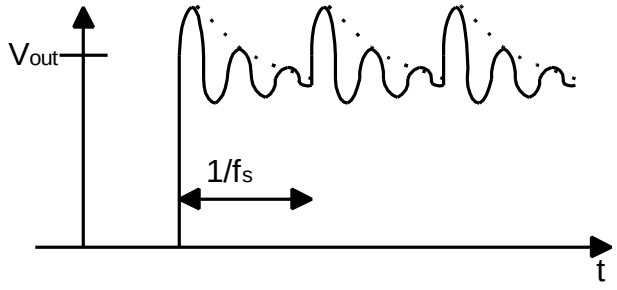
C. CONSIDER δ FUNCTION CURRENT CHARGING OF A CAPACITOR, C, TO V_O AT f_{sw}

The v_{out} will display RC decay in between δ function charging due to load dc current



If this δ function charging occurs via a wire with stray inductances which are **typically 5nf/cm at high frequencies**, then the switching waveform would then appear as a decaying sinusoid with both overshoot and undershoot at a frequency $w = \frac{1}{\sqrt{LC}}$ and decay envelope with

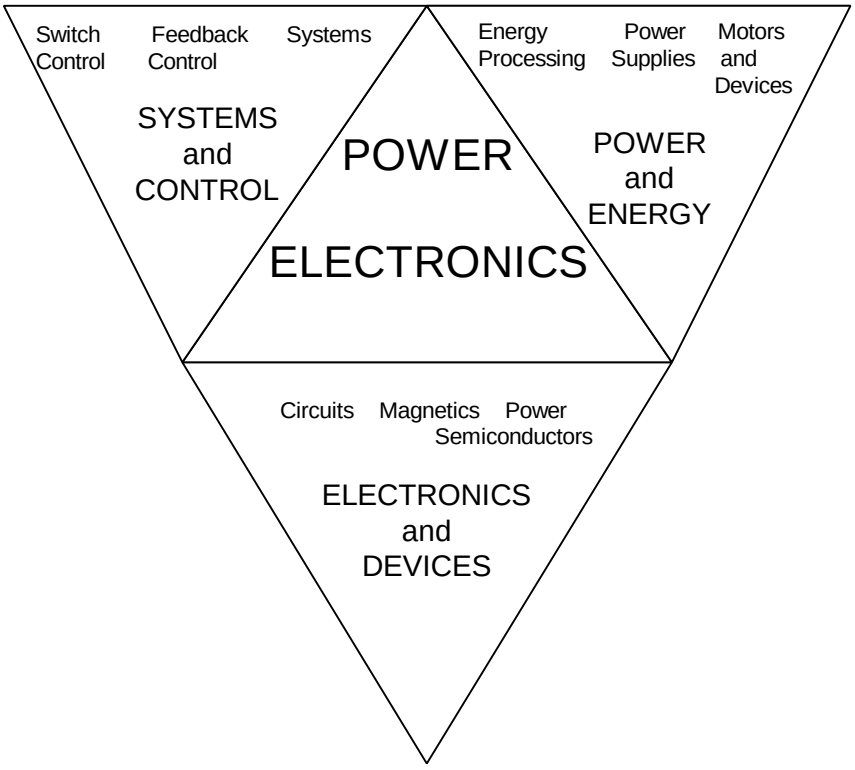
$\tau = RC$



HW#1: Thinking question #2

Give some general trends for the small ripple approximation in a simple L-C output filter for increasing switch frequency f_{sw} (i.e. smaller t_s). Show that a smaller "C" is allowed for fixed I drawn at the load and chosen Δv levels. Do a similar argument for the inductor size required

Now we can better appreciate the following chart which trys to depict all the aspects of ee that power electronics brings together to work on one topic energy conversion: controls, power, parasitic elements, and electronic devices to name a few.



OUR TWO SEMESTER COURSE as regards use of Erickson's text will be as follows. ALL HW PROBLEMS WILL BE FROM ERICKSON

CHAPTER		TOPIC
2	FALL SEMESTER	PWM CONVERTERS $V_{out} = f(D)V_{dc}$ (CRUDE) FIND f(D) FOR BUCK, BOOST, BUCK-BOOST
3	FALL SEMESTER	DC TRANSFORMER MODELS FOR POWER EFFICIENCY OF CONVERTERS
4	FALL SEMESTER	AVAILABLE SOLID STATE SWITCHES AND SWITCHING LOSSES
5	SPRING	D/D' CONTINUOUS vs. DISCONTINUOUS OPERATING MODES. PROGRAMMED DURATION OF D BUT D' AND D" SET BY CIRCUIT CONDITIONS
6,7	SPRING	CONVERTER CIRCUIT TOPOLOGIES AND SMALL SIGNAL ANALYSIS. SMALL SIGNAL TRANSFER FUNCTIONS WILL BE USED FOR CURRENT OR VOLTAGE FEEDBACK MODELS
8,9	SPRING	CONTINUOUS MODE VOLTAGE FEEDBACK TO ACHIEVE REGULATED OUTPUT FROM UNREGULATED INPUT

10 SPRING	DISCONTINUOUS MODE VOLTAGE FEEDBACK: SIMPLIFICATIONS AND STABILITY ISSUES, V_{out} = f(D, LOAD)
11 SPRING	CURRENT FEEDBACK CONTROL: CONTINUOUS OR DISCONTINUOUS MODES
12, 13, 14 FALL	MAGNETICS DESIGN OF INDUCTORS & TRANSFORMERS
15 SPRING	HARMONICS AND HARMONIC POLLUTION
16-18 SPRING	LOW HARMONICS RECTIFIER
19 SPRING	ZERO V, I SWITCHING TO MINIMIZE SWITCHING LOSS

GRADING:
1.HOMEWORK 60 percent-with 10 points from each chapter2, 3, 4, 12, 13, and 14
2. Midterm exam 20 percent
3. TERM PAPER 20 percent with 10 extra points for special projects