LECTURE 3

How is Power Electronics Accomplished:

I. General Power Electronics System

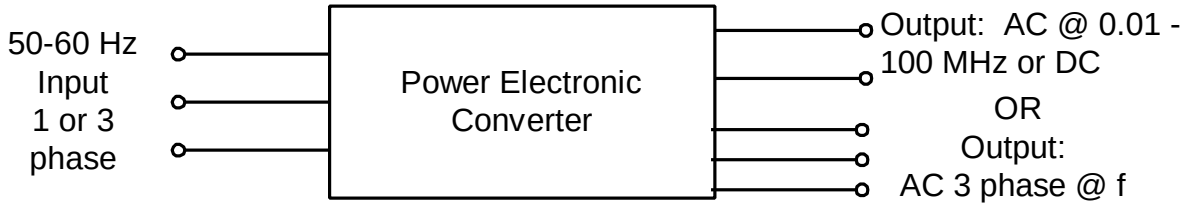
A. Overview
B. Open Loop No Feedback Case
C. Feedback Case and Major Issues
D. Duty Cycle VARATION as a Control Means on the Switching signal
E. Continuous CONDUCTION MODE (CCM) VS. DISCONTINOUS CONDUCTION MODE (DCM)
F. SWITCHING AND KIRCHOFF'S LAWS

II. UNREGUALTED AC MAINS TO REGULATED DC CONVERTERS: SIMPLEST CASES

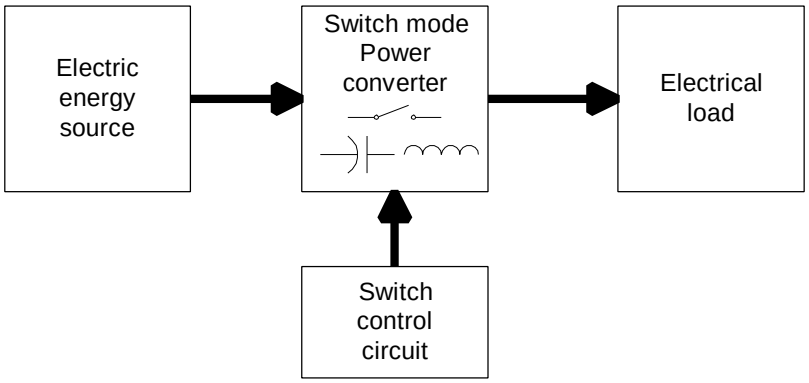
A. UNFILTERED DC SWITCH
B. Passive L-C FILTERED DC SWITCH
C. Skin Effect and Proximity Loses IN WIRES

A. Overview

In Power Electronics we take SINGLE OR 3 PHASE AC MAINS,at 50-60 Hz,1-10^6 Watt AS INPUT AND GET EQUAL POWER OUTPUT AT A FREQUENCY OF: $0 \leq f \leq$ GHz. FOR EXAMPLE, AC @ "ARBITRARY FREQUENCY" AS OUTPUT FOR MOTOR DRIVE INVERTER, OR MHZ POWER SUPPLY.



$1\ W < P < 10\ MW \Leftarrow 10^6$ range



THE KEY ENABLING TECHNOLOGY IS LOW COST (< $100) AND LOW LOSS (< 1%) SOLID STATE SWITCHES THAT CAN HANDLE 1W TO SEVERAL MEGAWATTS OF POWER FLOW THROUGH THEM AT SWITCHING FREQUENCIES 60Hz < f_{sw} < 1MHz. The switch frequency is f_{sw} and is chosen so that $f_{sw} >> f_{out}$.Also f_{out} is chosen by duty cycle control of the on-off of the switch. This course provides details on how we achieve this.

In the circuit topology we have two general methods.

1. Pulsewidth modulated(PWM) converters

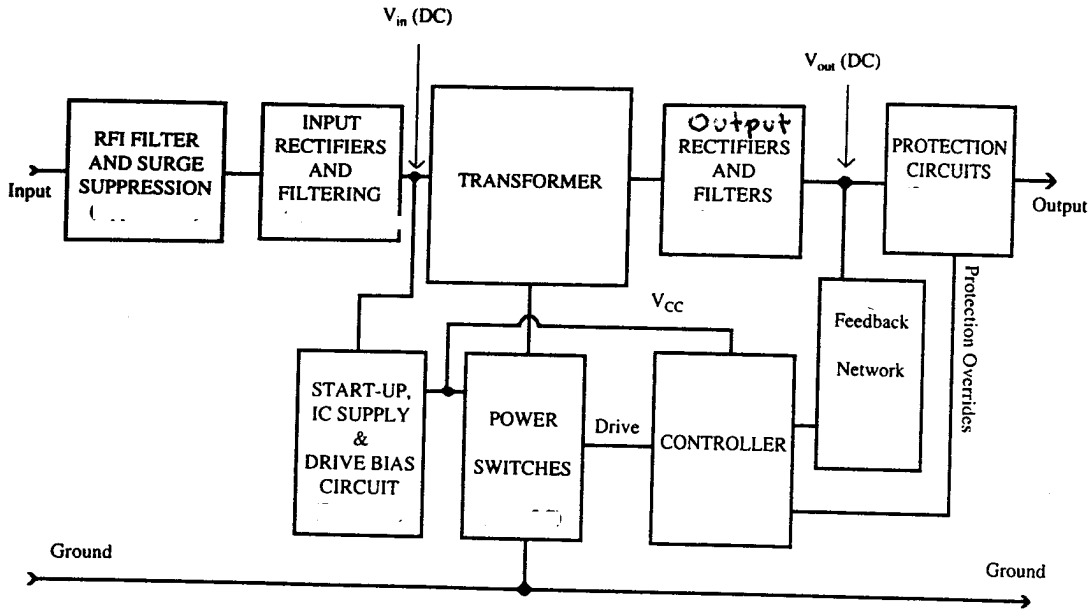
Employed in portable equipment or where high power flows demands the highest efficiency power conversion of about 90 %

2.Resonant switched converters

Utilized to achieve smaller size supplies and still avoid the electronic noise generated by PWM converters.

SWITCHES Driven between cutoff and saturation lose only 1% of the transmitted power.. To better appreciate the whole of power electronics design before we begin the detailed study of each individual subtopic we show on the next page a functional block diagram including:

- Input rectifiers and RFI filters as well as output and input filters
- Power switches and Controller Chip with associated feedback
- Specialized circuits for start-up of a PWM supply
- Protection circuits for the switches and the loads
- Note the use of an isolation transformer operating at the switch frequency and not the mains frequency



The functional block diagram for a PWM switching power supply.

We will cover output filters in lecture 4 and pulse width control in lectures 5-7 for the three circuit topologies:buck, boost and buck- boost.

Before we venture into details we can learn a lot by a black box overview. Specifically, from the output power requirements we can work backwards to the input power required. This input power will be driven by the nominal input voltage allowing us to ascertain:

- Average input current regardless of circuit topology which has 10- 25 possibilities
- After the circuit topology is chosen we can then determine the peak currents in the input of the switch mode. These peak currents will vary by factors of 1.5 to 6 as shown below on the next page.

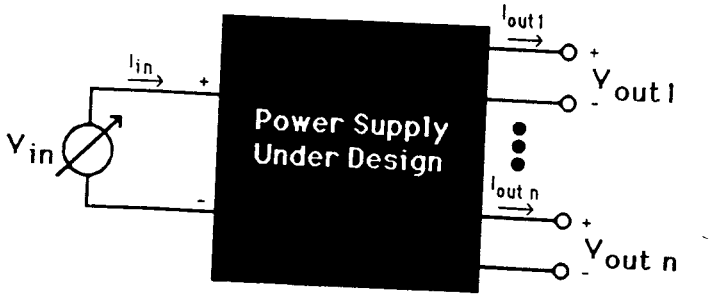


Figure 3–17 The SMPS treated like a black box.

1. Output power

$$P_{\text{out}} = \sum_{m=1}^{n} (V_{\text{out}(m)} I_{\text{out}(m)}).$$

2. Input power

$$P_{\text{in}} \cong \frac{P_{\text{out}}}{\text{est. efficiency}}.$$

3. Average input currents

$$I_{\text{in(av)(nom)}} = \frac{P_{\text{in}}}{V_{\text{in(nom)}}}$$

4. The input peak current
This is completely determined by the topology chosen.

$$I_{\text{pk}} = \frac{kP_{\text{out}}}{V_{\text{in(min)}}}$$

where k =: 1.4 for the buck, and full-bridge
=: 2.8 for the half-bridge, and half-forward
=: 5.5 for the boost, buck-boost, and flyback

The value of the peak current is useful in the design of the flyback-mode inductors and transformers. For the forward-mode supplies, it is just a curiosity at this time.

Hopefully this tilted overview will be kept in mind as we proceed in the course. Each subsection takes so much effort that we easily lose the overall goal.

In section B we start the introduction to the waveforms found in the PWM converters. Their shape and their mathematical representation. Again this material is meant

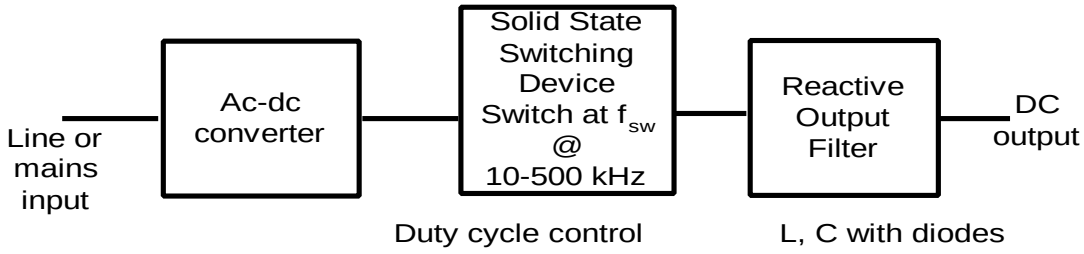
to get your brain thinking and see general trends-detailed analysis begins in lecture 5.

B. NO FEEDBACK CASE

The Dc we often talk about as input to the switch circuits may just be rectified mains. Can you show that you really know/remember Fourier analysis by proving or finding in a text that the spectrum of a full wave rectified cosine function V_oCoswt is:

$$V(t) = 2V_o/\pi + 4V_o/\pi * \sum_{n=1}^{\infty} \frac{Cos(np)}{1-4n^2} Cos(nwt)$$

where $w = 2w_{in}$, that is the fundamental component is twice the input frequency. The dc term is roughly 2/3 V_o This is the nominal DC if no filtering is employed. We have to filter out the AC components prior to the switch circuit. Note the harmonic amplitudes decrease as $1/n^2$ very rapidly and the first term at $2w_{in}$ has an amplitude $4V_o/\pi$. More on this later for now assume that the DC level is achieved. We will see later in the course that feed forward compensation can achieve good voltage stability with high ripple rejection. A $v_{out} \approx 1$ - 2% for $v_{in} \pm$ 10% requires low impedances. Often feedback is added to highly regulate (0.1%) the dc output as shown below in section C:



We want higher frequency switching to achieve lower weight and smaller size for all circuit elements such as C, L and transformers.

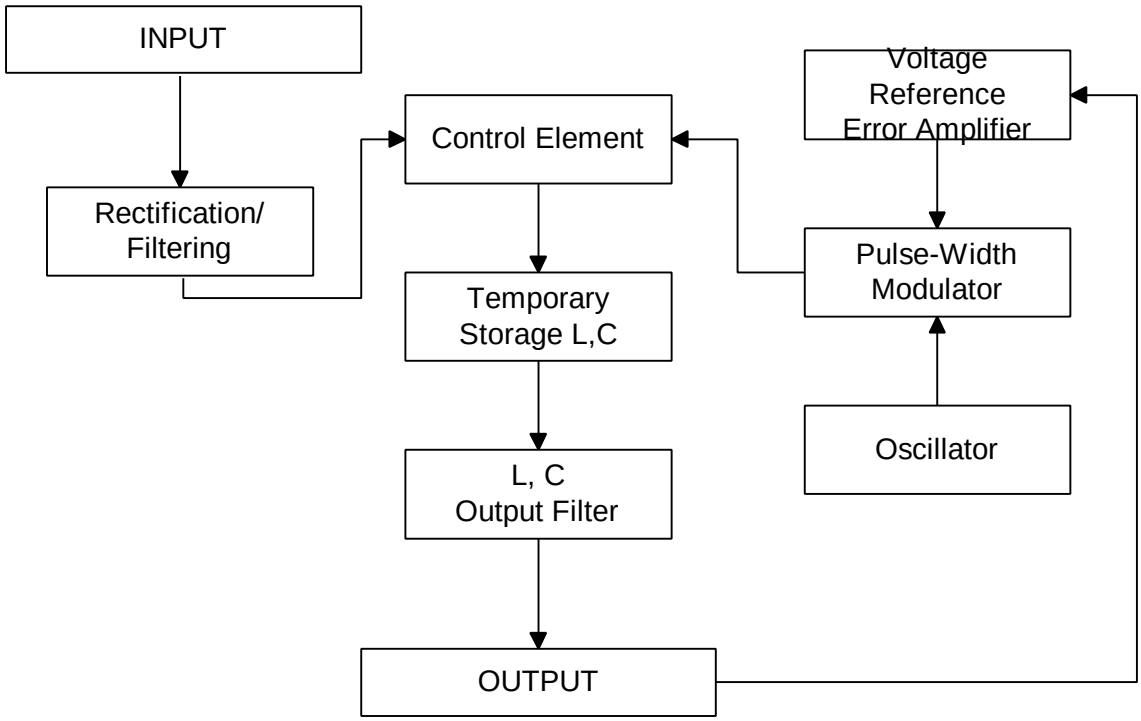
CAN YOU TELL WHY THIS IS???

Also keep in mind that the choice of circuit topology for the switches effects the maximum ratings that the switches will need to have. We are switching the SOLID STATE POWER DEVICES which CAN HANDLE POWERS 100 TIMES THEIR INSERTION LOSSES. As a rule of thumb as $f_{sw} \uparrow$ the power ratings of devices $\downarrow$. Moreover, if we want both high f_{sw} and high power it will cost 10-100 times more than standard switching devices. Finally, the switch when on must handle i(max) and while off the switch must be able to block V(max). BOTH I_{max} AND V_{max} MAY BE 10 TIMES HIGHER THAN AVERAGE VALUES.

THE CONCEPT OF TRADE OFFS IS CRUCIAL TO DESIGN.

C. FEEDBACK CASE

Below is illustrated a generic feedback design:

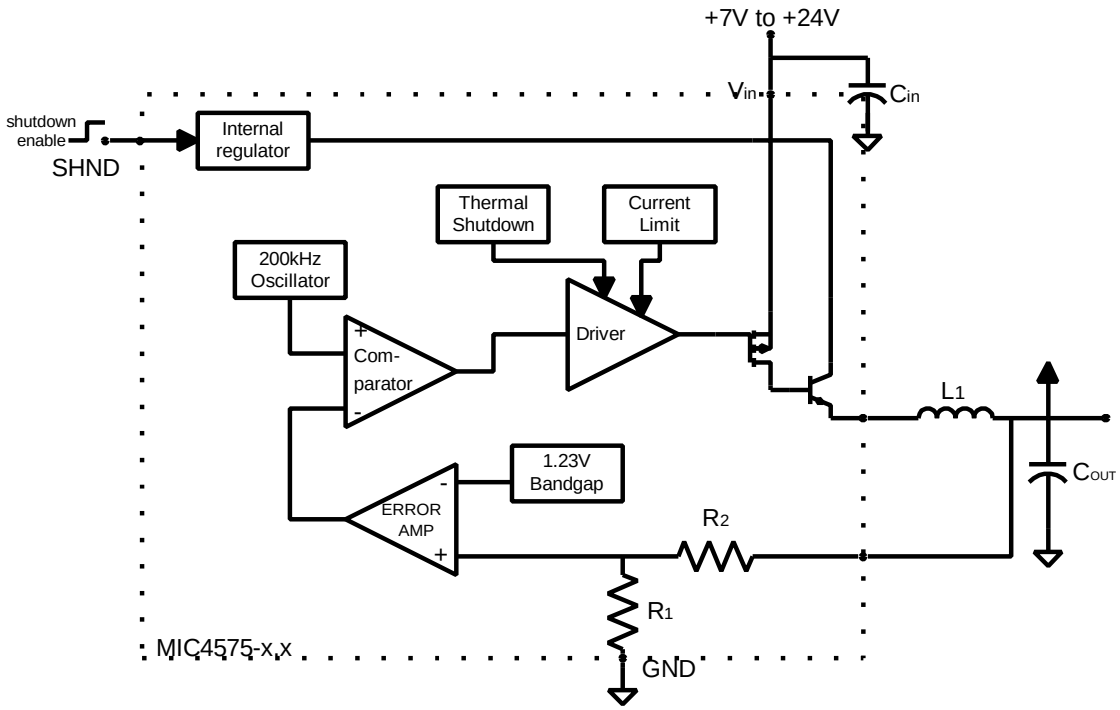


FEEDBACK BLOCK DIAGRAM

BELOW IS A MORE DETAILED FEEDBACK LOOP THAT INCLUDES:

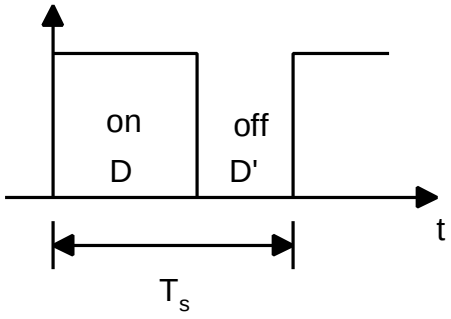
- Controlled shutdown
- Thermal protection

Do not worry about details at this point.



D. DUTY CYCLE CONTROL ON SWITCHING SIGNAL TO VARY V(OUT)

Although we fix f_{sw} and hence the cycle duration T_s, the on/off durations of the switch within the cycle are fully controllable form zero on time to a maximum of T_s. Variation of D will vary V(out)



assuming that only the control circuitry contains the switch we divide t_s into 2 periods that vary in a complementary fashion

$$\tau_{on} \equiv DT_s,\ \tau_{off} \equiv D'T_s, \text{ and } (D + D')T_s \equiv T_s$$

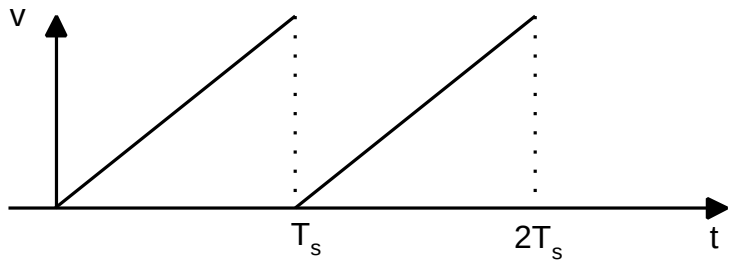
That is $D + D' \equiv 1$ when there are no dead periods.

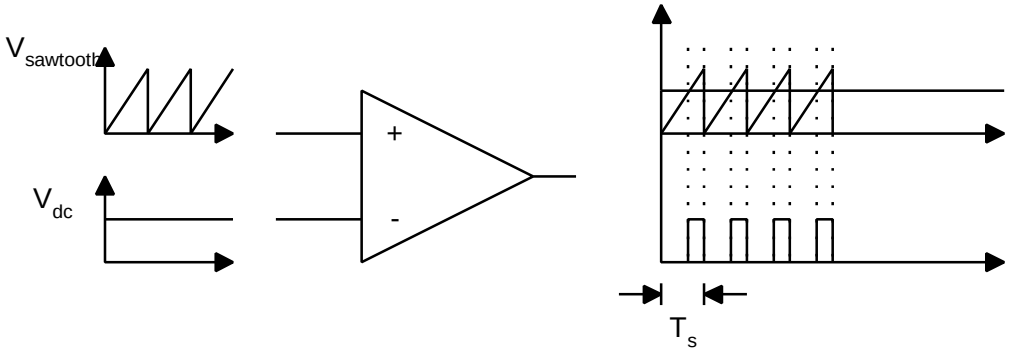
- HENCE FOR A PULSED SWITCH SIGNAL THE AVERAGE DC OUTPUT VOLTAGE MAGNITUDE WILL BE VARIED BY THE CHOICE OF D (OR D')
- how does an electrical engineer easily achieve both arbitrary switching frequency f_s and a variable d/d' ratio? that is achieve control from $0 < d < 1$?

FOR HW#1 - COME UP WITH A SIMPLE CIRCUIT TO GET f_{sw} AND D CONTROL, THEN COMPARE YOURS TO THE FOLLOWING COMPARATOR CIRCUIT SOLUTION. the comparator looks at two input signals, one dc and one ac.

THE AC WAVE SETS f_{sw} BUT THE DC LEVEL SETS THE DUTY CYCLE

- $V_{IN}(1)$: CHOSEN DC REF. VALUE SETS D/D' RATIO
- $V_{IN}(2)$: SAWTOOTH WAVE SETS f_s
- $f_{sw} \equiv$ SWITCHING FREQUENCY





COMPARATOR

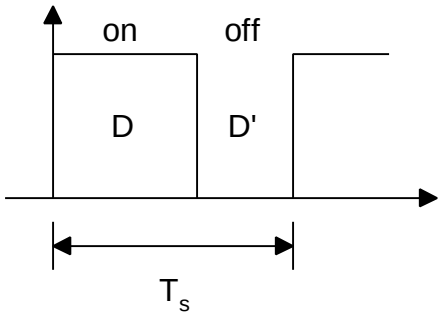
the comparator output is a pulse modulated signal (pwm) whose on time varies over the interval 0 < d < 1. d varies as v_{dc} changes from zero (d = 1 or 0) to v_{dc} equal to peak sawtooth value (d=d).

HOW DOES YOUR CIRCUIT PERFORM?

E. IN ACTUAL CIRCUIT TOPOLOGIES TWO SWITCH OPERATION MODES EXIST

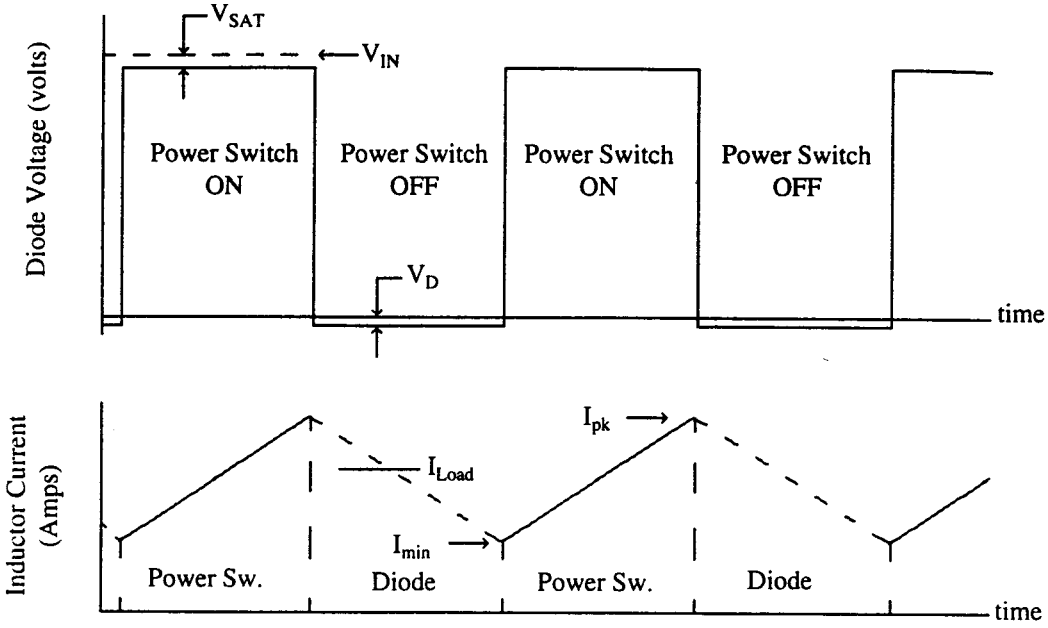
1. CONTINUOUS CONDUCTION MODE

•Assuming only the control signal to the switch and not other circuit conditions drive the switch, THEN, during the full interval T_s only d and d' periods are available in the switch mode



WE ASSUME V_{OUT} = f(D); D IS SET BY THE DESIGNER ONLY AND IT IS NOT AFFECTED BY THE LOAD OR CIRCUIT CONDITIONS. Later we will find the switching to be more complex due to large ripple effects under certain loads as well as the use of devices which conduct in one direction only. This will cause the switch be toggled at time other than those set by the control signal as shown in section 2 below.

On the next page we will show a diode voltage and an inductor current-both fully controlled by the switch interval.



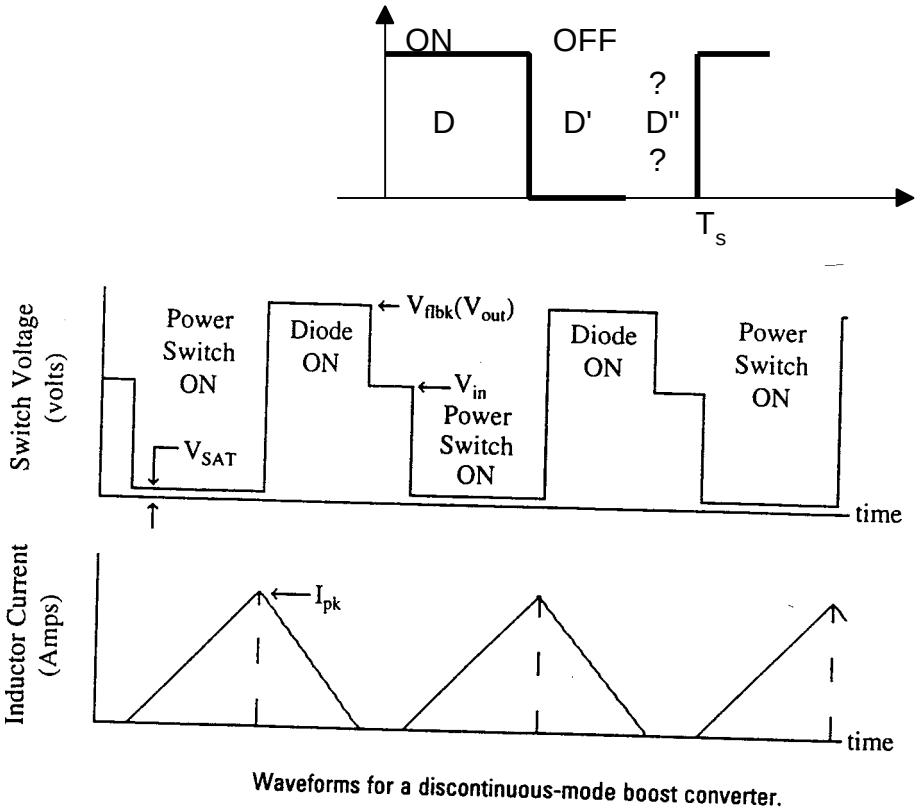
The voltage and current waveforms for a forward-mode converter (buck).

What if the inductor current wanted to go negative with a diode in the circuit?? What would occur??

2. DISCONTINOUS CONDUCTION MODE

An extra period "d" occurs in the switching that is created by circuit topology conditions, not by the switch drive alone. For example, switches may close or open due to circuit conditions alone as when a diode will not conduct in the opposite direction even though the controlled switch asks it to do so. This change occurs during a portion of a switch time interval and is independent of gate signals. Another example would be a bipolar transistor which conducts in only one direction and not in the opposite as MOS transistors can do.. The onset and duration of this "out of control" interval are not set by control switch signals but rather by the circuit conditions as we will see later.

Below we show this interval "d" and the associated switch voltage and inductor current waveforms.

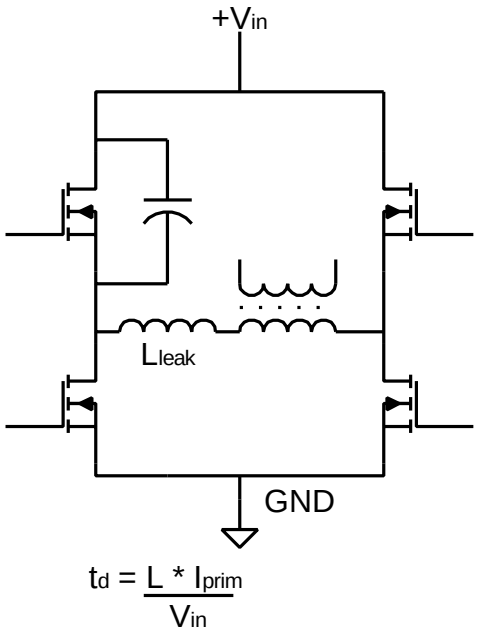


Waveforms for a discontinuous-mode boost converter.

NOTICE ABOVE THAT THE INDUCTOR CURRENT CANNOT GO NEGATIVE IN THIS TOPOLOGY AND CHOICE OF SWITCHES. Be careful, other circuit topologies and switch choices could allow a negative inductor current to occur.

FOR A SPECIFIC EXAMPLE, consider below the switch mode circuit where l (leakage) of a transformer causes a dead-time t_d when

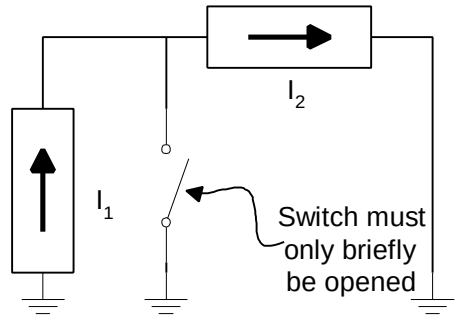
l (leakage) discharges. This leakage inductor is not on your original circuit design. It is a parasitic element of the real transformer which modifies the time durations expected from switching via control signals alone.

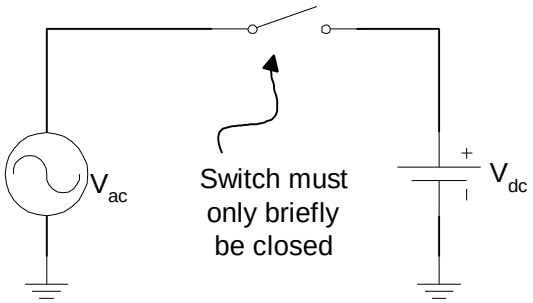


L_{eak} causes a dead time where some switching transistors stay on for an additional duration due to inductor current even though control signals try to turn them off at a specific time. You should be convinced that there may be at a minimum three intervals in t_s. Usually d is still controllable by the designer but d' and d" are divided up by the circuit conditions. Now we find in a switching converter v_{out} = f(d and circuit topology as well as load). Usually in the d" period the previously controllable interval switches are not working as expected.

F. SWITCHING AND KIRCHOFF'S LAWS

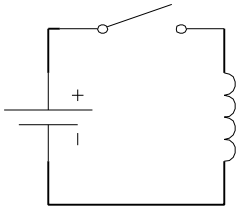
One thing our switches must never be allowed to do is violate Kirchoff's voltage (kvl) and current (kil) laws. Explain the problems that arise over time if the switches are closed too long in the circuits below:



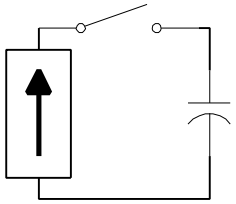


What's the problem?

What's the problem?



Inductive circuit with
long-term KVL problem if switch
remains closed too long

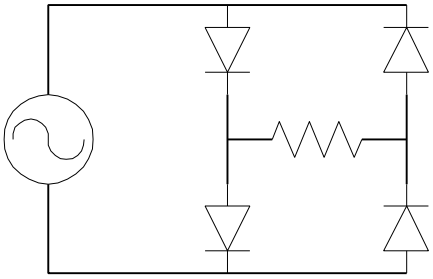


Capacitive circuit with
long-term KIL problem if switch
remains closed too long

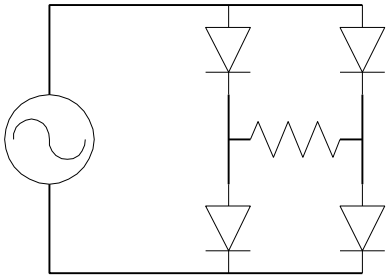
KVL and KIL problems in simple energy storage connections.

These connections are allowed only if brief in duration kvl and kil laws provide guidance for power electronics switching where we ONLY briefly connect the input to the output.

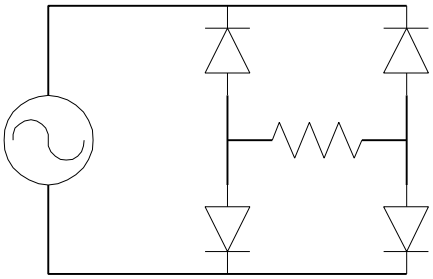
1. NEVER CONNECT V SOURCES DIRECTLY WITHOUT AN INDUCTOR IN BETWEEN TO LIMIT TRANSISENT CURRENTS.
2. NEVER OPERATE SWITCHES SO THAT UNEQUAL CURRENT SOURCES ARE CONNECTED IN SERIES WITHOUT A CAPACITIVE PATH TO LIMIT TRANSIENT CURRENTS.
3. LOOK AT THE FOLLOWING DIODE BRIDGE CONNECTIONS ON THE NEXT PAGE TO SPOT KVL VIOLATIONS:



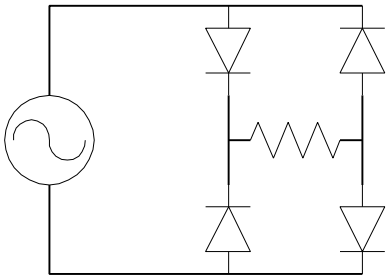
a) KVL problem



b) KVL problem when $V_{in} > 0$



c) No energy flow

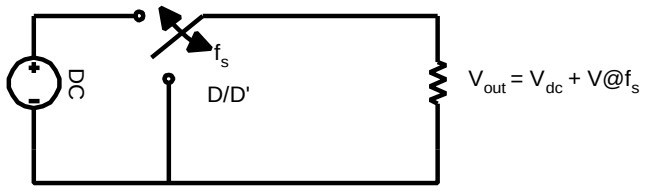


d) OK

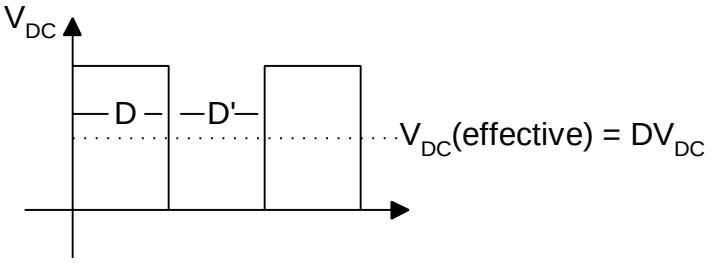
III. UNREGULATED AC MAINS TO REGULATED DC CONVERTER: SIMPLEST CASES

A. UNFILTERED DC SWITCH

- SWITCH IS PLACED IN BETWEEN AN UNREGULATED RECTIFIED AC WHICH WE TERM CRUDE DC.
- $V_{out}(DC) \propto DV_{DC}$ - $0 \leq V_{out} \leq V_{DC}$ NOTE IN THE SIMPLE CIRCUIT WHICH CONTAINS NO L OR C ELEMENTS: V_{out} CANNOT EXCEED V_{DC}



V_{out} WILL BE A SQUARE WAVE FROM O TO V_{max} AS SHOWN:



FOURIER ANALYSIS SHOWS that the harmonic content of the signal varies for d = d' = ½ (equal on/off time square wave) as: $a_n = (2V_{DC}/n\pi)\mathrm{Sin}(n\pi/2)$

WHAT HAPPENS IF D ≠ D'?

That is the fundamental component n=1 is the largest with an amplitude $v_{dc}/2\pi$. using this basic information test your ee skills by proving or disproving the statements below.

$V_{out\ av} = DV_{DC}$

$V_{out\ rms} = \sqrt{D}\, V_{DC}$ (prove this)

$$P_{out} = \frac{V_{DC}^2}{R} D$$

WITH CAPACITIVE OUTPUT FILTER (IDEAL)

$V_{out\ av} = DV_{DC}$

$V_{out\ rms} = DV_{DC}$ (prove this)

$$P_{out} = \frac{V_{DC}^2}{R} D^2$$

The output has an effective dc value that varies with choice of d. unfortunately it also has a large ac component. Note also that ($V_{out(average)} \neq V_{out(rms)}$)

- IN THIS SITUATION THE ONLY POWER LOSS IS FROM:
  - $-V_{ac}(out)$ @ f_s, WHICH IS RECOVERABLE WITH A FILTER AND CONVERTABLE INTO DC

-INTERNAL SWITCH LOSSES DUE TO

a) Dc loss $i_{out}*v_{on}$ is assumed small, almost lossless. v_{on} can be 1-2 volts for standard semiconductors

b) However, switching can be large. switching loss arises due to energy stored in parasitic elements. $p = f_{sw}*e(stored)$ The energy stored varies as c ($1/2\ cv^2$) or l ($1/2\ li^2$) which may be dissipated at each switch cycle by equivalent series resistance (esr). Energy wasted in resistance is lost to power conversion. Losses occur during transition time of the switch from the closed position to the open position and reverse.

B. PASSIVE L-C FILTERED DC SWITCH

- A low pass l-c filter is always placed between the switch and load allowing for flatter dc levels and/or low frequency ac levels for V_{OUT}
- L-C FILTER always partially converts previously wasted (due to resistance) v @ f_s into useful output
- FILTER LOSSES DO OCCUR DUE TO EQUIVALENT SERIES RESISTANCE OF REAL COMPONENTS — CONSIDER INDUCTOR LOSSES

$I_L^2R_L$ losses

R_L ARISES DUE TO:

-Hysteresis loss in inductor core material $\propto f_s$

-Eddy current losses in inductor core material $\propto f_s^2$

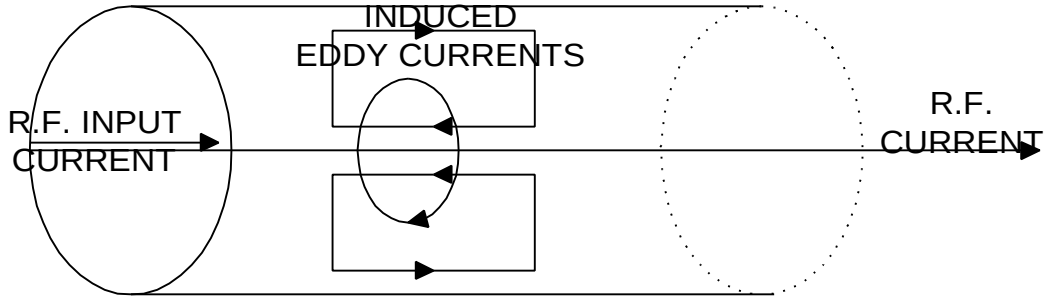
-copper wire losses due to ohmic resistance as given in G

C. SKIN AND PROXIMITY EFFECTS in Wires :

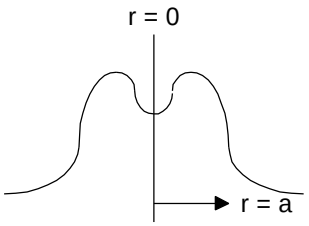
Wires that carry the currents at the switch frequencies, as compared to the mains frequencies, do not have simple Ohmic losses. Rather at high frequencies due to two well known effects high frequency currents drive the wire resistance up by a factor of 2 to 200 from the DC wire loss we might expect. Clearly , this causes large increases in the expected resistance which we must be aware of. For now we just introduce this phenomena qualatatively. This could be thought of as a parasitic resistance that we have to add to the circuit diagram to get an accurate analysis.

1. SKIN EFFECT

Skin effect: AC current flows in surface of the conductor. In case of superposition of DC and AC currents only the AC current causes the skin effect. This makes $R_{AC} > R_{DC}$ for the same wire.



INDUCED EDDY CURRENTS IN THE WIRE OPPOSE CURRENT AT THE CENTER OF THE WIRE THUS CANCELLING THE CENTER CURRENT. LEAVING CURRENT ONLY IN THE OUTER EDGES OF THE WIRE. THIS CAUSES THE CURRENT PROFILE IN THE WIRE TO HAVE A DISTINCT SPATIAL DIP AT THE CENTER POSITION r = 0.



$\delta^2 = 2 / (\omega \mu_o \sigma)$

ω - circular frequency of the AC current
μ_o - 1.256 * 10^{-6} Vs/m
σ - conductivity of the wire material

Skin depth of Copper (cu) = $\delta_{cu} = \frac{7.5cm}{\sqrt{f}}$

Typical values: 8.3mm at 60Hz and 0.75microns at 10GHZ.

2. PROXIMITY EFFECT

Much more important than the simple skin effect for multi-turns of wire on a transformer coil.

RF magnetic field from nearby wires act upon the wire of interest and forces an additional current to flow in the wire of interest. The superposition with the original current in the wire increases the current density on one side of the wire compared to the other.