Lecture 51
Tailoring Dynamic Response with Compensation

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Lecture 51
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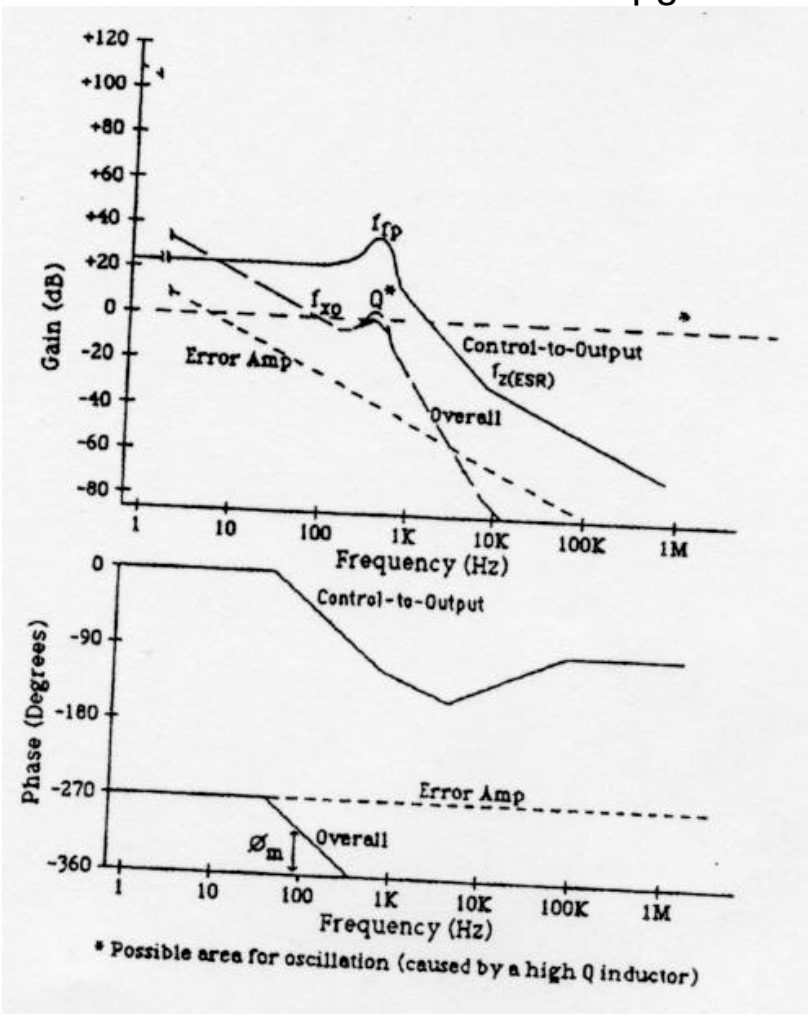
A. Compensation Networks

1. Overview of G_c (Alterations Tailoring)

a. Rude and Crude Single Pole Compensation

Consider an original converter G_{VD} with DC flat response and a 40 db roll-off, starting at f_{FP}, with strong "Q peaking" in the plot below. The original control-output G_{VD} crosses unity gain with too little phase margin and also has a zero due to the ESR in the filter capacitor. The op-amp single pole response is a dashed line from DC at a slope of 20 db/decade as we saw on pg.13 in Lecture 50.



The G_{VD}, has a double pole at f_{FP} due to the L-C filter network,. It has a unacceptable phase margin for closed-loop operation.

The new T(s) involves $G_C G_{VD}$ and it's f_C is located at f_{XO}. At this frequency the phase plot of the new T(s) must have a phase margin ϕ_M =45° to meet stability. We create a new T(s) by placing the error amp G_C(single pole) in tandem with the original G_{VD} to create the new T(s) which lies just below the old T(s) in the plot on page 2. The "shift of the new T(s) plot" to the left of the G_{VD} plot is caused by the single pole G_C choice we made. It reduces the f_C of the new T(s) as compared to the old T(s). **Is this a good thing entirely?** G_C will introduce 270° of CONSTANT phase shift. Hence for acceptable phase margin of 45 ° on the new T(s) at f_{XO}, we can only allow 45° at f_{XO} from the G_{VD} portion of the old T(s). Otherwise a potentially unstable closed-loop will result.

The new T(s) has a lower f_C, typically 50- 500 Hz, which is too slow. Momentary transients may cause the output to go to values OUTSIDE the SPEC'c. The "Q peaking" of G_{VD} makes the conservative choice of f_{XO} to be placed at even lower frequencies to avoid oscillation at the cross-over frequency. Single pole compensation is too crude a means to stabilize an original T(s) with 40 db per decade slope at the cross-over frequency.

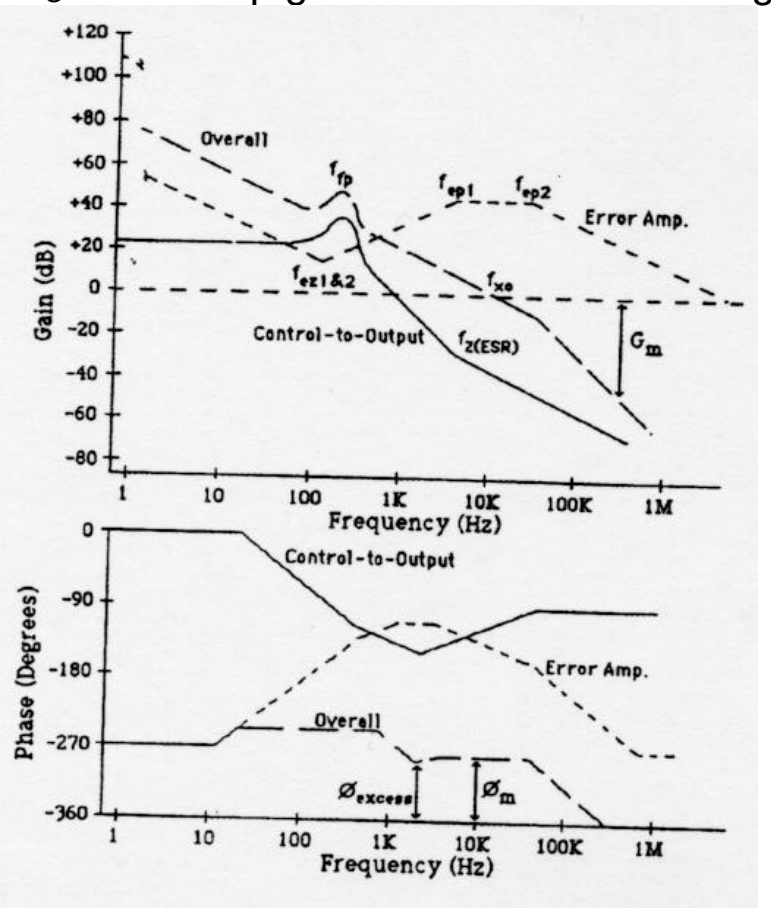
b. Two Pole/ Two Zero Compensation

This is a BETTER WAY to stabilize and improve a G_{VD} that rolls off at 40 db/decade. The G_C design is very complex as it attempts to take into account both the desired phase margin, INCREASE the maximum f_C for the new T(s) and it also try's to cancel out the parasitic zero in G_{VD} caused by the ESR in the filter capacitor. This requires the G_C designer to do all of the following:

i) Use a PAIR of zeros from G_C to cancel the effect of the two G_{VD} poles at the L-C resonance of the output filter.. Usually the zero's are placed on either side of the f_{FP} location to minimize the "Q peaking" from the L-C filter double pole.

ii) Chose one of the G_C pole locations to cancel out the ESR zero in the original G_{VD}. The second pole is at very high frequency and insures the proper phase margin at cross-over of the unity gain point of the new modified T(s)

Page 13 of Lecture 50 has the two zero/ two pole G_C Bode plots versus frequency. This G_C is placed in tandem, with the G_{VD} of the converter response to from a new T(s) with improved closed-loop properties. G_C Bode response is shown below by a short length DASHED lines. The original G_{VD} plot, with a flat DC response up to the point f_{FP}, is depicted by a solid line, that crosses unity gain at 40 db per decade at a frequency f_{GDO}. Our task is to shift this plot to the left in the **final or overall T(s) plot**, which is represented by a long DASHED curve. This has the effect of increasing the f_C of the loop gain above that of the original G_{VD}.

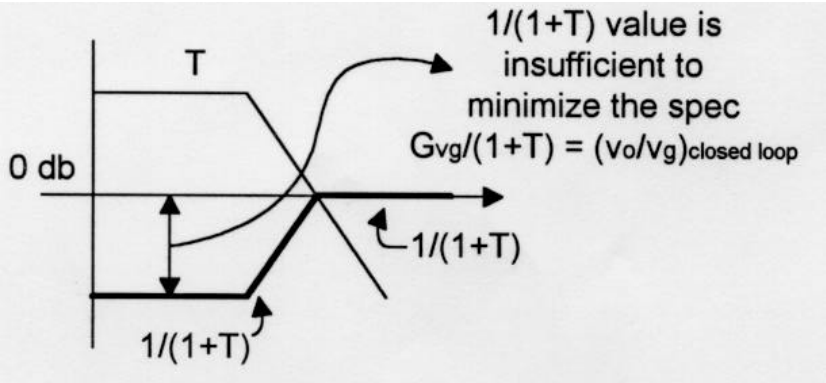


The overall or final T(s) plot starts at DC with a slope of 20 db/decade. Around f_{FP} it has a "Q peaking" but maintains its 20 db/decade slope past the unity gain frequency, f_{XE}, due to the double zero's in G_C all the way until the very high frequency pole kicks in because the first pole of G_C cancels the ESR zero. This

T(s) plot has an effective 20 db/decade roll off from DC to the location of the very high frequency pole where the roll off is 40 db/decade from there on. The difference between the f_{VDO} , where the uncompensated G_{VD} crosses unity gain, and f_{XE} where the new T(s) crosses unity gain is the improvement in the frequency response achieved. Moreover we go from the original G_{VD} crossing unity gain with 40 db/decade slope to the new T(s) which crosses unity gain at 20 db/decade. We now have a designed in phase margin, ϕ_M, as well as an excess phase condition, ϕ_{EXCESS}. Actually the excess phase is the most important as it is the point of closest approach to 360 ° at any point on the Bode plot. This is due to the fact that f_{XE} lies much higher than f_{FP} ,where the L-C resonance occurs. In summary, we achieve both improved phase margin and improved transient response by the use of such a complex G_C network. In short we have a higher performance power supply all because of a simple op-amp based feedback network design. We showed the flow of the design but not the detailed calculations involved. The calculations are iterative and will be considered below in some examples as well as in HW.

2. Lag Compensator

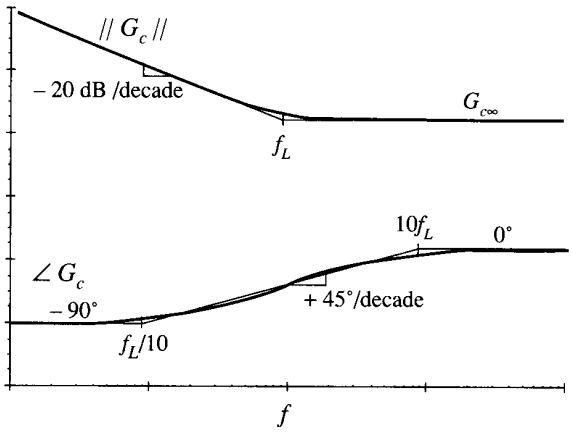
Consider an original T with a 20 db/ decade roll off and its associated and 1/1+T plots. We are satisfied with the stability of the old T(s). We are **not** satisfied with the 1/ (1+T) plot in the low frequency region, since the mains voltage varies a lot.



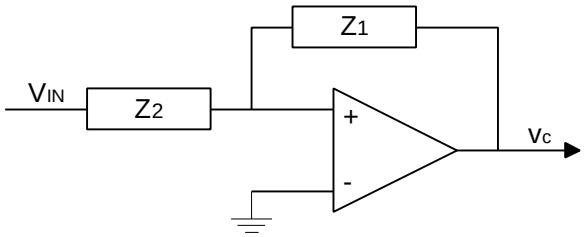
We add via G_c(s an inverted zero to increase T at low frequency and thereby meet the $\frac{\Delta V_o}{\Delta V_g}$ specification at mains frequencies on the PWM dc-dc converter. $G_{c\infty}$ is carefully chosen to obtain desired f_c in compensated T/1+T or T plots.

$$G_c(s) = G_{c\infty}\left(1+\frac{W_L}{s}\right)$$

Choose the inverted zero frequency, $f_L < f_c/10$ so that no ϕ change occurs at f_c. That is, we alter T and 1/1+T at low f gain but leave unchanged T's phase margin at the cross-over frequency. If the DC loop gain $\rightarrow \infty$ we find V_{error} due to power supply, V_G, changes $\rightarrow 0$. The desired G_c vs f is plotted below which will address our modified low frequency T(s) design goals. :



Op. Amp. Implementation



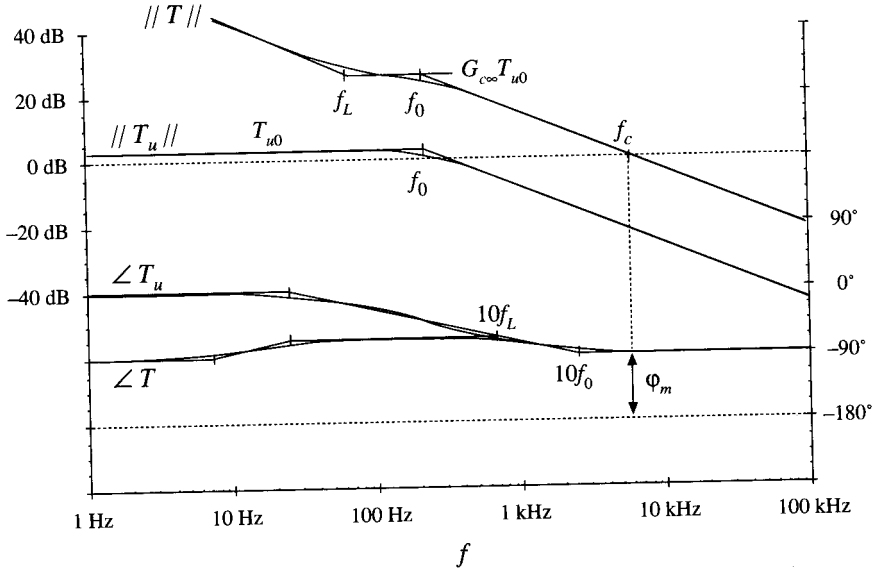
For HW # 4, using R's and C's ,what is your Z_1 and Z_2 to get the desired inverted zero transfer function.

T(compensated) = T(original) G_c(s) and we chose T(original) = $\frac{T_{vo}}{1+s/w_o}$ for illustration purposes above. Note also the absolute value of $G_{c\infty}$ effects the desired f_c of the new T(s). The power supplies transient response specification in turn determines f_C. Hence by careful choice of f_L and $G_{c\infty}$ could also change f_C.

$$|T| = 1 = \frac{T_{vo}\ G_{c\infty}}{f / f_o}$$

We have already insured that we will addd no phase from f_L at the old. If we wish to vary f_C in the new T(s) then $f_c = T_{vo}\ G_{c\infty}\ f_o$. Given the T_{vo} as fixed from the converter response G_{VD} we can only diddle $G_{c\infty}$ to achieve the desired f_c for the new compensated T(s)

$$G_{c\infty} = \frac{f_C(\text{desired})}{T_{vo}(\text{original T}) f_o(\text{original single pole})}$$ is our design guide

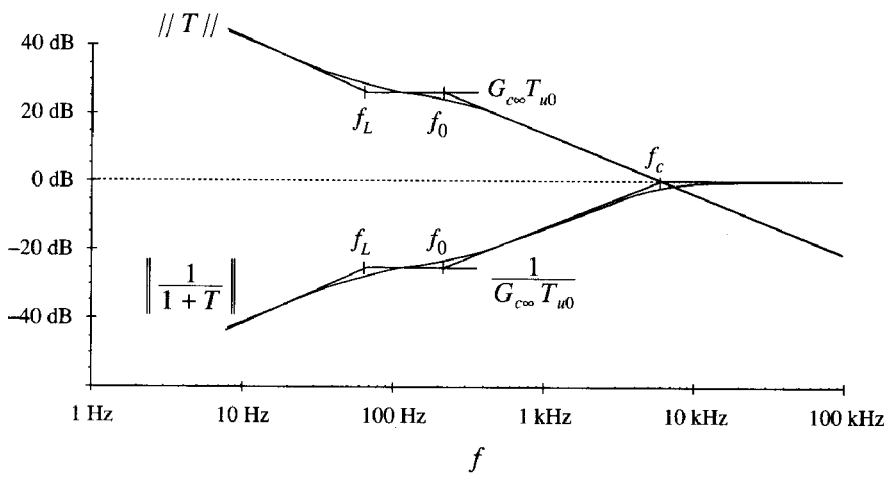


Summary of the LAG design method is:

(1) Choose new f_c (desired) of compensated T(s) which sets $G_{c\infty}$.

(2) Choose f_L (inverted zero) << f_c. so no phase is contributed

Use algebra-on-graph to get the new compensated 1/1+T Bode plots. Our primary goal is to increase the low frequency value of T to reduce Z_{OUT} and G_{VG} based variations by the factor 1/ (1+T), but at the same time we can increase f_C without jeopardizing closed loop stability. Again this is an iterative design process that requires cut and try “guestimates”, iteration and design compromises as we will see in the HW.



LAG G_C insures in feedback PWM converters mains voltage variations and Z_{OUT} are very well regulated since 1/1+T $\rightarrow$ 0 @ low f. What about at higher frequencies of interest??

A common AC mains to output spec is:

$$\frac{\Delta V_o}{\Delta V_g}\,(@100/120Hz) = \frac{G_{vg}(@100/120Hz)}{1+T}$$

This Spec by the power supply user and G_{vg} from the choice of the converter topology, specify the required 1/1+T to achieve it.

3. Hybrid PID Compensator(Two Pole/Two Zero)

This G_C is used to get the BEST or optimum new T(s) with both mains variations and dynamic response in mind:

a. Increased f_c for better transient response

$\Delta t = \frac{1}{2p f_C}$ We seek as high f_C as possible,YET f_C <1/5 f_{SW}

b. Small Output Variations from low f ΔV_g Variations

We achieve both a and b by adding to the original T(s) a $G_c(s)$ to get a new $T_{eff}(s) = T_{old} * G_c(s)$

If the original T(s) was stable we do not want to add because of the additional G_C ϕ lead near the original f_c or we may degrade the stability or original phase margin. We can also improve it as well.

$$G_c(s) = G_{cm} \frac{(1+\frac{w_L}{s})}{(1+w/w_p1)} \frac{(1+w/w_z)}{(1+s/w_{p2})}$$

↓ ↓

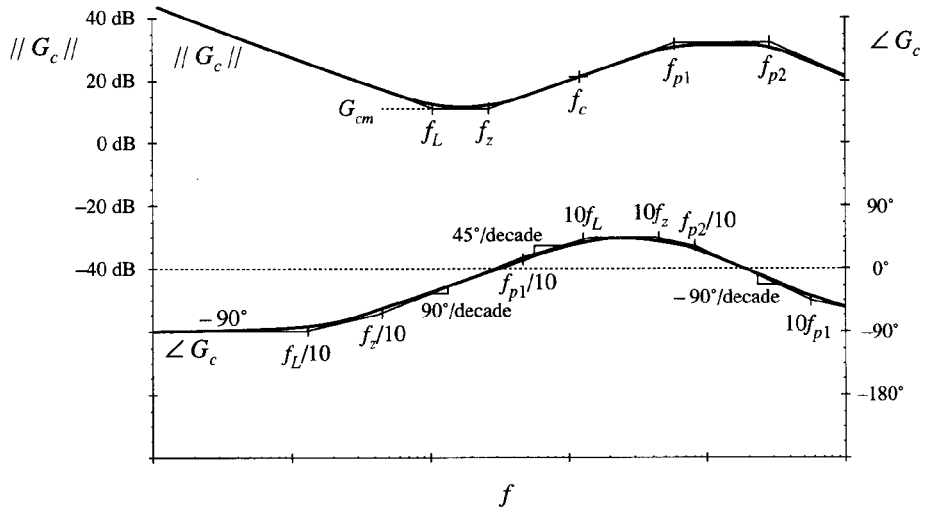
PI form **PD form**

Inverted zero adds to gain of T(s) at low f. Both poles are required to feep the new T(s) gain low at the switch frequency, f_{sw}.

As $s \to \infty$ $\angle G_c \to -90$ } ϕ at frequency extremes

$s \to 0$ $\angle G_c \to -90$ } is -90^o

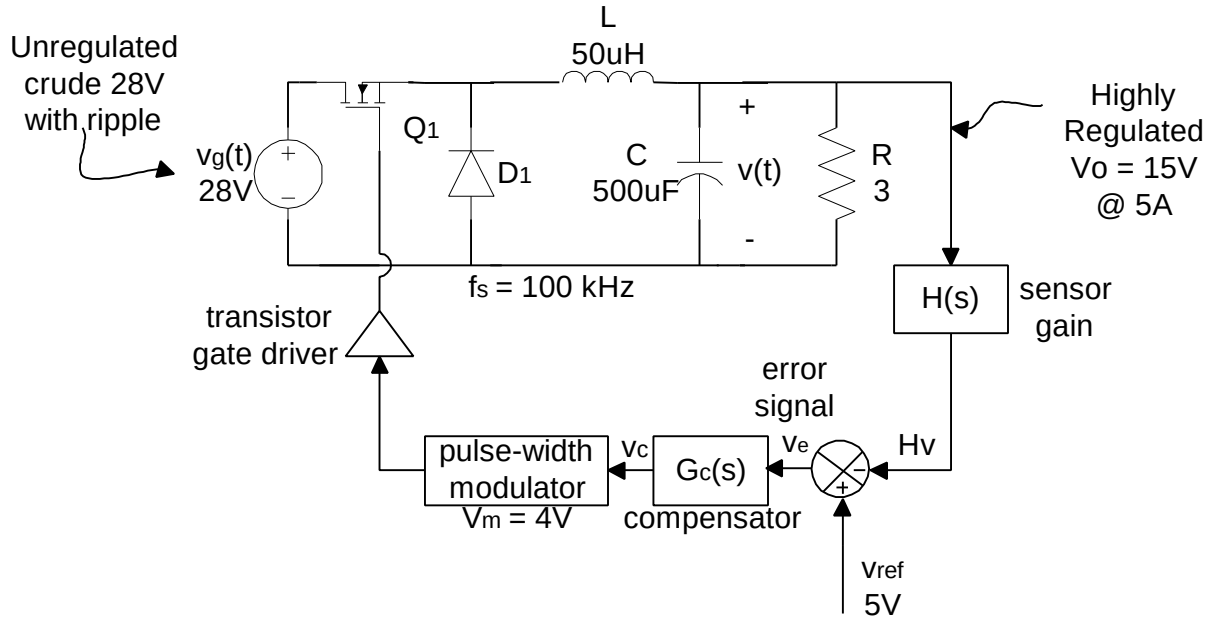
For a range of intermediate frequencies we can ADD positive phase



We can place this positive phase where the old T(s) or G_{VD} will benefit most. We also choose in a very conservative fashion $f_c < f_{sw}/10$ for the new T(s). The zero locations are f_L and f_z are chosen below the original cross-over frequency , f_c. Whereas the frequency location of the two poles f_{p1} and f_{p1} are purposefully placed above the original cross-over frequency , f_c. We must also be careful that the choice of op-amp is such that the frequency response of the op-amp exceeds all pole and zero frequency locations. Finally we try to choose an op-amp with $f_{MAX} < f_{sw}/10$ so that we do not amplify switch noise.

B. Design of Proper Feedback PWM Buck Converter:

f_{sw} = 100 KHz and we keep the T(s) maximum f_C well below this value as described above. Consider the following BUCK circuit



1. DC Conditions:

H(s) is achieved via precision temperature and frequency compensated resistors and is:

$$H = \frac{V_{ref}}{V_o} = \frac{5}{15} = \frac{1}{3}$$

Quiescent or dc duty cycle for buck topology is

$V_o = DV_g \Rightarrow D = 0.536$ and the DC control voltage is $D V_M = 2.14$

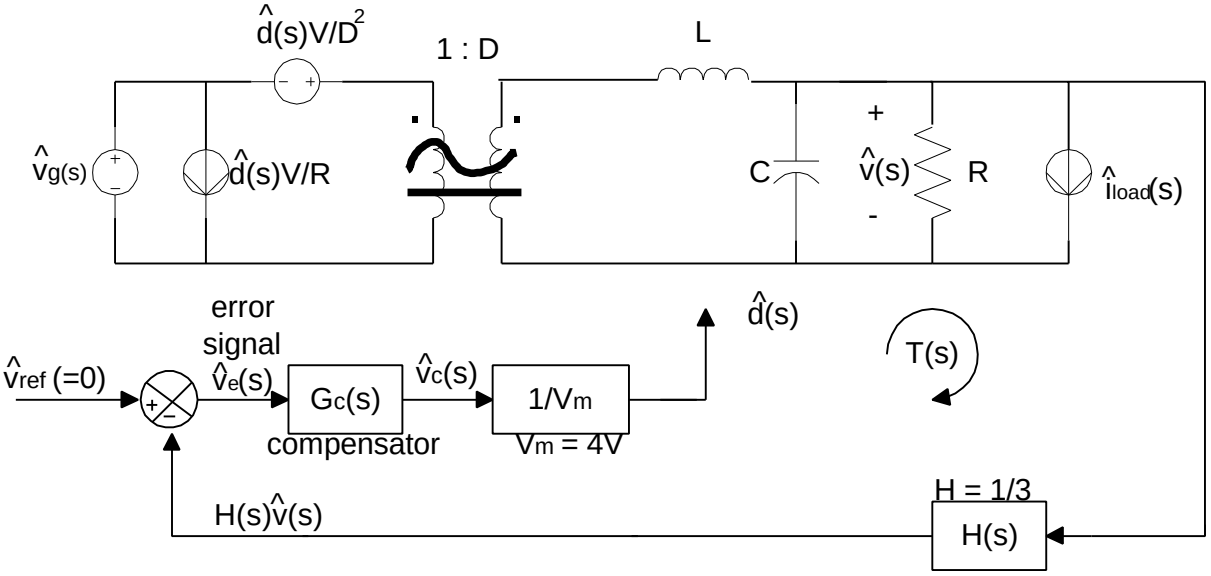
2. Open loop AC Conditions:

$$G_{vd}(s) = \frac{V}{D} \frac{1}{1 + s\frac{L}{R} + s^2 LC}$$ is found from the BUCK converter

open loop block by shorting out the v_g sources and solving for V_{OUT}/ d. We then compare to the standard form second order transfer function and equate terms.

$, \frac{R}{L} = w_o Q, w_o^2 = 1/LC, \frac{V}{D} = \frac{15}{.536} = 28$ or 29dB

Note how the choice of the DC operation duty cycle effects the converter DC or low frequency level. This in turn shifts T(s) plots in the vertical direction.



$f_o = \frac{W_o}{2p} = \frac{1}{2p\sqrt{LC}} = 1KHz$ for: L = 50uH and C = 500uF

For R=3 then $Q = \frac{R}{w_{oL}} = R\sqrt{C/L}$ = 9.5 or 19.5 dB for the "Q peaking" effect, which we can term the high Q case !

$$\text{open loop } G_{vd}(s) = \frac{29db}{1+\frac{s}{W_o Q}+(\frac{s}{w_o})^2}$$

Likewise, **with the same poles as G_{VD}**, we can determine by setting d=o

$$\text{open loop } G_{vg}(s) = D\,\frac{1}{1+\frac{s}{w_o Q}+(\frac{s}{w_o})^2} = .536 \text{ or } -6 \text{ db for the}$$

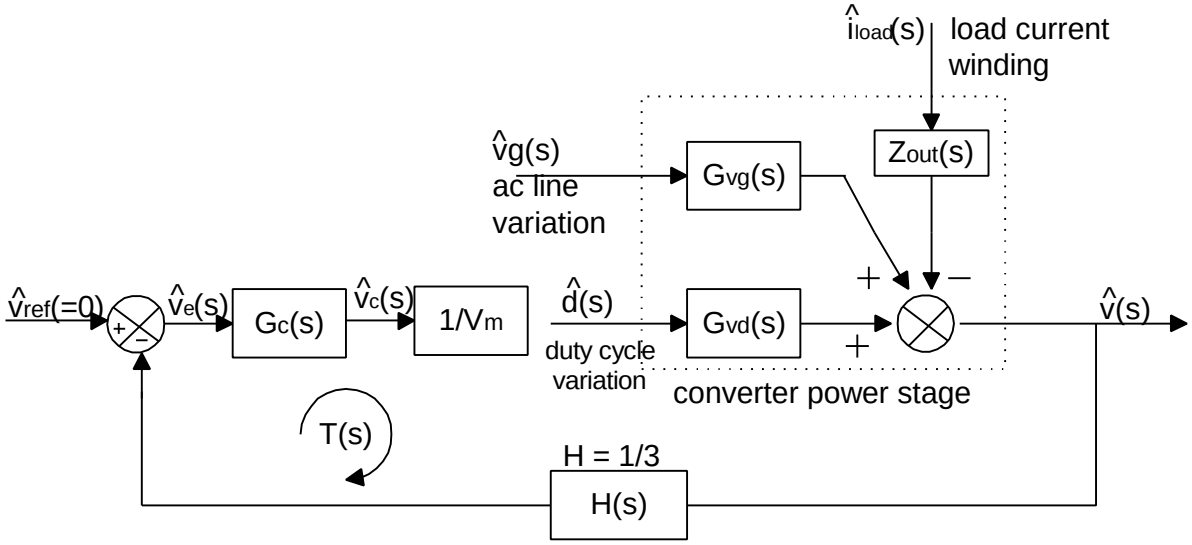
numerator of the expression.

$$Z_{out}(s)_{\text{open loop}} = R \| \frac{1}{SC} \| sL = \frac{sL}{1 + \frac{s}{w_o Q} + (\frac{s}{w_o})^2}$$

Q is high in all of the above - expect “Q peaking” in Bode plots

3. Closed Loop Conditions

Based on the existing G_{VD}, our design choice for G_c to achieve an even better T(s) and closed-loop response will be outlined below.



$$T(s) = G_c(s) \frac{1}{V_M} G_{vd}(s) H(s) = \frac{\frac{29}{12}}{1 + \frac{s}{w_o Q} + (\frac{s}{w_o})^2}$$

$$V_m = 4 \qquad G_{vd}(s) = \frac{29}{1 + \frac{s}{w_o Q} + (\frac{s}{w_o})^2} \qquad H(s) = 1/3$$

G_c(uncompensated) = 1.0 and T(s) uncompensated is just 1/12 $G_{vd}(s)$

Still Q is high in G_{VD}: Double pole located @ f_o

Gain decays at 40db/decade, which is a possible unstable case

Phase decays 180^o over the frequency span of the double pole.

We need to exactly specify the two frequency locations for the

phase asymptote plot. We employ the rule $f_{LOWER} = f_{o/}\ 10^{-1/2Q}$

$\frac{f_o}{10^{1/18}}$ = 900 Hz is the lower phase breakpoint. f_{HIGHER} =??

←--------100 Hz -------→ f_o = $10^{1/18}\ f_o$ = 1100

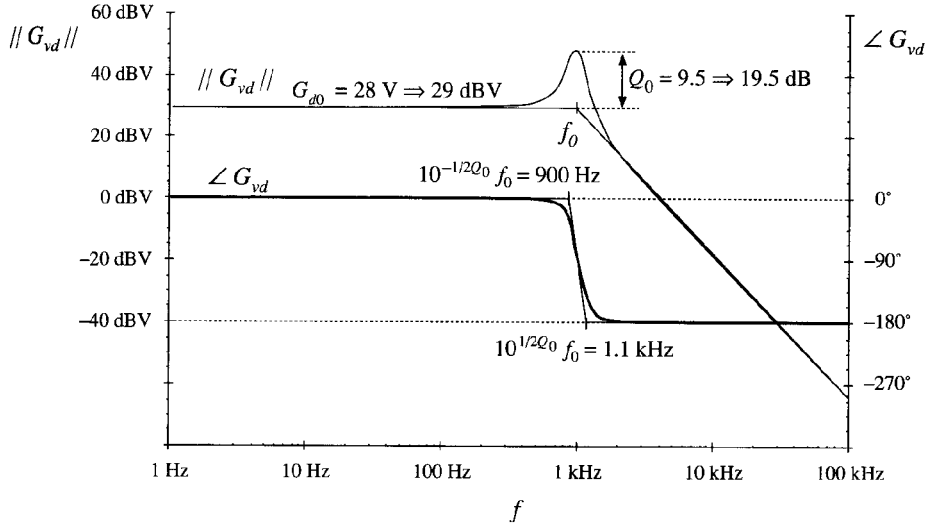
|←----------|----------→|

←-------100Hz----------→

$10^{-1/2Q}\ f_o$ 1000 $10^{+1/2Q}\ f_o$

low f onset pole location high f final

We judge from the Bode below that the phase margin of G_{VD} is not sufficient, and we will need compensation to achieve a new T(s) with better frequency response and more stable phase margin. G_{DO}= V/D= 28, $Q_O = R(C/L)^{1/2}$ =9.5 absolute=19.5 db



We will find that the issue of "Q peaking" in determining the f_C of T(s) is different from the case of " Q peaking" in G_{VD}(s). We note that f_C for G_{vd}(s) only follows the asymptote as Q has peaked much earlier and receded before T(s) crosses unity gain. Under this case of neglecting "Q peaking" we find the uncompensated T(s) crossover frequency to be set by G_{DO} and f_O

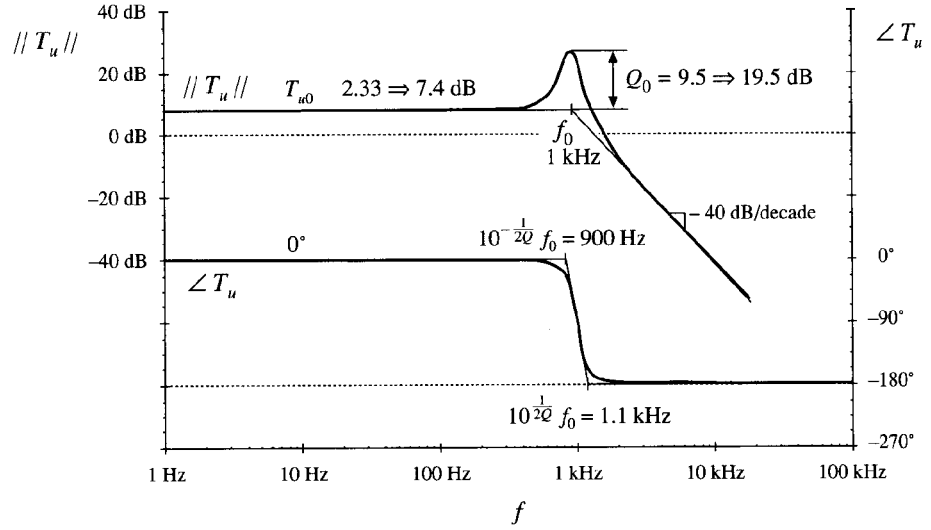
$G_{do}\ (\frac{f_o}{f})^2 = 1,\ f(\frac{G_{vd}}{1}) = \sqrt{G_{do}}\ f_o = 5.3KHz$

What do you expect to occur to f_C ,if we decrease the DC level?? This is what occurs when we form T(uncompensated).

T(s) uncompensated then basically follows G_{vd} with a scale factor.

G_{do} = 2.8V or 29db $\leftrightarrow$ It differs by $\frac{G_c}{V_m} H_s \leftrightarrow T_{uo}$ = 28/12 = 2.33

or 7.4 db. We have for the uncompensated loop gain the plot below. Please note that the DC coefficient T_{uo} =HV/ D V_M =7.4 db or 2.33 in absolute units, as described above



Determining f_c for T_μ from Bode plots above is much harder when including Q is peaking. Since T_{uo} is lower "Q peaking" is not negligable. f_C is harder to determine, as we need to "guesstimate" it by a cut and try approach.

First Guess without peaking could be way off

$$T_{vo} \left(\frac{f_o}{f}\right)^2 = 1, \quad f(\text{guess}) = \sqrt{2.33}\ f_o = 15\text{KHz}$$

Indeed f(with Q peaking as seen from the Bode plot with Q peaking) = 1800 Hz. Now that we know the uncompensated cross-over frequency we need to check the uncompensated phase margin to see if it needs a G_C network to tailor it into better shape.

By inspection at f_C=1.8 kHz, f_M= 5°. Is this good???

This value is barely positive and way off desired 76° (for conservative old man Collins) for a stable closed loop system.

Conclusion: $G_c(s)$ = 1 is not sufficient for this case! We need to design a G_C specific to the old T(s) to make it better for closed

loop operation.

4. Choose to design a PID compensator to achieve our goals on phase margin. There are other G_C as well**.**

a. Choose f_c of T(new) to be way below f_{sw} = 100 KHz.

$f_c = \frac{f_{sw}}{20}$ is an arbitrary choice but well below $f_{sw}/10$ for a slow old man. By the choice of f_C = 5 kHz we are limiting the dynamic response. We could choose f_C as high as $f_{SW}/5$ =25 kHz

b. We now calculate at 5 kHz the value of

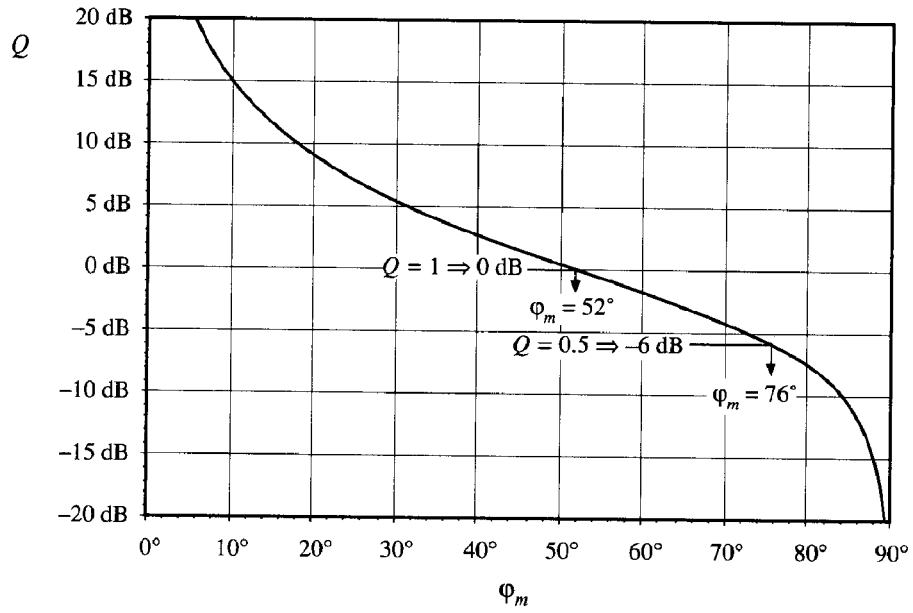
$T(\text{uncompensated}) = 2.33(\frac{f_o}{f})^2 = .09$ @ 5KHz

T_u(@5KHz) = .09 or -20.6 db This means our G_C design will have to take this into account when we design for the target f_C.

$\Rightarrow G_c$ (5 KHz) must be +20.6 db. Now is the time to step up to the plate and actually DECIDE the value of the phase margin we want. Recall this is a trade off between stability and transient response.

$\phi_m = 52^o$ is a more aggressive choice and also corresponds to the border between overdamped and under damped

For $\phi_M = 52^o$ we need to insure $\frac{f_p}{f_z} \approx 10$, and for a compromise Q peaking we have Q = 1.0 , which only peaks at 1.16 or 16% over the DC level we expect in steady state. This may be too much for some loads. The customer decides. The load could also take a lot more overload. If so then we could speed up the dynamic response as well. The well worn Q versus phase margin chart is given on the top of page 16.



We need to choose one pole and one zero location.
Given $\phi_m = 52°$ for the PD portion of the PID controller as our goal

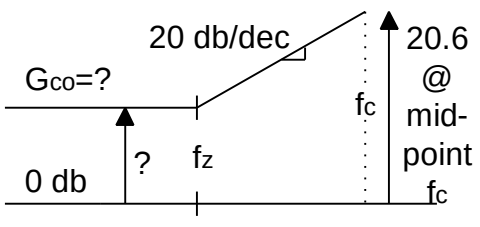
$$f_z = 5\sqrt{\frac{1-\sin 52}{1+\sin 52}} = 1.7\text{KHz}$$

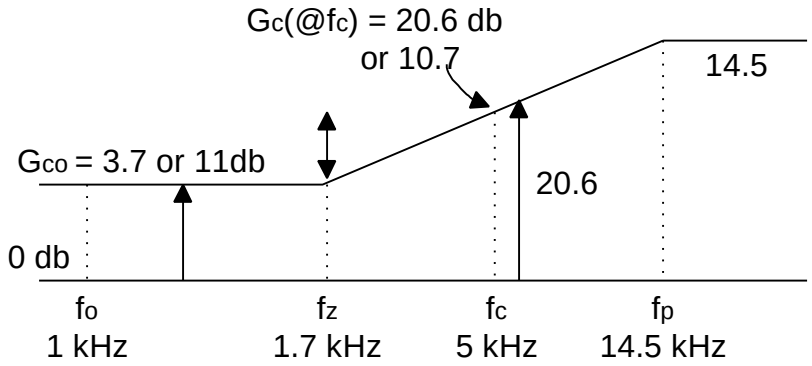
$$f_p = 5\sqrt{\frac{1+\sin 52}{1-\sin 52}} = 14.5\text{KHz}$$ Which is also low compared to f_{sw} (100 KHz) and within the gain-bandwidth product of the op-amp chosen for the task.

$$G_c(s) = G_{co}\frac{(1+s/w_z)}{(1+s/w_p)}$$

Choose G_{co} such that overall gain at chosen f_c of the compensated $T_c(f_c)$ is unity. That is don't change the unity cross-over gain by this portion of the G_C network.

$T_c(s) = G_c(s) * T_u(s)$
↓ ↓
want +20.6db @5 KHz added -20.6 db @5 KHz



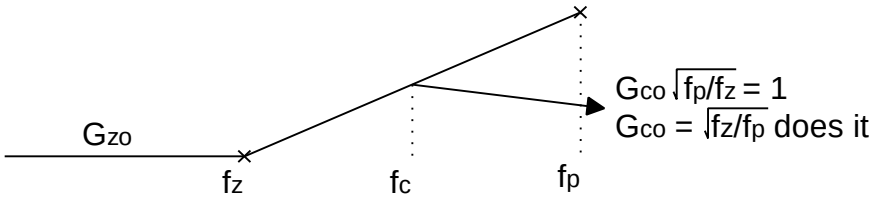


The zero adds some gain so we have to account for this as well and realize the difference must come from G_{CO}. Use the 20 db/ decade rule to determine the inverted zero gain from f_Z to f_P

$$f_c = \sqrt{f_z f_p} \qquad G_c(f = f_c) = G_{co}\sqrt{\frac{f_c}{f_z}} = G_{co}\sqrt{\frac{f_p}{f_z}}$$

G_{co} = 3.7 or 11.3 db

Considering <u>$G_c(s)$ alone</u> and asking for unity gain @ f_c

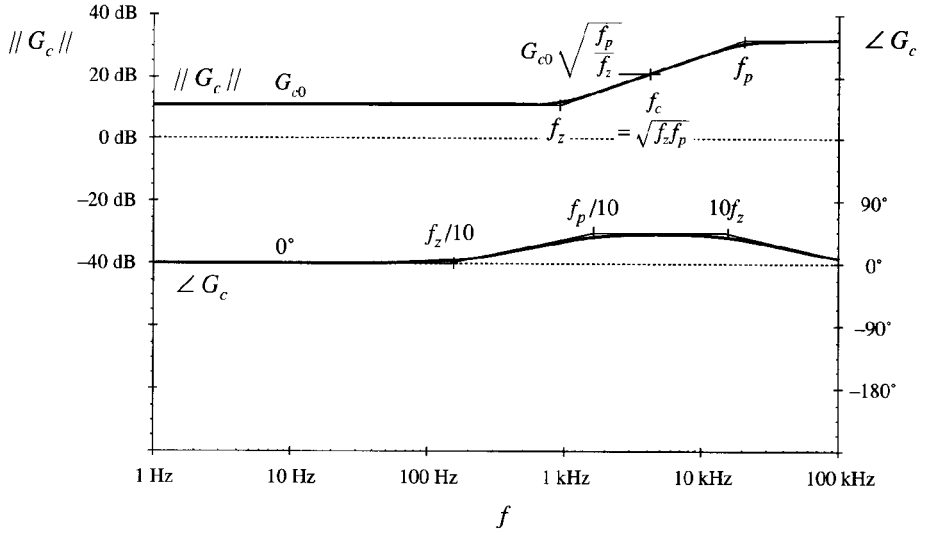


However with $T_c = T_u G_c$. T_u is reduced from f_o to f_cThe value of G_{CO} value becomes:

$$G_{co} = \frac{1}{T_{vo}\left(\frac{f_o}{f_c}\right)^2}\sqrt{\frac{f_z}{f_p}} = \left(\frac{f_c}{f_o}\right)^2 \frac{1}{T_{vo}}\sqrt{\frac{f_z}{f_p}}$$

G_{co} = 3.7 or 11.3 db

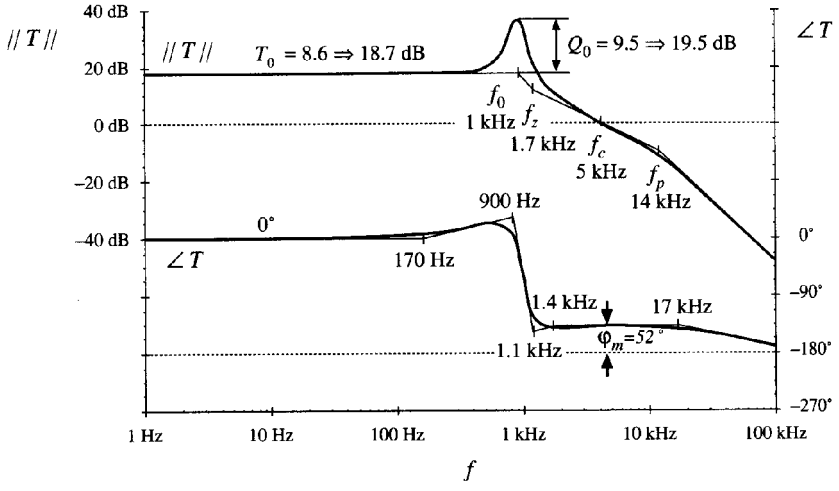
In summary: 52^o of phase margin is provided to the new T(s) over the frequency range $\frac{f_p}{10} \le f \le 10 f_z$



The PD compensated T(s) is then:

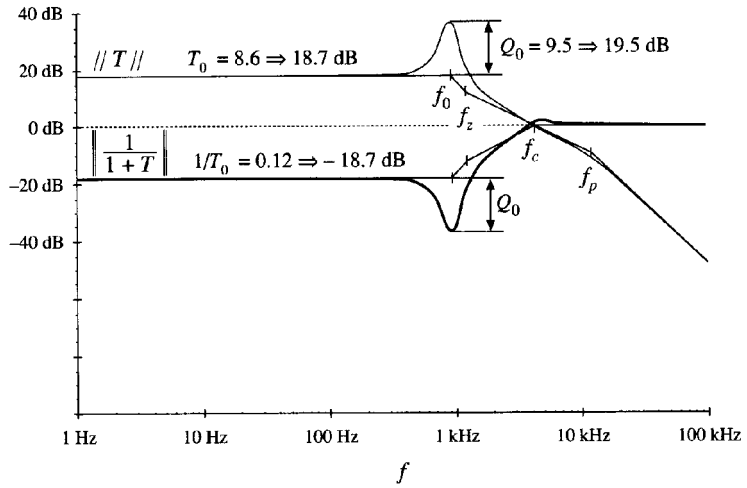
$$T_c(s) = \frac{T_{vo}\ G_{co}\ (1+s/w_z)}{(1+s/w_p)\left[1+\frac{s}{w_o Q}+\left(\frac{s}{w_o}\right)^2\right]}$$

$T_{vo}\,G_{co}$ = 8.6 absolute or 18.7 db. Q remains 9.5 db in the "Q peaking" effects in the Bode plot. Tc(s) Bode plot is then as shown below. Note at once the target phase margin is hit.



ϕ_m is 52° much improved and the f_C target for the compensated T(s) we chose is met. **For HW #4 repeat the problem to here with at target f_C=15 kHz.**

Use algebra-on-graph to get T/1+T from T(compensated)



For f < 1 KHz the 1/(1+T) factor reduces both Z_o and $\frac{\Delta V_o}{\Delta V_g}$ }by 18.6 db or 8.6. This is another improvement due to PD compensation. Let's quantify the improvement. G_{vg} (open loop) = D(the DC duty cycle). Therefore

$\frac{\Delta V_o}{\Delta V_g} \sim 0.536 \Rightarrow \Delta V_g$ 1V gives $\Delta V_o = .536\,V$

Which is clearly unacceptable when the mains, V_g clearly varies a lot more than that on occasion. The 1/(1+T) factor makes

G_{vg}(closed loop) = $\frac{D}{1+T} = \frac{.536}{8.7} = .062 \Rightarrow \Delta V_o = 62$ mV

$\Rightarrow \Delta V_g$ 1V

Let's futher <u>improve</u> this low f behavior even further by adding to G_c an inverted zero at f_L. This is the PI portion of the full G_C

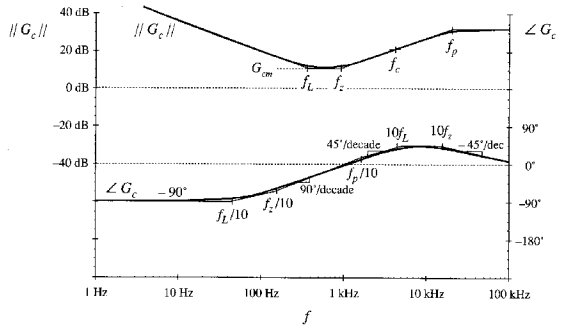
A Newer and more improved $G_c(s)$ would look like:

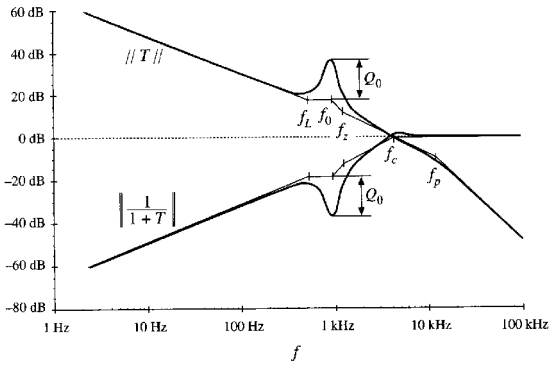
$$G_C(s) = G_{cm}\left(\frac{1+s/w_z}{1+s/w_p}\right)\left(1+\frac{w_L}{s}\right)$$ Note the inverted zero

↓ PD ↓ Added PI portion to G_C

To the old P.D. compensation we simply added a PI section. Choose the same G_{co} = 3.7absolute$\Rightarrow$ 11.3 db f > f_L the loop gain is unchanged but for f < f_L the loop gain is increased. Arbitrarily choose the location of the inverted zero $f_L = f_c/10$ so it doesn't contribute any phase to ϕ_M at f_c which we are now happy with.

G_c G_c Bode T and 1/1+T, Q = 1 db for 52°





We add inverted zero to PD without changing DC gain or f_C. G_{co}(100Hz) is improved by an inverted zero located at 500Hz. G_c increases at 100 Hz by the ratio(from the 20 db/decade slope) of 500/100 = 5 in absolute terms. This is 5x lower Z_{OUT} and G_{VG} variations than PD compensation alone! Let's look at details. Again use algebra-on-graph to get the variation versus frequency from the product of [G_{vg}] and 1/ (1+T) for PID compensation:

G_{vg} (open loop) & 1/1+T

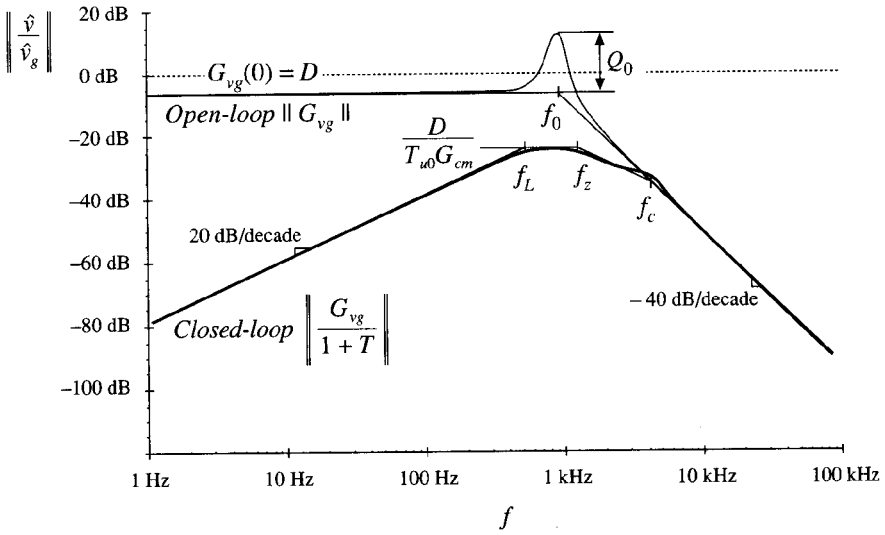
$\downarrow$ | $\downarrow$

$$\frac{D}{1 + \frac{s}{Q w_o} + \left(\frac{s}{w_o}\right)^2}$$ | above f_c = 1

Q effect $\uparrow$ at f_o | Q effect $\downarrow$ at f_o

Poles and Q of G_{vg} $\leftarrow$ cancel $\rightarrow$ Zeros and Q of 1/1+T

$\Rightarrow$ Q effects are all <u>gone</u> in G_{vg} (closed loop)x 1/(1+T)



We also see at what frequencies where the benefits of the 1/(1+T) factor are not so large.