31 July 2003

Xilinx Project Navigator Reference Guide

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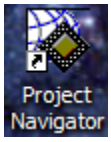
Background: This guide provides you with step-by-step procedures in using the Xilinx Project Navigator to perform the following:

- Synthesize your Very High speed Integrated Circuit Hardware Description Language (VHDL) code to a netlist
- Map, place and route your netlist onto a Spartan II FPGA (which is used on the XESS XSA-50 Field Programmable Gate Array (FPGA) protoboard
- Map Input/Output (I/O) pins to devices on the XESS XSA-50 FPGA protoboard.
- Generate a bit stream so the design can be downloaded onto the Spartan II FPGA residing on the XESS XSA-50 FPGA protoboard.
- Finally, although the downloading utility is NOT apart of the Xilinx Project Navigator, the steps to download the design are also provided here.

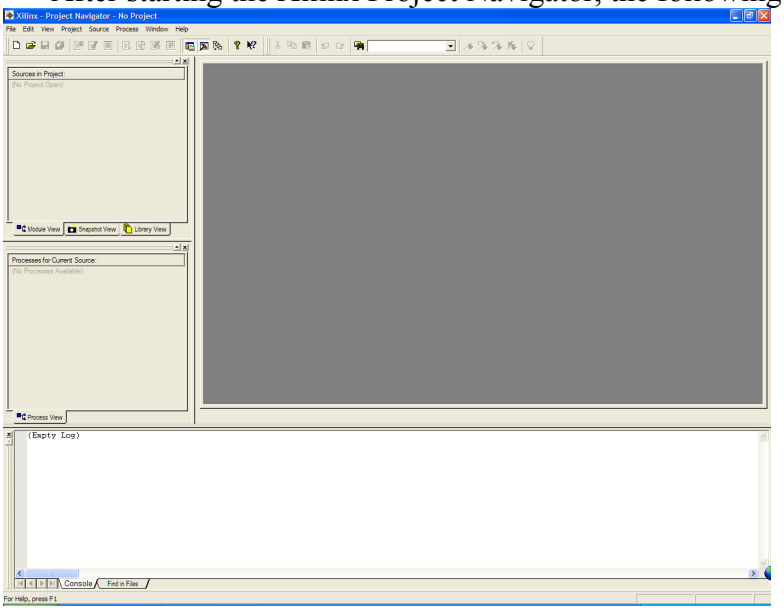
Assumption: Students have a basic understanding of Windows

Procedures:

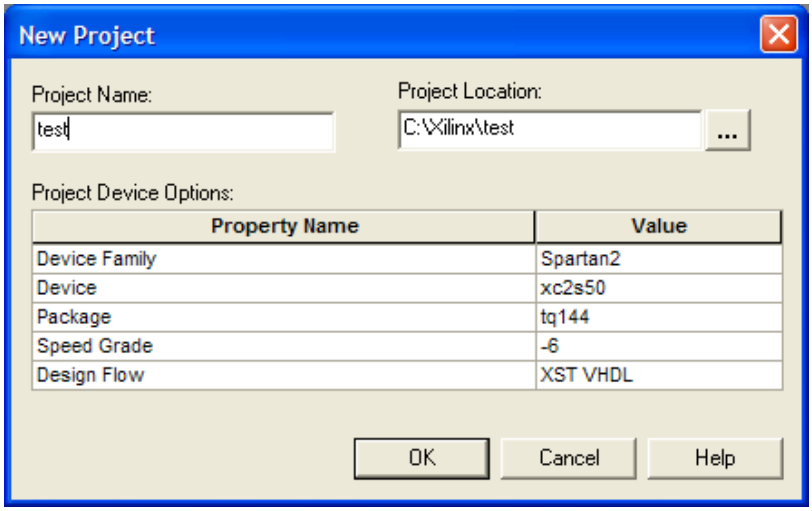
1. To Start the Xilinx Project Navigator,
   Start > Engineering Applications > Xilinx ISE 5 > Project Navigator
   or using the following icon:



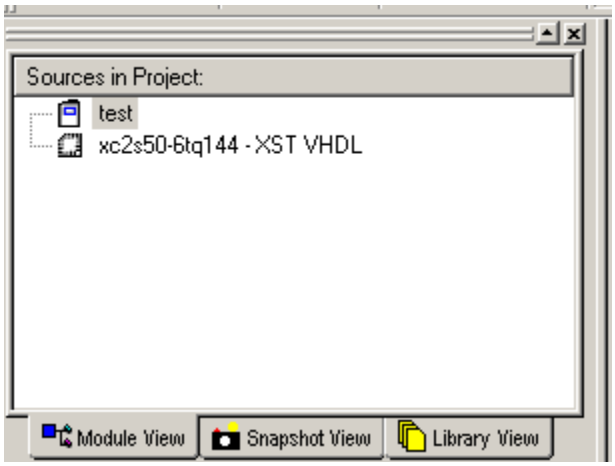
2. After starting the Xilinx Project Navigator, the following screen will be displayed:



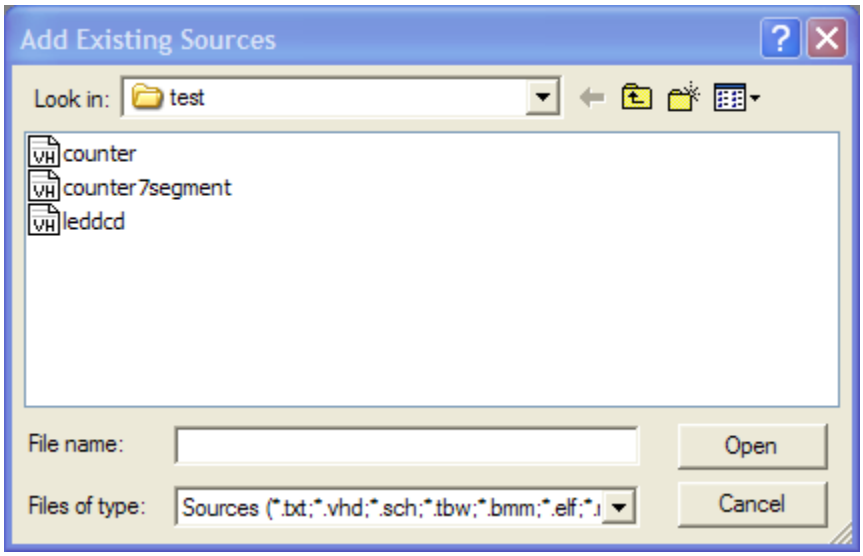
3. You must create a new project, if you have not done this step before. From the Xilinx Project Navigator main menu select File > New Project. The window displayed below will be displayed. You must enter a new project name. In this case, "test" was used. The Device Family, Device, Package used for the XESS XSA-50 FPGA protoboard is provided. The speed grade characterizes the type of performance you require. You can opt for a speed grade of –5 (standard performance or speed grade –6 (higher performance). Speed grade –5 should suffice. For the Design Flow, if using VHDL as your source, select XST VHDL from the pull-down menu or if using Verilog as your source, select XST Verilog from the pull-down menu. Press OK.

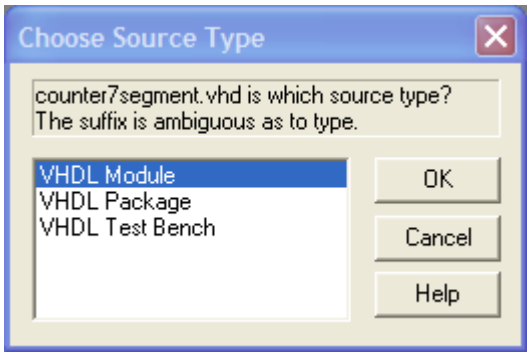


4. After you have completed step 3, the following screen will be display with your device in the upper left hand corner of "Sources in Project" Window.

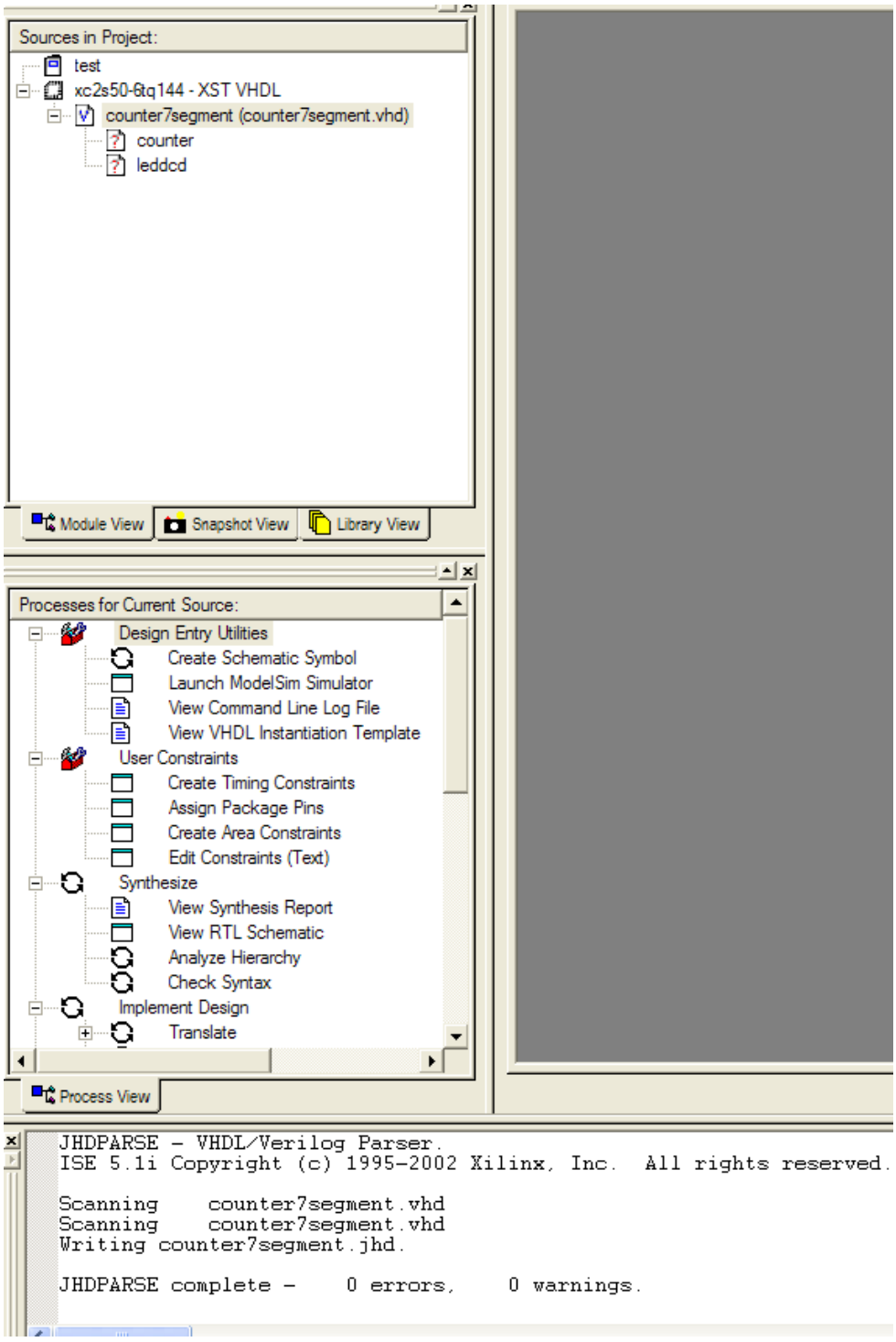


5. At this point you should make sure your already compiled and simulated VHDL source code is located in the directory you created in step 3. Next you need to add your source code to the project. In the "Sources in Project" window, left click on the line where XC2s50 –5tq144-XST VHDL (or XC2s50 –6tq144-XST) is located to highlight that entry. Using the pull-down menu (or alternatively the right mouse click) select Project > Add Source. Now enter your source code through the "Add Existing Sources" window by highlighting the desired source code and pressing "Open". Note if you are using a hierarchical design, enter the high level module first. You may be asked to clarify what is the source via the "Choose Source Type" window. Make sure VHDL Module is highlighted and press OK.

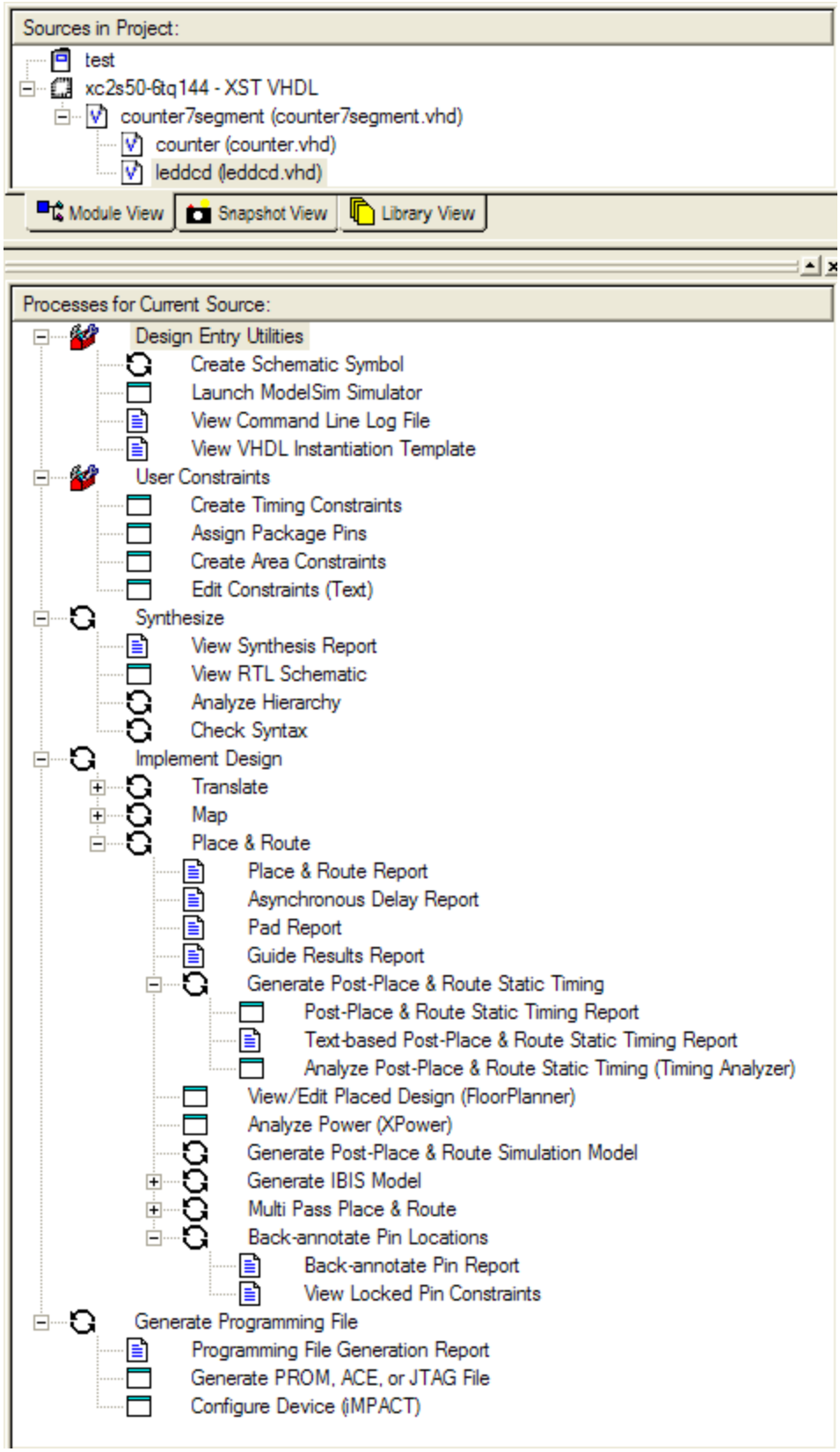




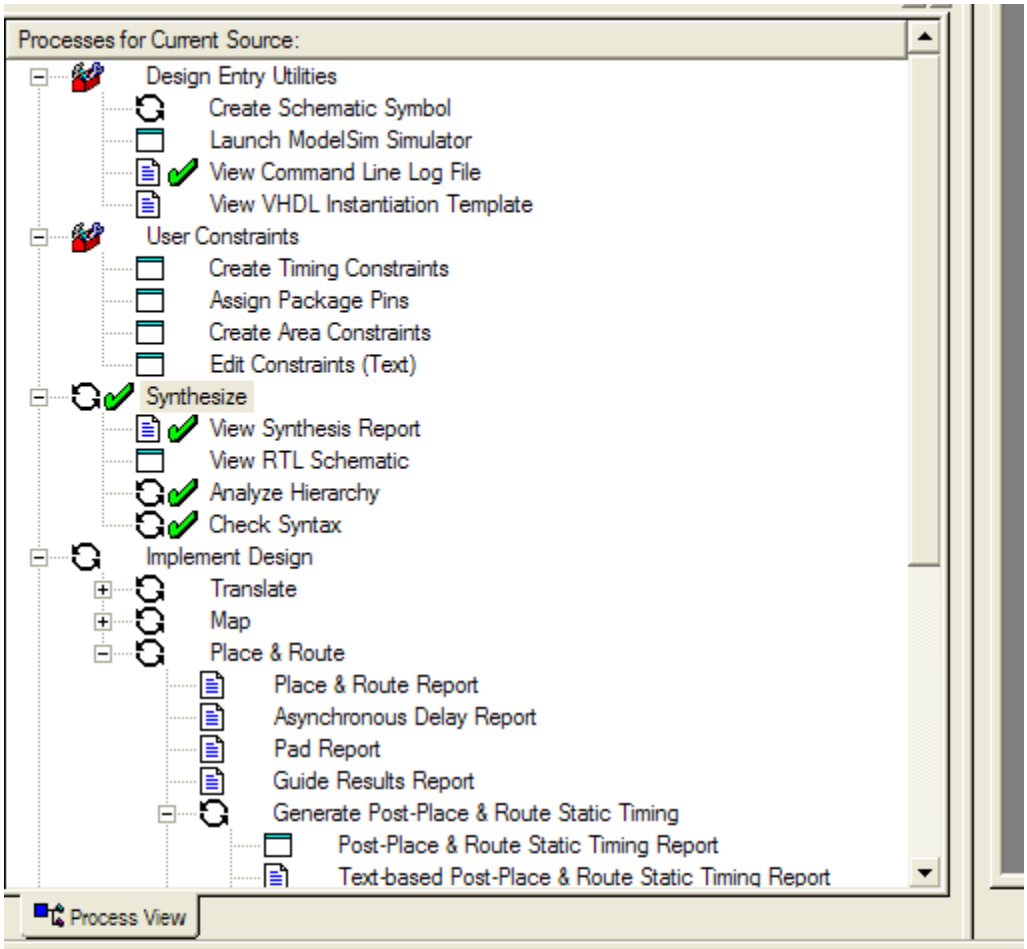
6. Xilinx Project Navigator will load your design and the windows will look something similar to what is illustrated below. It should be noted that the example used in this tutorial is a hierarchical design. It has an ARCHITECTURE block with two components (counter & leddcd). The high-level ARCHITECTURE is defined in the file counter7segment.vhd. If using a hierarchical design, the other files must be added. Repeat step 5, but highlight each component to load its associated VHDL file. If you successfully complete this action, there will be "check" marks to the left of your design name(s)

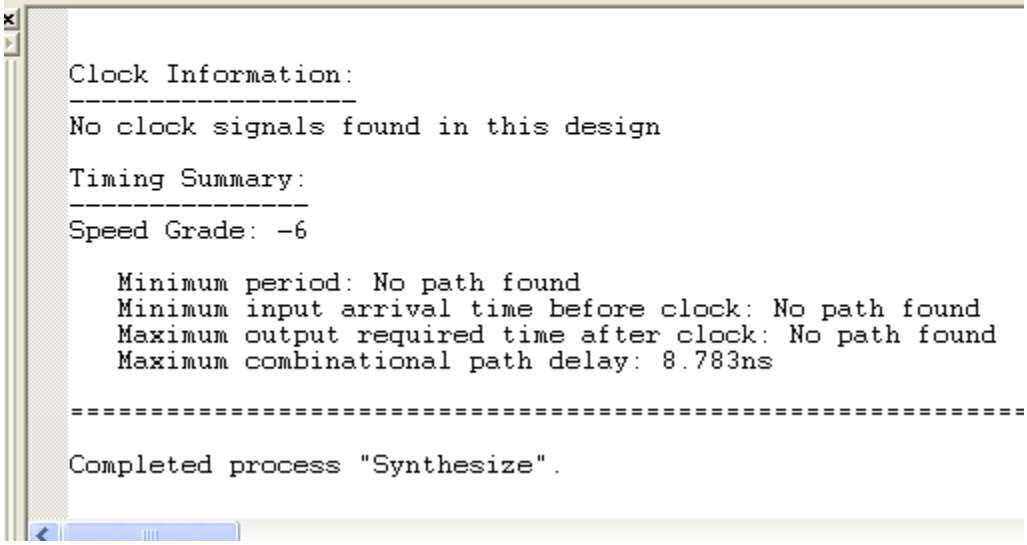


7. Now you are ready to synthesize your design to make a netlist. To begin with the options of the "Processes for Current Source Window" is provided below.

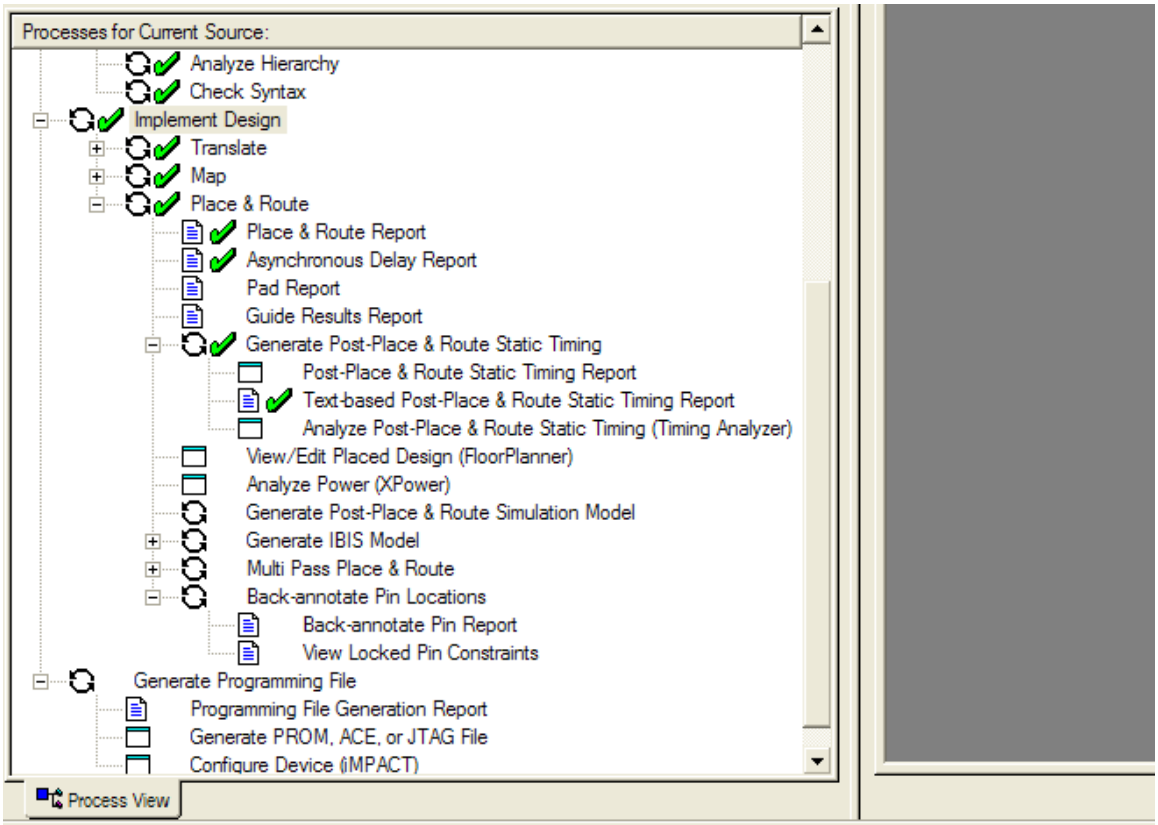

Sources in Project:
test
xc2s50-6tq144 - XST VHDL
counter7segment (counter7segment.vhd)
counter (counter.vhd)
leddcd (leddcd.vhd)
Module View
Snapshot View
Library View
Processes for Current Source:
Design Entry Utilities
Create Schematic Symbol
Launch ModelSim Simulator
View Command Line Log File
View VHDL Instantiation Template
User Constraints
Create Timing Constraints
Assign Package Pins
Create Area Constraints
Edit Constraints (Text)
Synthesize
View Synthesis Report
View RTL Schematic
Analyze Hierarchy
Check Syntax
Implement Design
Translate
Map
Place & Route
Place & Route Report
Asynchronous Delay Report
Pad Report
Guide Results Report
Generate Post-Place & Route Static Timing
Post-Place & Route Static Timing Report
Text-based Post-Place & Route Static Timing Report
Analyze Post-Place & Route Static Timing (Timing Analyzer)
View/Edit Placed Design (FloorPlanner)
Analyze Power (XPower)
Generate Post-Place & Route Simulation Model
Generate IBIS Model
Multi Pass Place & Route
Back-annotate Pin Locations
Back-annotate Pin Report
View Locked Pin Constraints
Generate Programming File
Programming File Generation Report
Generate PROM, ACE, or JTAG File
Configure Device (iMPACT)

To synthesize your design, double left click on “Synthesize” in the “Processes for Current Source:” window or right click on “Synthesize” and select “Run” or “Rerun” (the latter instructions will depend on whether or not you have selected to synthesize your design on an earlier occasion). The following will result:



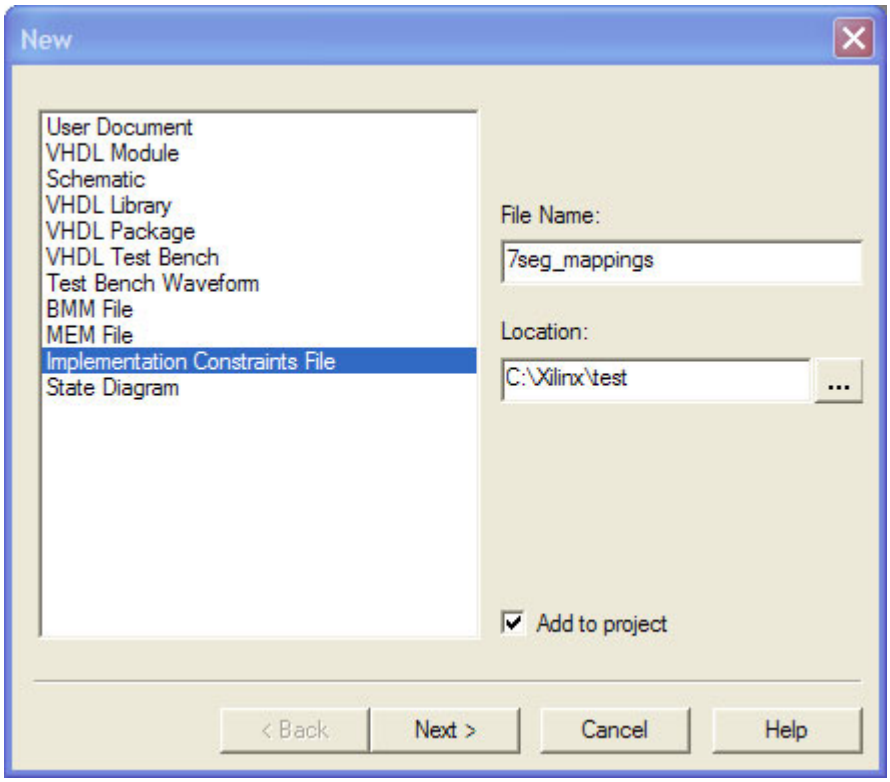


7. Now you are ready to route, place and map your netlist onto a Spartan II FPGA (which is used on the XESS XSA-50 FPGA protoboard). To route, place and map your design, double left click on “Implement Design” in the “Processes for Current Source:” window or right click on “Implement Design” and select “Run” or “Rerun” (the latter instructions will depend on whether or not you have selected to route, place and map your design on an earlier occasion). The following will result:

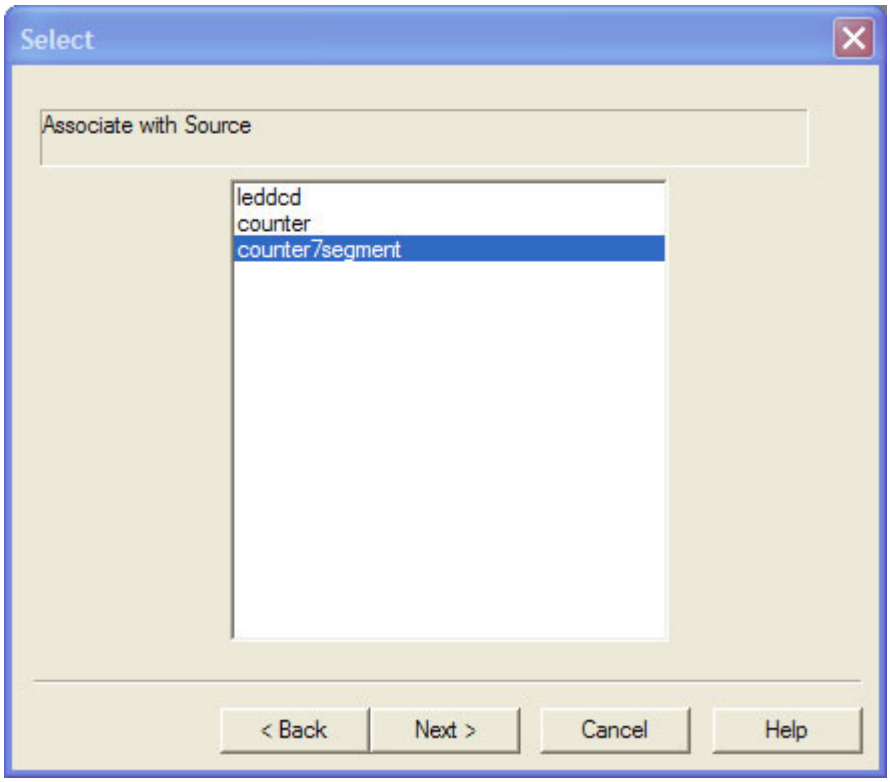



```
Started process "Generate Post-Place & Route Static Timing".


Loading device database for application trce.exe from file "leddcd.ncd".
   "leddcd" is an NCD, version 2.37, device xc2s50, package tq144, speed -6
Loading device for application trce.exe from file 'v50.nph' in environment
C:/Xilinx.

Analysis completed Sat Jul 19 13:15:00 2003
--------------------------------------------------------------------------------

Generating Report ...


Completed process "Generate Post-Place & Route Static Timing".

Place & Route Module leddcd . . .
PAR command line: par -w -ol 2 -t 1 leddcd_map.ncd leddcd.ncd leddcd.pcf
PAR completed successfully
```

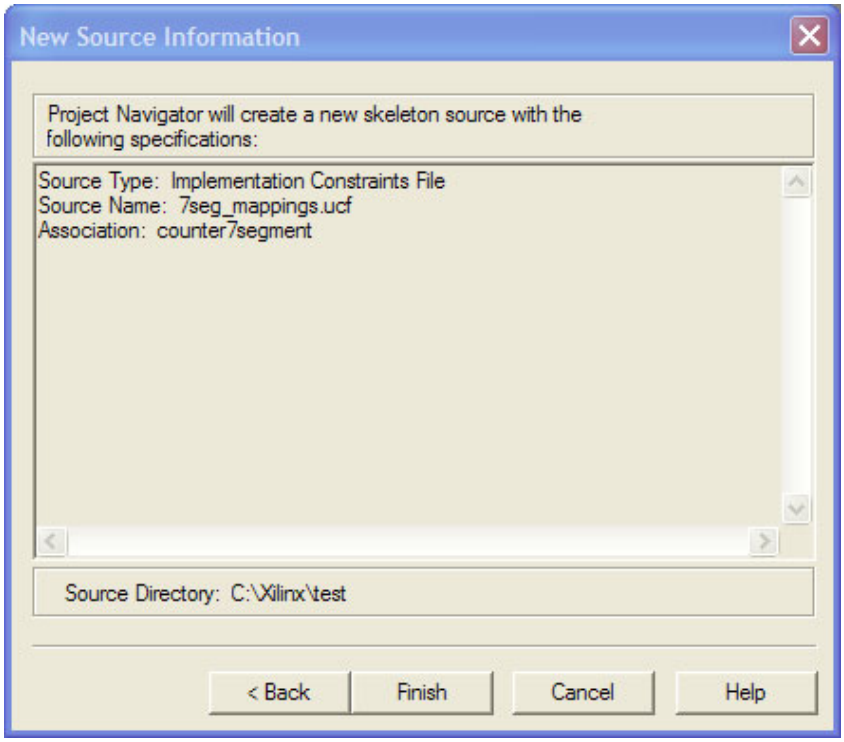
8. Before you generate your bit stream to download onto the FPGA, you must first define your I/O to be used on the XESS XSA-50 FPGA protoboard. The pin definitions for various I/O devices used in EE451 can be found in the EE451 website under Tips > XESS Corporation FPGA Protoboard > I/O Pin Mappings. In this particular example, we will define the clock input and outputs to a 7-segment display. First we must attach an implementation or user constraints file (or *.ucf file) to the XC2s50 –5tq144-XST VHDL (or XC2s50 –6tq144-XST) definition of the FPGA. To do this, highlight the XC2s50 –5tq144-XST VHDL (or XC2s50 –6tq144-XST) in the "Sources in Project:" window. Using the pull-down menu (or alternatively the right mouse click) select Project > New Source. A "New" window will be displayed as illustrated below. Highlight the "Implementation Constraints File" entry and enter a name of your implementation constraints file. Press "Next".



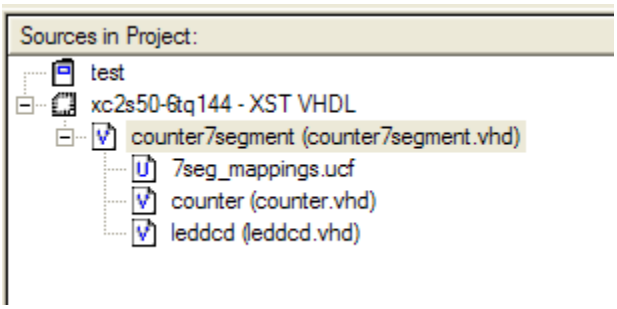
In a hierarchical design, select you top-level source code filename as illustrated below and press “Next”.



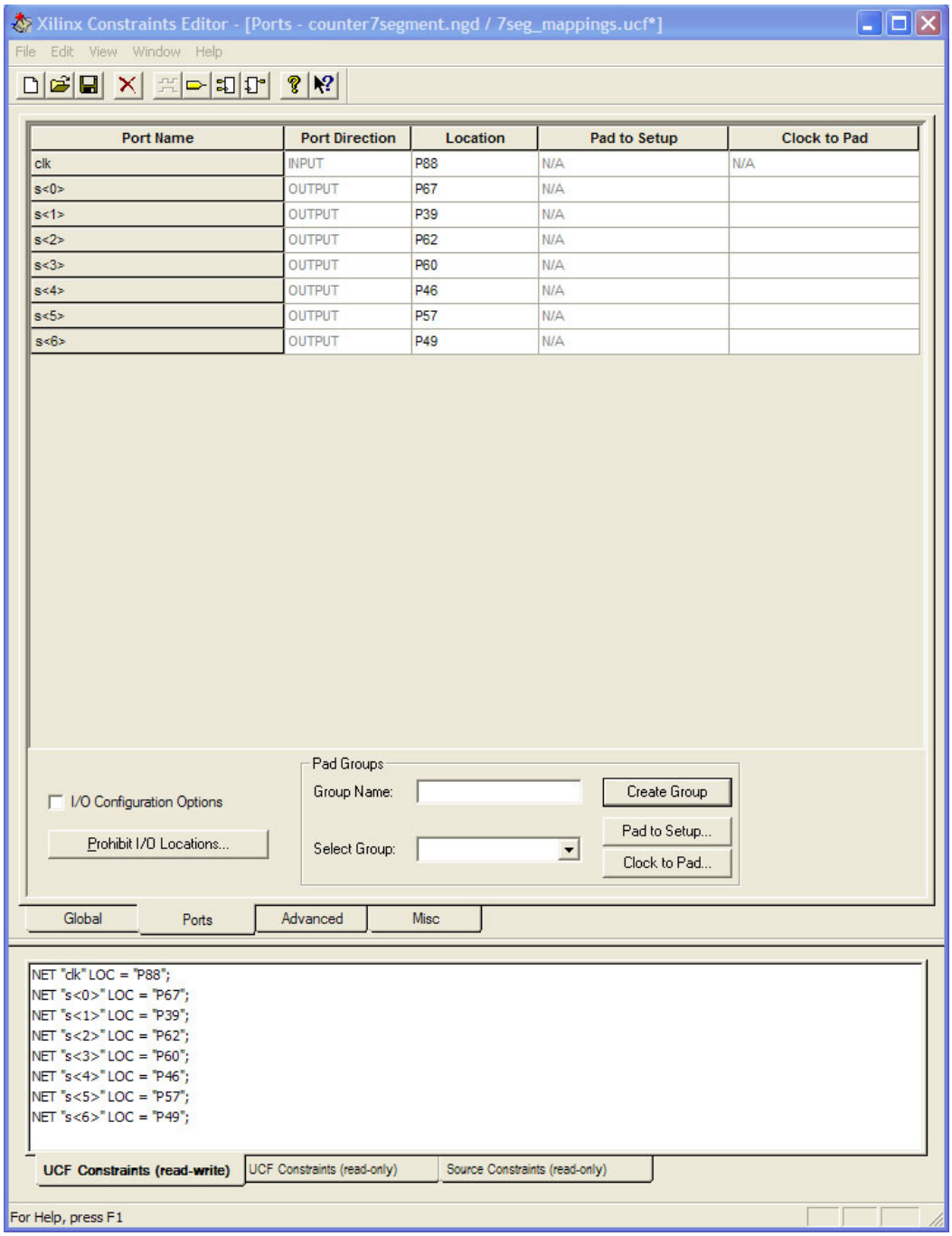
The following screen will be displayed. Simply press “Finish”.



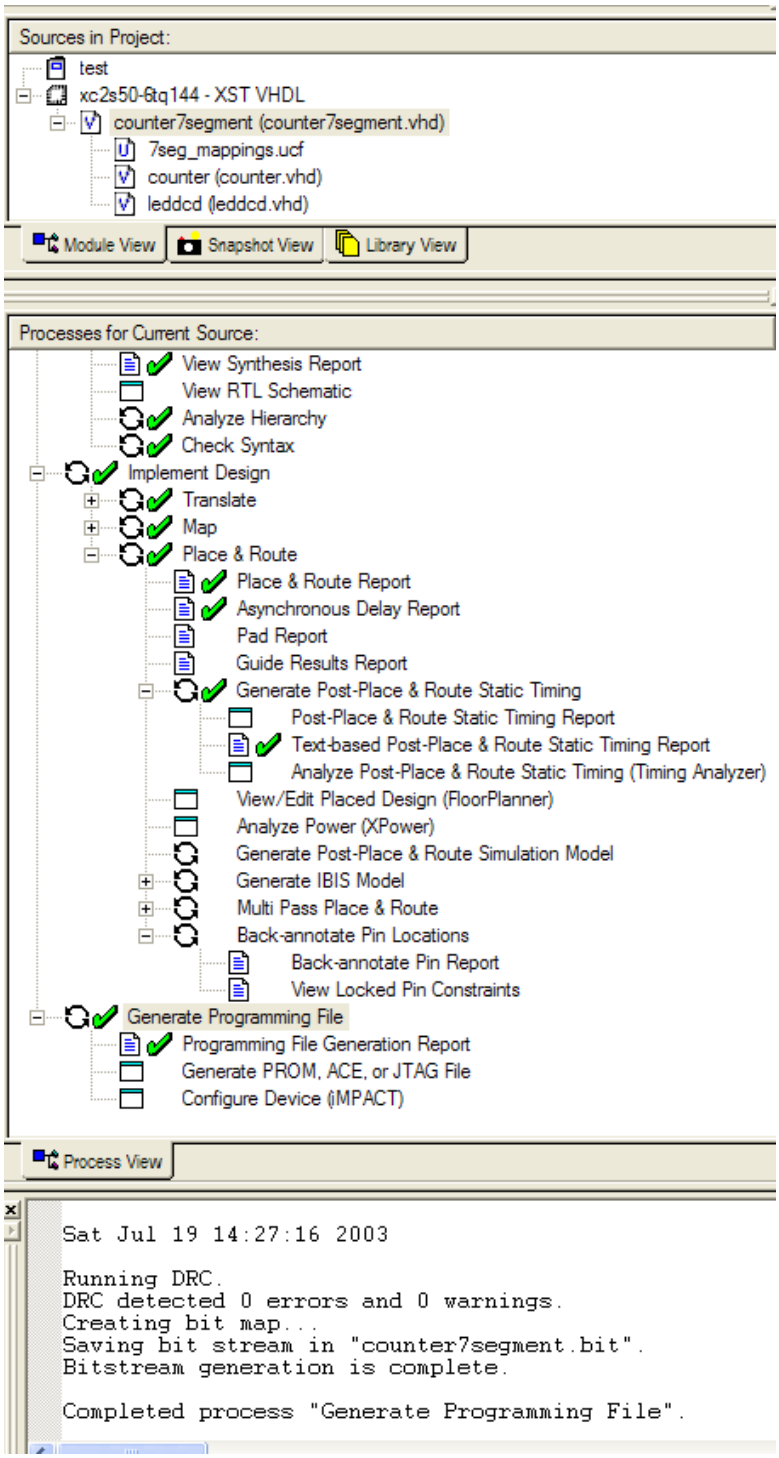
In the “Sources in Project:” window the *.ucf file is now added to your design.



Make sure you highlight your top-level design in the “Sources in Project:” window. In the “Processes For Current Sources:” window, double click on the following application: User Constraints > Create Timing Constraints. The “Xilinx Constraints Editor” Window will be displayed. Ensure you have the “Ports” tab selected. You can enter the I/O to/from your FPGA as being used on the XESS XSA-50 FPGA protoboard. Ensure you enter a “P” for pin before each pin number. The results are shown below. Make sure you save the mappings to the *.ucf file that you just created for possible future use. In the “Xilinx Constraints Editor” pull-down menu, select File > Save. If you use this file in the future, you do not need to create it as in step 8. All you do is “add” the *.ucf file to your design. Additionally, since the route, place and map procedures done in step 7 mapped I/O without a user constraints file, you may have to repeat step 7 with the user constraints file that you just created.

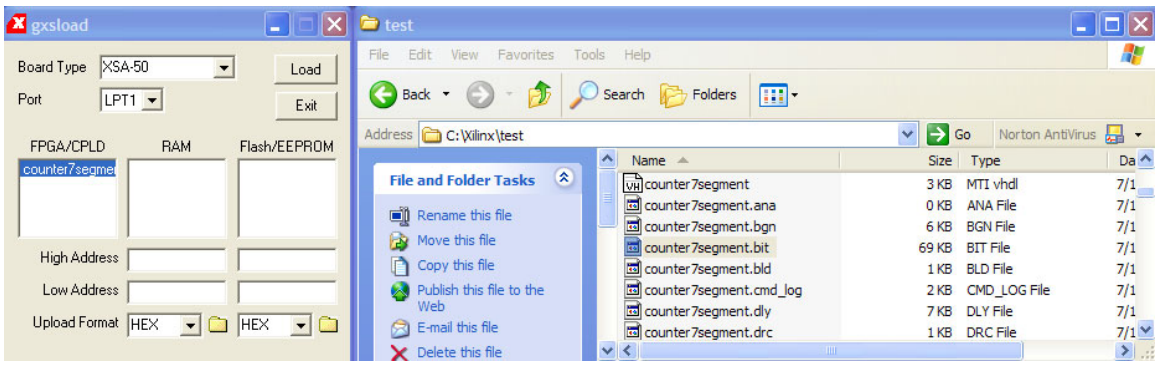


9. Now you are ready to create the bit stream to be downloaded to the XESS XSA-50 FPGA protoboard. Ensure your design is selected in the "Sources in Project:" window. In the "Processes for Current Source:" window, double left click on "Generate Programming File" or right click on "Generate Programming File" and select "Run" or "Rerun" (the latter instructions will depend on whether or not you have selected to create a bit stream on an earlier occasion). The following will result:


Sources in Project:
test
xc2s50-6tq144 - XST VHDL
counter7segment (counter7segment.vhd)
7seg_mappings.ucf
counter (counter.vhd)
leddcd (leddcd.vhd)
Module View
Snapshot View
Library View
Processes for Current Source:
View Synthesis Report
View RTL Schematic
Analyze Hierarchy
Check Syntax
Implement Design
Translate
Map
Place & Route
Place & Route Report
Asynchronous Delay Report
Pad Report
Guide Results Report
Generate Post-Place & Route Static Timing
Post-Place & Route Static Timing Report
Text-based Post-Place & Route Static Timing Report
Analyze Post-Place & Route Static Timing (Timing Analyzer)
View/Edit Placed Design (FloorPlanner)
Analyze Power (XPower)
Generate Post-Place & Route Simulation Model
Generate IBIS Model
Multi Pass Place & Route
Back-annotate Pin Locations
Back-annotate Pin Report
View Locked Pin Constraints
Generate Programming File
Programming File Generation Report
Generate PROM, ACE, or JTAG File
Configure Device (iMPACT)
Process View
Sat Jul 19 14:27:16 2003
Running DRC.
DRC detected 0 errors and 0 warnings.
Creating bit map...
Saving bit stream in "counter7segment.bit".
Bitstream generation is complete.
Completed process "Generate Programming File".

10. Now you are ready to download your bit stream onto the XESS XSA-50 FPGA protoboard. To accomplish this, we must use the XESS GXSLOAD utility. The utility can be found in
Start > Engineering Applications > XESS > GXSLOAD
or using the following icon:

The following application will be started for download. Use the "My Computer" windows feature to go to the subdirectory where your subdirectory you created in step 3 is located. Simply drag the *.bit file into the FPGA/CPLD of the GXSLOAD utility. Now press "Load". The bit stream will be downloaded onto the XESS XSA-50 FPGA protoboard.



11. Now you can demonstrate that your design is properly working.

Helpful Tools Associated with Xilinx Project Navigator:

In the "Processes for Current Source:" window there are some utilities and reports that can help you with your design.

1. To observe where your signals were mapped onto the FPGA, your can look at the PAD Report. This can be found at Implement Design > Place & Route > Pad Report

2. Once your constraints file is created, instead of using the Xilinx Constraints Editor, you can simply edit the results. This can be done by executing User Constraints > Edit Constraints (Text) or you can go back to the Xilinx Constraints Editor by executing User Constraints > Create Timing Constraints