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Force File and Force Commands

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Background: You can manually simulate your circuit design in Mentor Graphics' ModelSim or QuickSim with force commands. However, using a file that has a series of test vectors is more efficient to test your design. This file is also referred as a "force file" consisting of force commands. This will eliminate manually re-entering test vectors as you debug your VHDL code or your schematic in Design Architect.

References: (a) Defining Test Input Stimuli (Forces), David M. Zar, http://users.ece.gatech.edu/~schimmel/cmpe4500/vhdl.html

The following is a sample of "force commands" that could be included in your text file:

Command	Explanation
force a 0	set a single input variable "a" to logic 0
force b 1 30	set a single input variable "b" to logic 1 at time T + 30ns
force d "00" 0	Give the value 00 at time 0 to signal d. Notice that signal d is a two-bit vector.
force clk 0 0, 1 20 –repeat 40	**Use with ModelSim**. Creates a clock waveform on signal "clk" with period 40, with value 0 for the first half and 1 for the last half. Reference (a).
force clk 1 0, 0 5 –repeat 10	**Use with ModelSim**. Creates a clock waveform on signal "clk" with period 10, with value 1 for the first half and 0 for the last half. Reference (a).
force c 1 0, 0 10, 1 20	**Use with ModelSim.** Give the value 1 at time 0 to signal c, at time 10 give a value of 0 and at 20 give a value of 1. c will have a value of 1 after 20ns. Reference (a).
run 50	This tells the simulator to run the design for 50ns. You can observe all the new values in "wave" & "list" windows.
force clk 0 0 –repeat force clk 1 50 –repeat	**Use with QuickSim.** These two commands, in concert with one another**,** create a clock waveform with value 0 at 0ns and value 1 at 50ns. The period is 100ns.

Notes:

1. To call your "force file", enter the following in ModelSim (VHDL):
   `Select Macro > Execute Macro then select your force file`

2. To call your "force file", enter the following in QuickSim II (Schematic):
   - Select signals (to trace on your design sheet)
   - Select "TRACE" in "Stimulus" window
   - In the "TRACE" window, right click the mouse
   - In the "QuickSim" pop-up window, select
     Force > From File Enter the ***forcefilename***

Let's assume you created a VHDL to simulate an AND gate. A sample force file that you created using an editor may look like (to test all the combinations):

```
force a 0
force b 0
run 10
force a 0
force b 1
run 10
force a 1
force b 0
run 10
force a 1
force b 1
run 10
```