ECE 331: Electronics Principles
I Fall 2014

Lab #3: MOSFETs Characterization

Pre-lab due on Thursday, Oct. 16, before noon

Pre-lab

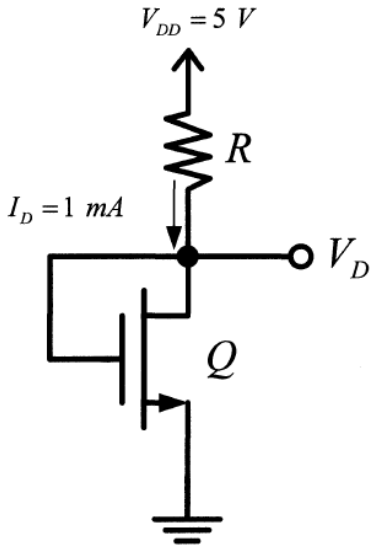
A. Draw both the large and small signal models for NMOS transistors. Sketch I_D vs V_{DS} characteristics for several values of V_{GS} and graphically illustrate the Channel Length Modulation effect.

B. List the difference between NMOS and PMOS transistors. Draw a schematic of each one, Labeling all relevant voltages and currents. What is an advantage of using a PMOS? What is a drawback? (Hint: Consider the response time)

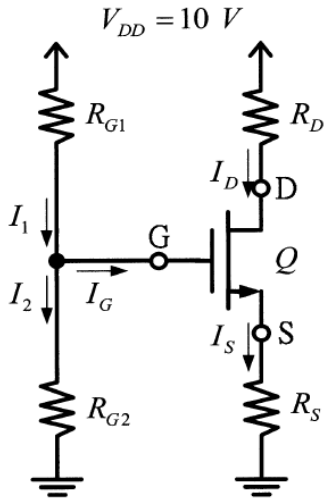
C. For an NMOS transistor with threshold voltage Vt = 0.62 V, Kn' = 0.167mA/V^2, here Kn' is defined to be equal to $\mu_n C_{ox}$, If Vover-drive is 0.25 V, W = 0.55 μm and L = 0.18 μm, answering the questions listed below:

1. What is the actual channel length for Vds equal to 0.5 V, 1V and 1.5V separately? Assume $\lambda = 0.1\ V^{-1}$ for this process. What is the output impedance r_o at Vds = 1 V?
2. Assume $\lambda = 0$, find g_m at I_D = 1 mA.

D. For the circuit below, given Vt = 1 V, Kn'(W/L) = 2 mA/V^2 and $\lambda = 0$, Find R to make I_D = 1 mA and how much V_D is.



E. For the circuit below, given Vt = 1 V, Kn'(W/L) = 0.5 mA/V^2 and λ = 0, R_{G1} = 5 MΩ, R_{G2} = 5 MΩ, R_D = 6 KΩ AND R_S = 6 KΩ, Find voltages at the each terminal (V_G, V_S, V_D) and current at each node (I_G, I_S, I_1, I_2).



F. Design the circuit below to make Qp working in saturation region and I_D = 1 mA, V_D = 3 V, given Vt = -1 V, Kp'(W/L) = 2 mA/V^2 and λ = 0, Find R_D, R_{G1}, R_{G2}