ECE 331: Electronics Principles I
Fall 2013

Lab #3: MOSFETs Characterization

Pre-lab due on Thurs, Oct. 24, before noon
Report due on Tues, Nov. 12 to Fri, Nov. 15, at the beginning of your registered lab sessio

Important: All voltages are given for NMOS devices. Remember to reverse polarities for PMOS devices.

1: For **both NMOS and PMOS** with W = **0.54 μm** and $Lmin$ = **0.18 μm**:

- **Plot i_D vs. v_{GS} for v_{DS} = 0.2 V, 0.8 V and 1.5 V.**
  (Sweep v_{GS} from 0 V to 1.8 V with step size of 0.1 V)
  Write down the approximate threshold voltage you find from your plot.
  Open results browser to find the threshold voltage calculated by Cadence.
  With different v_{DS} what have you found from your plots? Why?

- **With W/L=3, L = 0.18 μm, Plot i_D vs. v_{DS} for v_{GS} = 0.2 V, 0.5 V, 0.7 V, 0.9 V, 1.1V,**
  (Sweep v_{DS} from 0 V to 1.8 V with step size of 0.1 V)
  Write down the approximate saturation voltage from each plot.
  With W/L=3, L = 2 μm, Plot i_D vs. v_{DS} for v_{GS} = 0.2 V, 0.5 V, 0.7 V, 0.9 V, 1.1V, and
  (Sweep v_{DS} from 0 V to 1.8 V with step size of 0.1 V)
  Write down the approximate saturation voltage from each plot.
  What have you found from the plots? Draw your conclusions.

- **Plot the transconductance (g_m) as a function of v_{GS} for v_{DS} = 1 V.**
  (Sweep v_{GS} from 0 V to 1.8 V with step size of 0.1 V.)
  How linear is the transconductance in the saturation region? Do you prefer g_m to be large Or small when designing the amplifier using MOS transistors ? With the same size and Overdrive voltage, assume no channel length modulation, will you prefer **PMOS** or **NMOS** when you design a high speed high gain amplifier? why?
  Comparing **NMOS** and **PMOS**, which is difference on consideration of g_m

- **Plot output impedance *ro* vs. v_{DS} for v_{DS} sweep from 0 V to 1.8 V with 0.1 V step size.**
  A. For v_{GS} equal to 0.8V, W/L=3, L = 0.18 μm
  B. For v_{GS} equal to 0.8V, W/L=3, L = 2 μm
  What have you found from your plot? Do you want the output impedance to be larger or smaller? Why? Comparing **NMOS** and **PMOS**, which is your priority when designing Precision current reference? What is the good side of increasing channel length? What is the down side?

2: For both **NMOS and PMOS**, with W = **3 μm** and L = **1 μm**;
Connect the body terminal of the transistor to a voltage source to make $|v_{SB}|$ = 0.2 0.2V, 0.5 V, 0.8 V respectively:

- **For each of the $|v_{SB}|$, plot i_D vs. v_{GS} for v_{DS} = 1 V.**
  (Sweep v_{GS} from 0 V to 1.8 V with step size of 0.1 V.)
  What have you found through the plots after adding $|v_{SB}|$?
  What is the effect of **increasing** $|v_{SB}|$? Is it good or bad to your circuit normally?