ECE 331: Electronics Principles I
Fall 2014

Lab #0: Introduction to Computer Modeling and Laboratory Measurements
Report due at your registered lab period on the week of Sept. 8-12

Week 1

Accessing Linux Servers

We will be using Cadence Virtuoso for all schematics, simulations, and layouts in this class. Cadence Virtuoso requires a Linux environment to run. Cadence Virtuoso is available on eight different **Linux servers named Linuxa1, a2, a3; Linuxb1, b2; nausicaa, teto and yupa**. There are two methods to access these servers and you can use either one of them.

Method 1: (**preferred**)
Start -> All Programs -> Internet -> NX Client for Windows -> NX Client for Windows
This should take you to a login screen that looks like this:

Choose one Linux server from the drop down list labeled above and **log in with your own username and password**. Open up a shell window.

Method 2:
Start -> Programs -> Cygwin – X -> XWin Server

This should start a windows bash shell. Minimize the shell, since you only need it to be running in the background. Next you need to run an SSH client called PuTTY.
Start -> Programs -> Internet -> PuTTY

In putty, enter the host name as linux#.engr.colostate.edu (where "#" is the server you want to login to). On the left menu, go to SSH -> X11 and enable X11 forwarding. Then click "open" and a shell will open with a login prompt.

First time setup

Create a directory named ece331 with the following command

$ **mkdir** ece331

Enter your newly created directory with:

$ **cd** ece331

Download and place the tsmc_setup.tgz file with the command below:

$ **cp** -r /top/students/UNGRAD/ECE/tuckern/shared/tsmc_setup.tgz

Extract the setup files with the command below (Don't forget, Linux is case-sensitive):

tar –xvzf tsmc_setup.tgz

This will create a folder called TSMC_Cadence that contains all the files necessary to start Cadence Virtuoso (formerly Custom IC) with the tsmc18rf technology files.

Starting Cadence

Make sure you are in your TSMC_Cadence directory.

$ cd TSMC_Cadence

Run the start-up script with:

$ bash

$ source cust_ic613_mmsim.cshrc

This script sets up the proper environment for Cadence to run. It may produce messages indicating that it has fallen back to older versions of the software. This is due to some version inconsistency on the ENS servers. If the script falls back to MMSIM72, you should consider trying a different server.

If you receive errors like this:

CLS_CDSD_COMPATIBILITY_LOCKING=NO: Command not found.

You most likely forgot to start a bash session.

Invoke Virtuoso with

$ virtuoso &

(The "&" keeps the terminal running in background)

Starting a Project

Once two windows open, close the “What’s New” window and open Library Manager under “tools” in the cds.log window.

In Library Manager you will want to start a new library for all your labs.

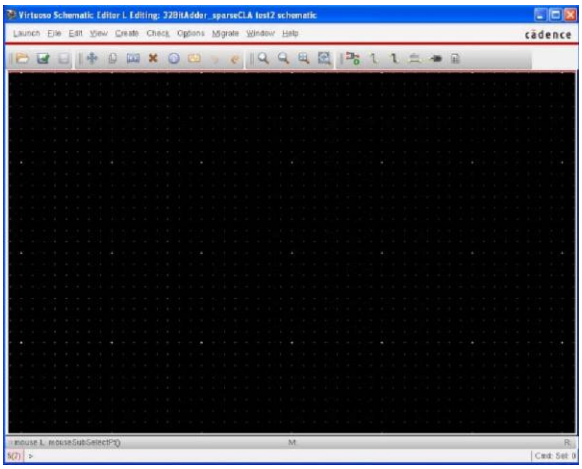
File -> new -> library

Type in the name for your new library (ie: ECE331Labs). A new window will come up prompting you for a technology file. Choose “attach existing technology file”. You need to attach “tsmc18rf”.

You will need to start a new cell view for each schematic (usually one cell view per circuit).

File -> new -> cell view

Enter a name and make sure the type is schematic. Click “always” to any license questions that you are asked. You should now have a blank schematic that looks something like this:



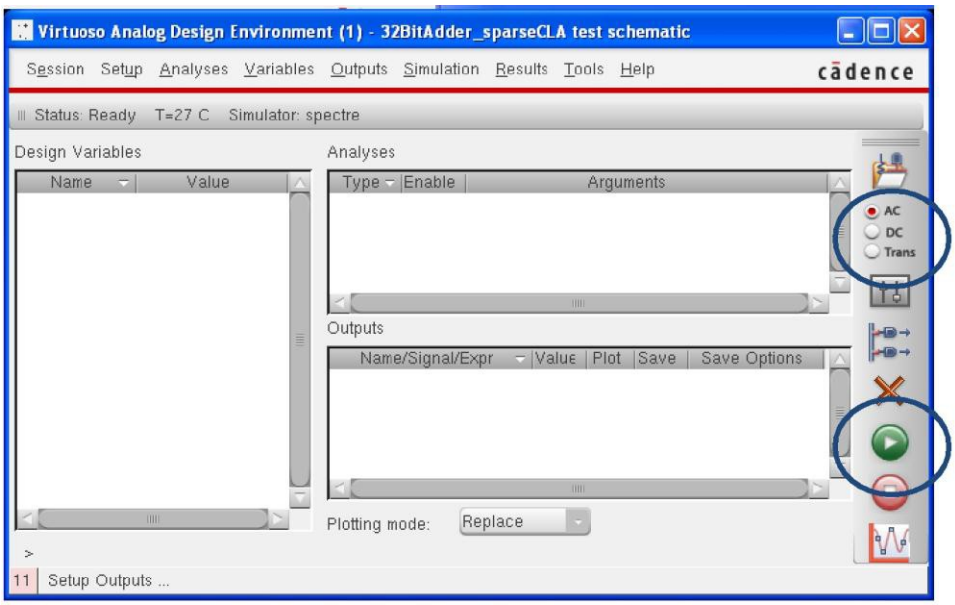
Hit the “i” key or click the “create instance” button. Browse to the “analogLib” library, choose the “res” cell, and set the view to “symbol”. Close the Library Browser window and change the value of the resistor from 1K to 5K. Click the “Hide” button and place two instances of the resistor on your schematic. Now hit the “w” key or click the “create narrow wire” button and connect the two resistors in series. Add a vdc voltage source from analogLib, set it to 1.8V, and connect it across the two resistors. Add a gnd symbol from analogLib and connect it to the negative node of the voltage source. If at any time you need to adjust an instance that has already been placed, simply select the instance and hit “q”; this will bring up all the parameters for that instance.

Analog Design Environment

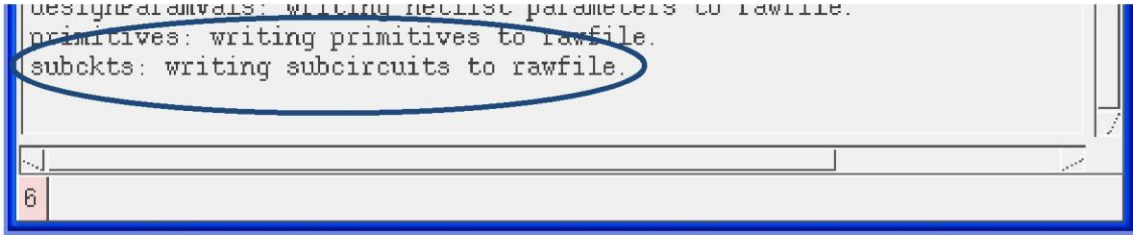
Now save your design with the “check and save” button and open Analog Design Environment:

Launch -> ADE L

Click “always” for the license request and you will see a simulation window that looks like this:



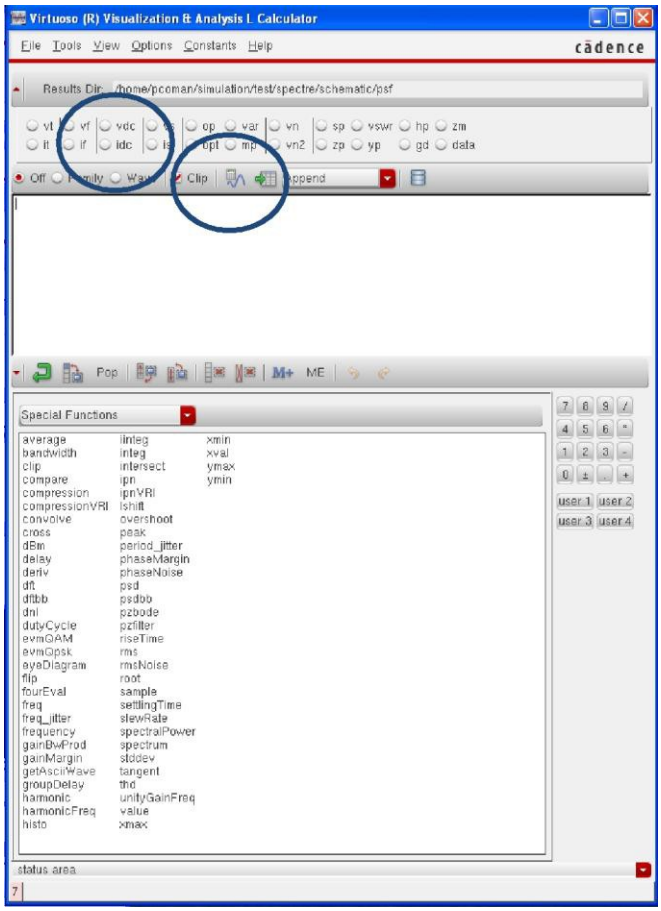
On the right side of the window, click the “choose analyses” button (second from the top). Select “dc” and check “Save dc Operating Point”. Click “OK” to return to the ADE window. Press the green “Netlist and Run” button to simulate. The simulation is done when you see this line in the new window:



This new window is only there to document the simulation, and can be closed once the simulation is complete.

From the ADE window, open the calculator with:

Tools -> calculator



In the upper left, select “vdc” and select the node between the two resistors on your schematic. Then press the “Evaluate the buffer” button. You should get a number corresponding to half the supply voltage in the text area. Close the calculator and any windows associated with ADE.

In your schematic window, press “q” and click on the resistor connected to the gnd node. Change its resistance value to this string: var1 . Save and open ADE again. Copy all variables from the schematic into ADE with:

Variables -> Copy From Cellview

Select DC analysis just as before, but this time selects “Design Variable” under the “Sweep Variable” option. The variable name is var1, and you should sweep it from 1k to 100k. Use a linear sweep with 10 points.

Let’s also set up the output graph to open automatically upon

completion: Outputs -> To Be Ploted -> Select On Schematic

On the schematic, select the node between the two resistors as the output to be plotted and run the simulation.

Here are some useful hotkeys:

“e”	descend hierarchically
“ctrl – e”	ascend hierarchically
“i”	create instance
“l”	name wire/net
“m”	move
“p”	create pin
“q”	edit object properties
“r”	rotate
“u”	undo the previous action (up to 128 times)
“shift – u”	redo what you just undid
“w”	create wire
“esc”	cancel selected action

Week 2:

You will need to bring a breadboard for this lab. You need to take a shot of the waveforms in all different parts and attach it into your final report write up.

1: Choose the values of a resistor and a capacitor in series to yield a cut off frequency of 10 kHz. Configure them to function as a low pass filter. Apply a 2-V peak to peak sinusoidal wave at 1 kHz, 20 kHz, and 100 kHz at the input and measure the output voltage (peak to peak value).

2: Choose the values of a resistor and a capacitor in series to yield a cut off frequency of 75 kHz. Configure them to function as a high pass filter. Apply a 2-V peak to peak sinusoidal wave at 5 kHz, 50 kHz, and 150 kHz at the input and measure the output voltage (peak to peak value).

3: Combine a low-pass filter and a high pass filter to create a band-pass filter that filters out frequencies below 10 kHz and above 75 kHz. Apply the input 2-V peak to peak sinusoidal wave at 1 kHz, 35 kHz, 50 kHz, and 100 kHz at the input and measure the output to verify functionality. Record the output voltage peak to peak value at different frequency.

4: Input a 2-V peak to peak square wave at 5 kHz into each of these three filters built above and observes the results. Try to explain what is happening in each case.