QUARTUS TROUBLESHOOTING GUIDE

1. Naming conventions:

Files and components in circuit-The name of the project file (qpf), block diagram/ circuit file (bdf), waveform file (vwf), and pins, gates and other symbols in bdf files should always start with a letter and never with a number or special character. The only special character allowed in the naming is an underscore.

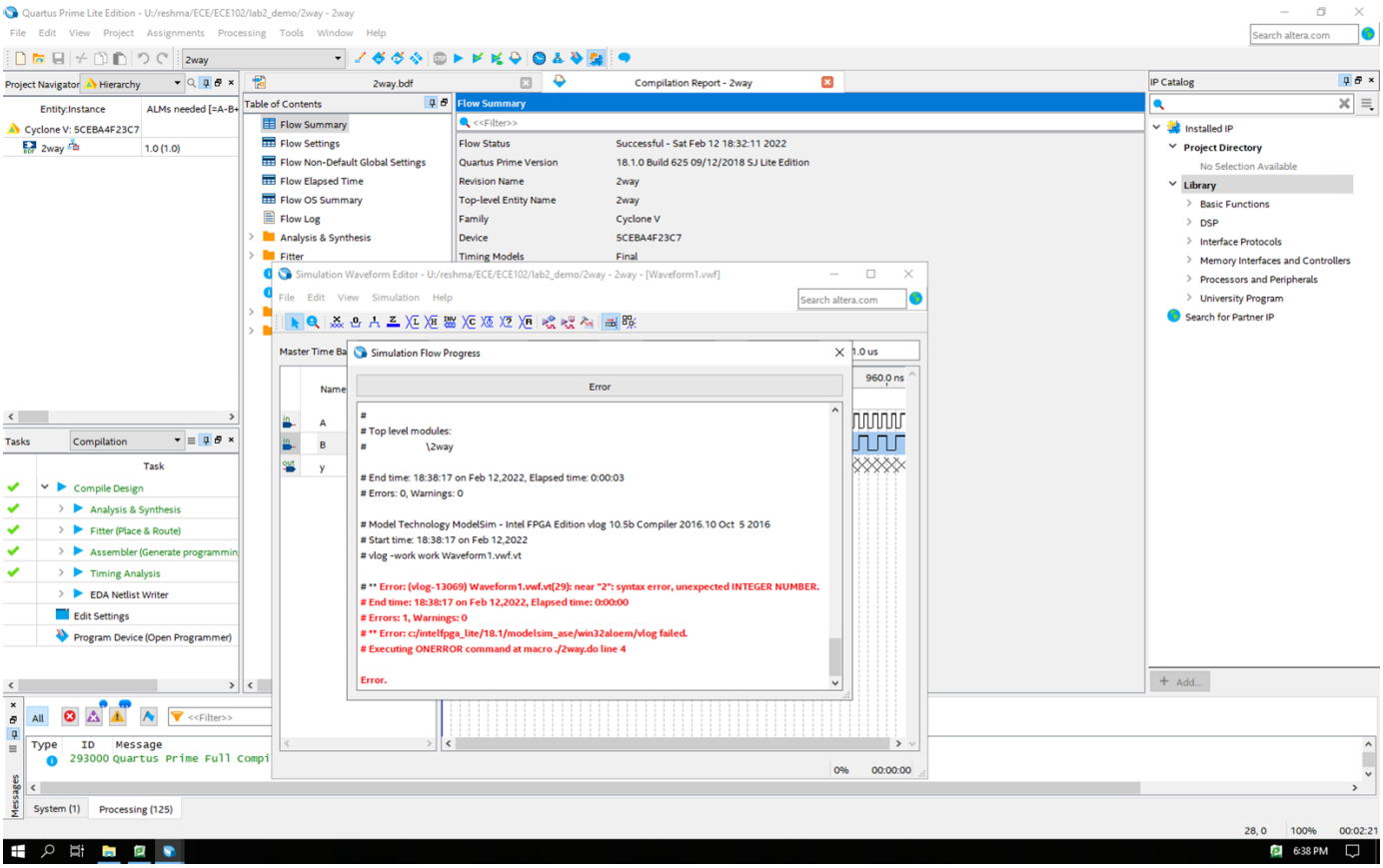

Fig 1: Simulation error due to incorrect naming of project and schematic files

The above figure shows an error message because the project file is named 2way and so is the schematic file. Note that the software compiled the bdf without any errors, but the simulation was unsuccessful.

The pins and logic gates in your circuit should not be named ‘input’, ‘output’, ‘xor’, ‘not’, ‘reg’ (for register) or by any such reserved keywords.

Naming wires- By naming wires, we can make Quartus recognize connections without physically connecting the entire path. Fig 2 shows an example.

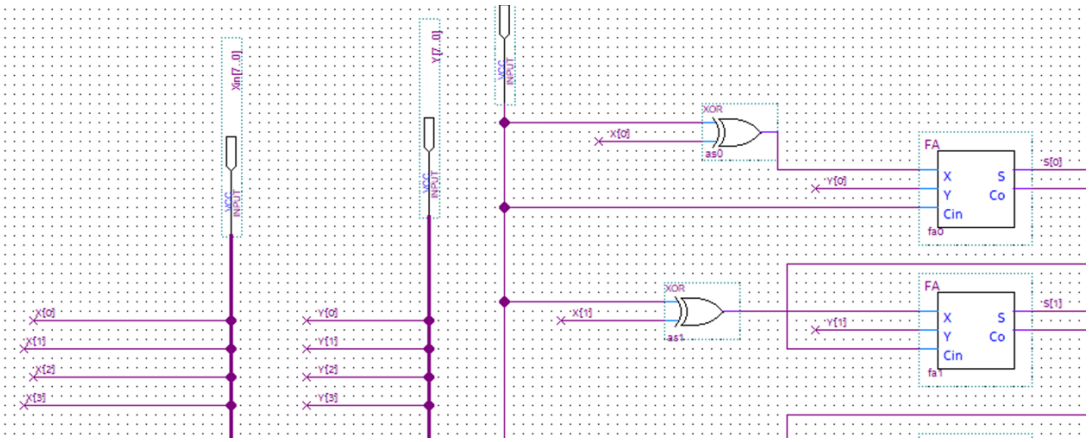

Fig 2: Wires named to make easily readable connections

Multi-bit inputs, outputs and use of buses - A bus carry multiple bits of data. When naming a bus, it is important to add the maximum capacity it can hold, eg: Abus[7..0] can hold 8 bits- Abus[7] to Abus[0]. Remember that if an input A of 3 bits are connected to the bus line Abus, the input pin should be labelled A[2..0] and Abus[2] will get the value of A[2], Abus[1] will be A[1] and Abus[0] will be A[0].

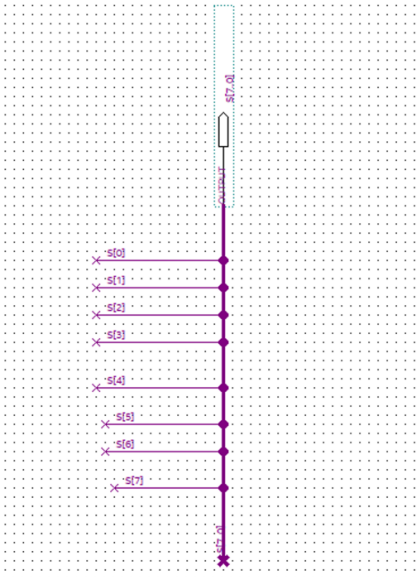

Fig 3: Bus line carrying 8 bits of output

2. Running multiple block diagram/ circuit files (bdf s) under the same project:

Note that Quartus by default recognizes a bdf file that matches the name of the project. If you create a new bdf file and if your project name doesn't match the file name, Quartus will compile a bdf file under the project that matches the project name or throw an error saying that the file does not exist under the project, as seen in Fig 4. Note that in the highlighted section under the 'Flow Summary' section of the Compilation Report, the 'Top Level Entity name' as Lab4. Top-level

Entity refers to the schematic file under compilation and Revision name refers to the project being run on Quartus.

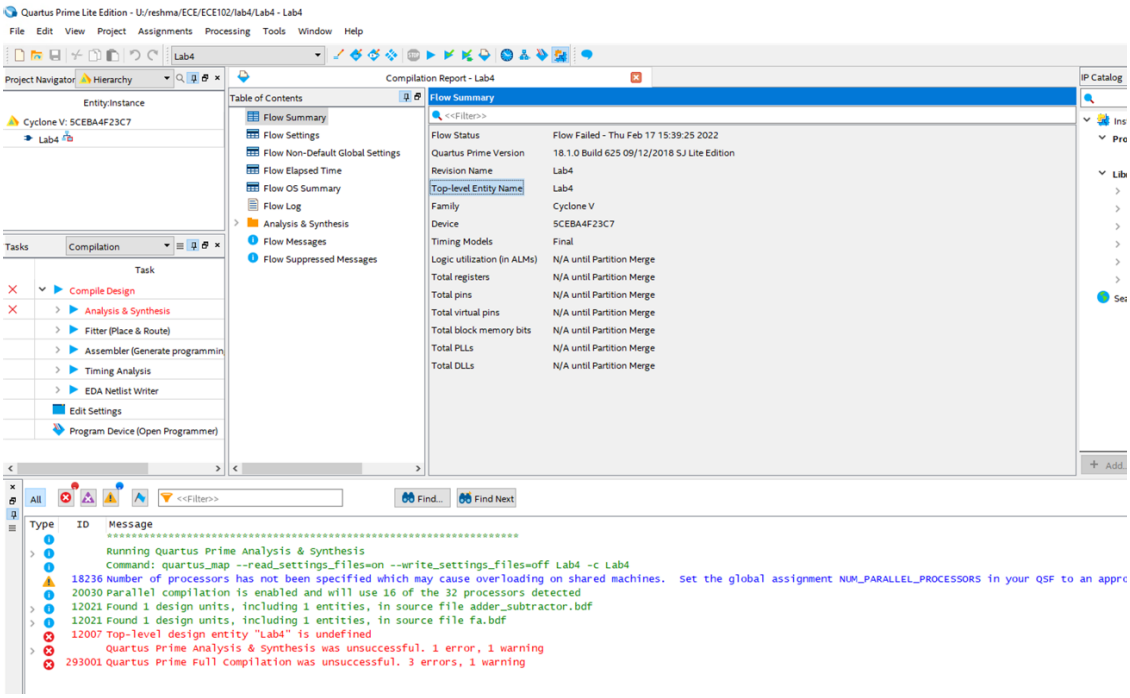

Fig 4: Error on compilation as no bdf file of the name ‘Lab4’ exists under the project

To compile the desired file, right click at the name of the board under the ‘Project Navigator’ window at the left of the main window. Go to Files, click on Add all option at the right. Make sure you have the required bdf file pasted to the folder. You’ll see the name in the list if you’ve put it in the correct path.

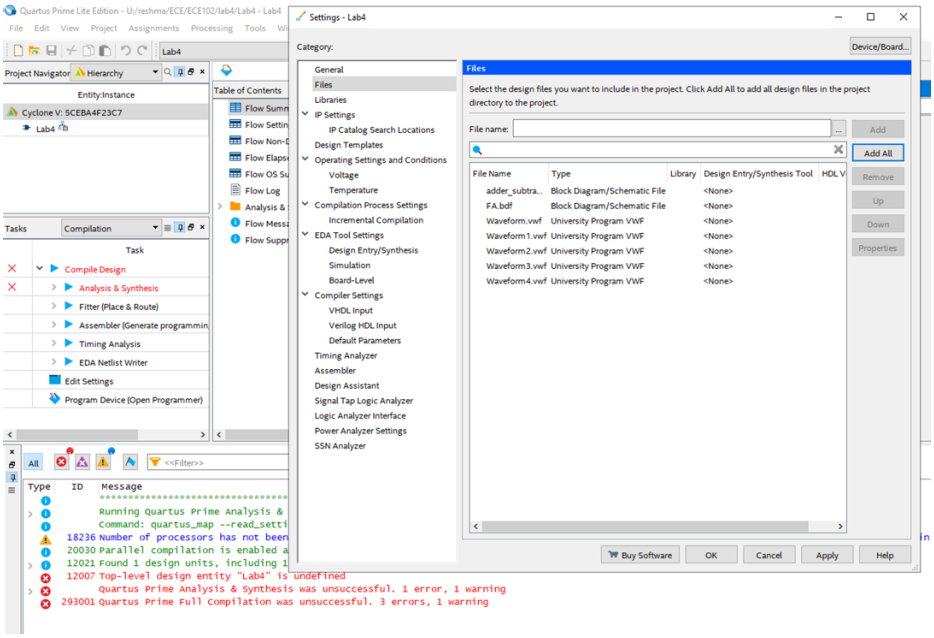

Fig 5: Adding the desired files to the project

Now click okay and compile. There will still be an error message because you must compile any new files to be recognized as a file under that project, but you will see a message that shows that Quartus has recognized the new bdf file, as seen in Fig 6.

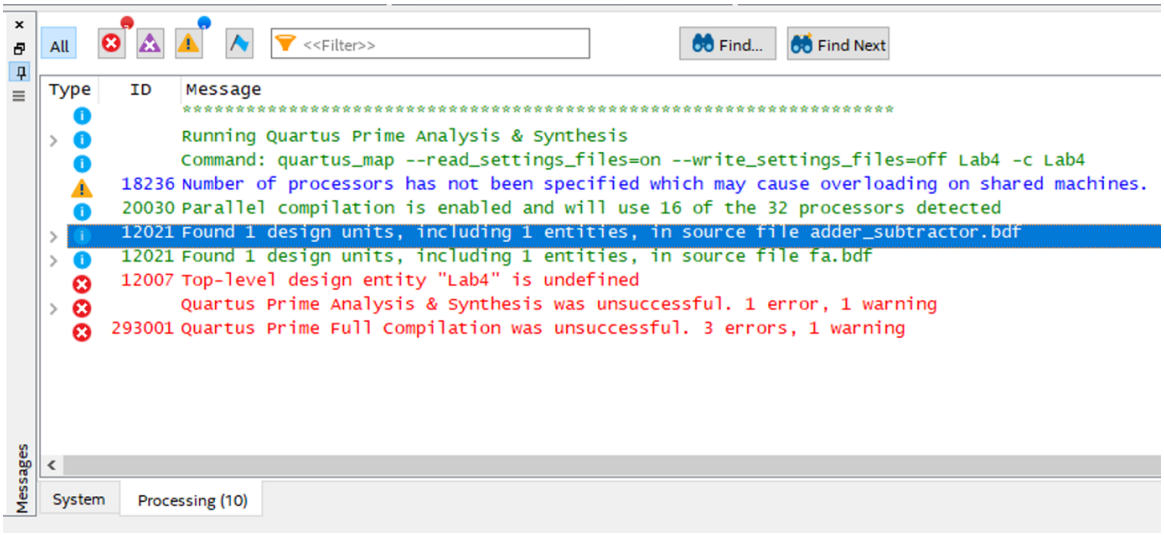

Fig 6: Message showing Quartus has recognized the newly added files

At the name of the board, right click again, Settings>General> Top Level entity, from the drop down, choose the correct file and compile.

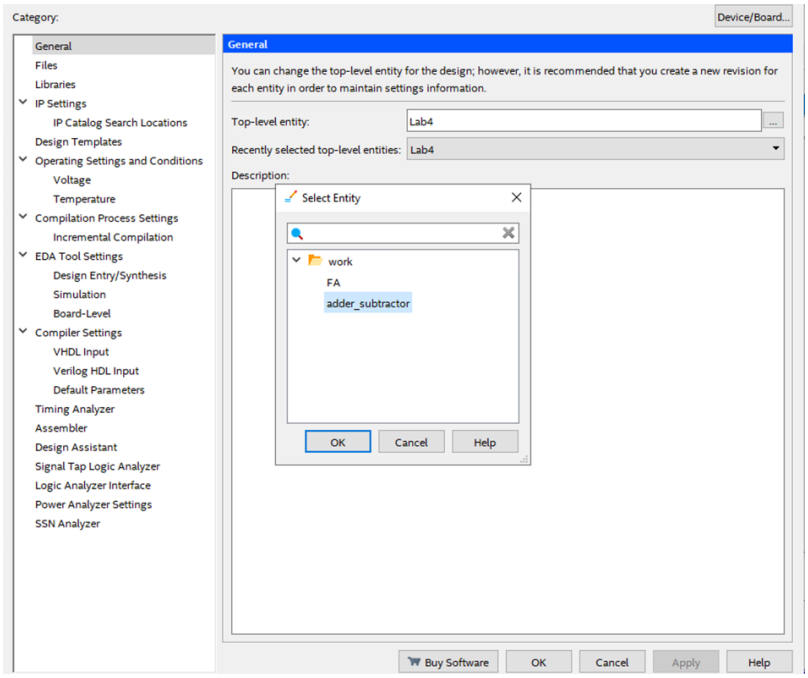

Fig 7: Showing the available bdf files

You can see from Fig 8 that at the left side, the 'Project Navigator' window has the file name 'adder_subtractor' and the 'Top Level Entity name' in the compilation report has also changed, and the file has successfully compiled.

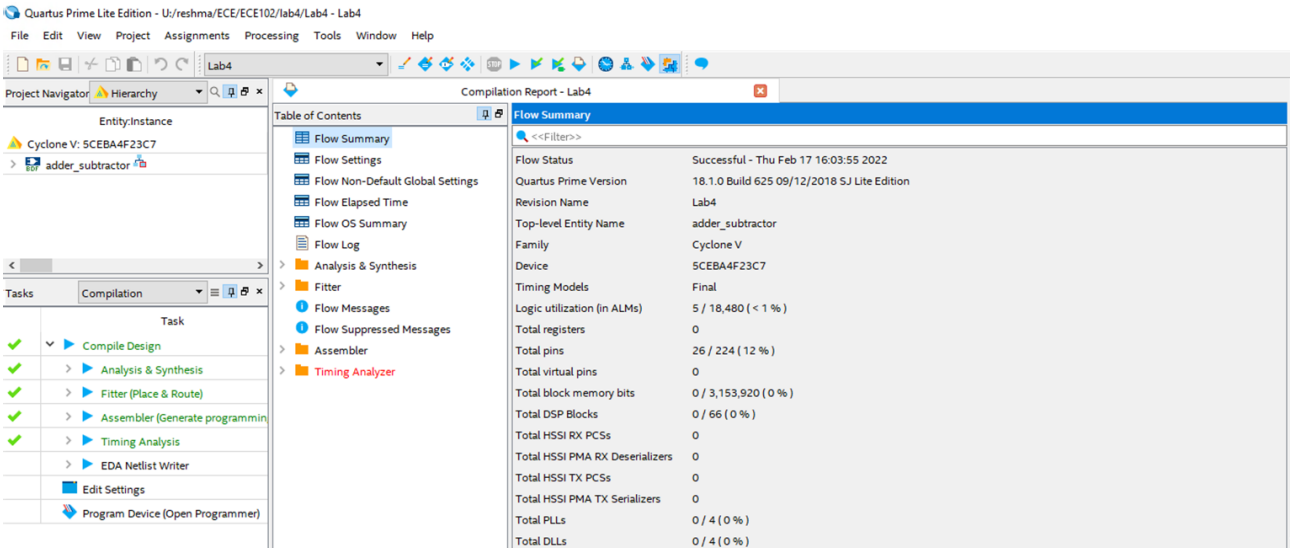

Fig 8: Successful compilation of the new schematic file

3. Troubleshooting simulation errors:

The main directory that contains the project file and schematic file also contains multiple subfolders containing files such as testbenches, netlists and simulations. The waveform file may get saved by Quartus in one such subfolder, commonly the 'output_files' subfolder. University Program VWF will only read a file under the main directory. In such events, you may get error messages as seen in Fig 9 and Fig 10.

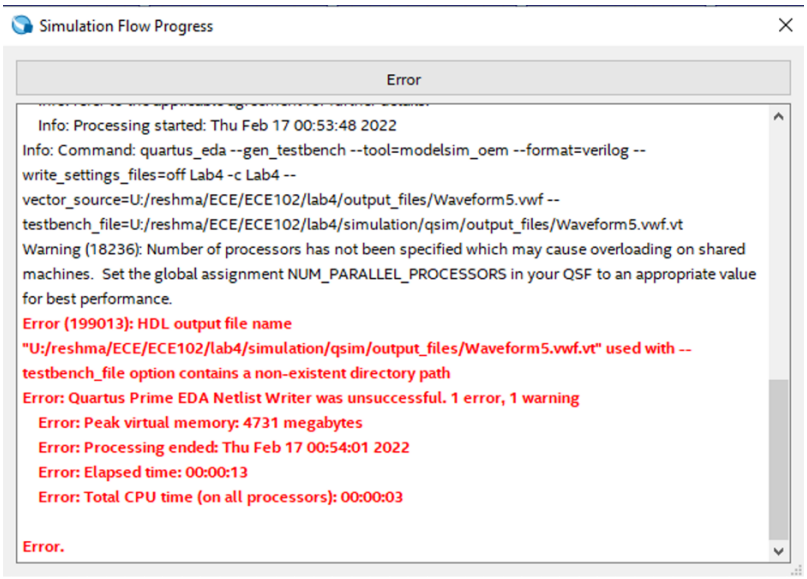

Fig 9: Error showing that the testbench file is in the wrong subfolder

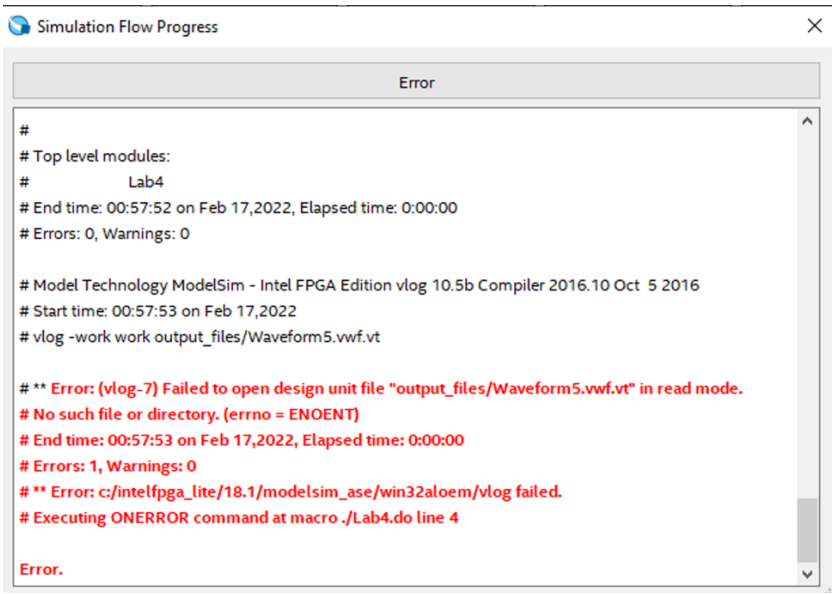

Fig 10: Error showing that the waveform file is under the wrong subfolder

To solve this issue, before running Functional simulation, go to Simulation> Simulation settings. The window in Fig 11 will pop up. There are three sections in the window that you should modify. Under 'Testbench Generation Command (Functional Simulation)', there are two paths, one to generate the waveform file(vwf) and another to generate testbench in the simulation subfolder (U:/……simulation/ ….vwf). Under 'ModelSim Script (Functional Simulation)', there is the command to generate the simulation netlist. Delete ONLY the 'output_files/' from the three selected parts in Fig 11.

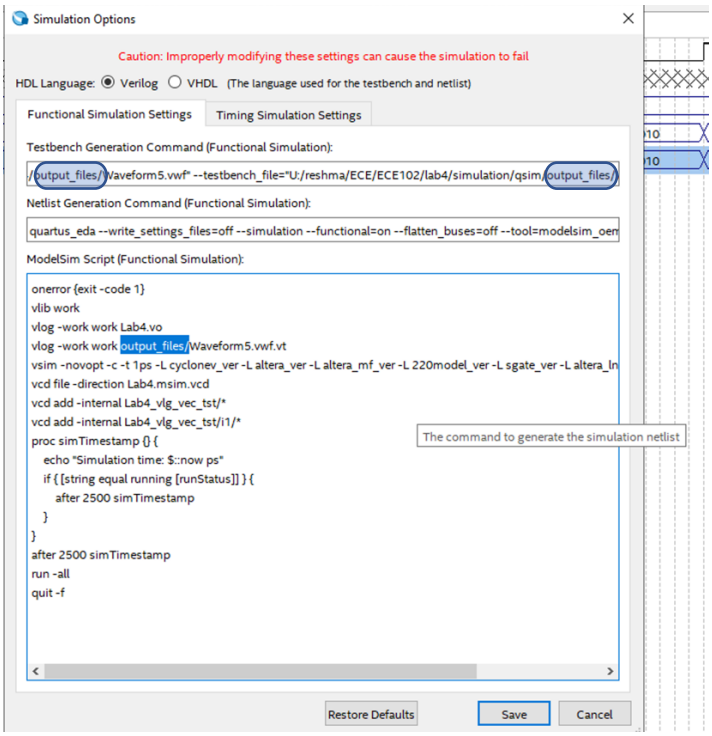

Fig 11: The sections to be edited for successful simulations

Note that even after editing the paths, the waveform file may get stored in the output_files subfolder and give an error as shown in Fig 8. To avoid this, you must save the file manually by selecting File>Save As and ensure that it is saved in the main folder with your. qpf and .bdf files.