EE 102 **Fall 2011**

Digital Circuit Logic

Final Exam

Dec. 13, 2011

Duration: 100 Minutes

Honor Code:

I have neither given nor received – nor have
I tolerated others' use of – unauthorized aid.

Name: _____

This is a closed book exam.
One page of notes is allowed.
Write the answer in the space provided.
Partial credit will not be given unless all the steps are clearly indicated.
Work all the five problems.

1. A) Convert the decimal number -114 to each of the following formats assuming an 8-bit representation:

Sign magnitude:

One's complement:

Two's complement:

B) Carry out the addition of the following two's complement numbers. Is there an overflow?

```
  10011010
  11101110
```

C) Multiply the following two binary integers:

```
    101001
      1011
```

2. Find the Minimum 2-level NOR realization of the function F + G′ where

$F(A,B,C,D) = \Sigma\, m(0,3,4,5,6,10,14,15)$

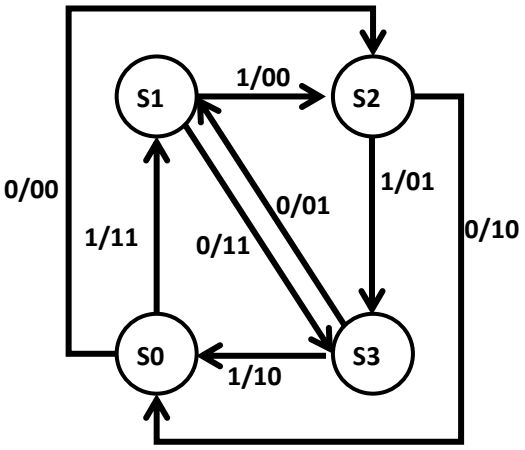
$G(A,B,C,D) = \Pi\, M(2,3,5,6,7,10,13)$

3. Design a Moore State Diagram for a single input (X) two output (Z1, Z2) circuit, which produces an output Z1= 1 whenever the sequence 100 is detected. The output Z2=1 whenever the sequence 100100 is detected. Note that it is possible for both Z1 and Z2 to be one simultaneously for certain input patterns.

4. Design a Mealy State Diagram for a single input single output system the output of which is 1 if and only if in the input **there have been exactly two consecutive 1's followed by two more consecutive 0's.** An example sequence is given below:

X = 0 1 1 1 0 0 1 1 0 0 0 0 1 1 0 0 1 1 1 0 0 0
Z = 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 1 0 0 0 0 0 0

5. Implement the following state diagram using J-K flip-flops. Use the following state assignment: S0=00; S1=01; S2=10; S3=11;



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