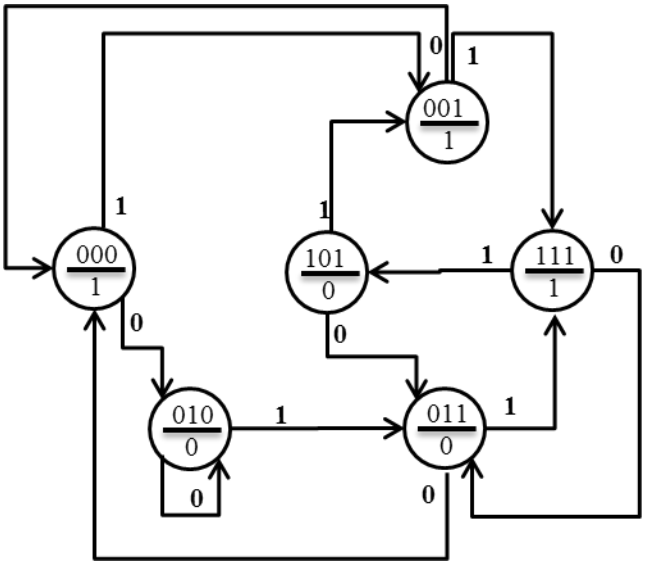
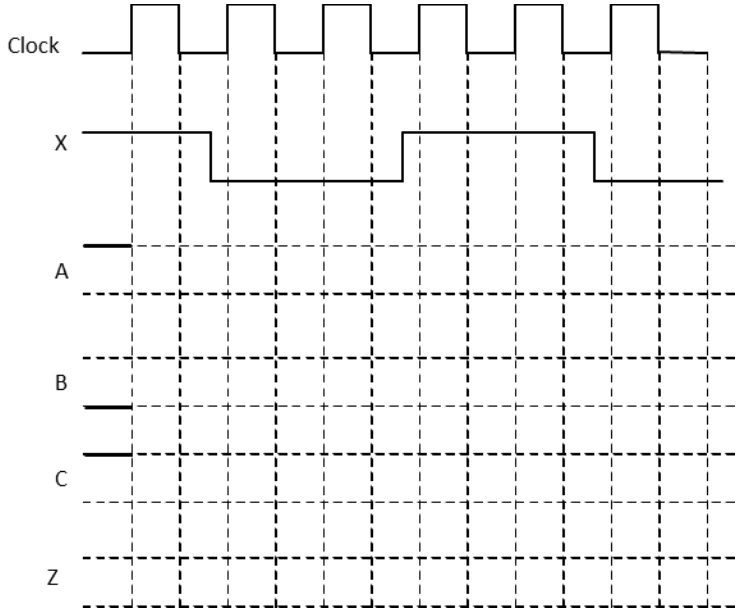
Homework 11 Due 11/14/17

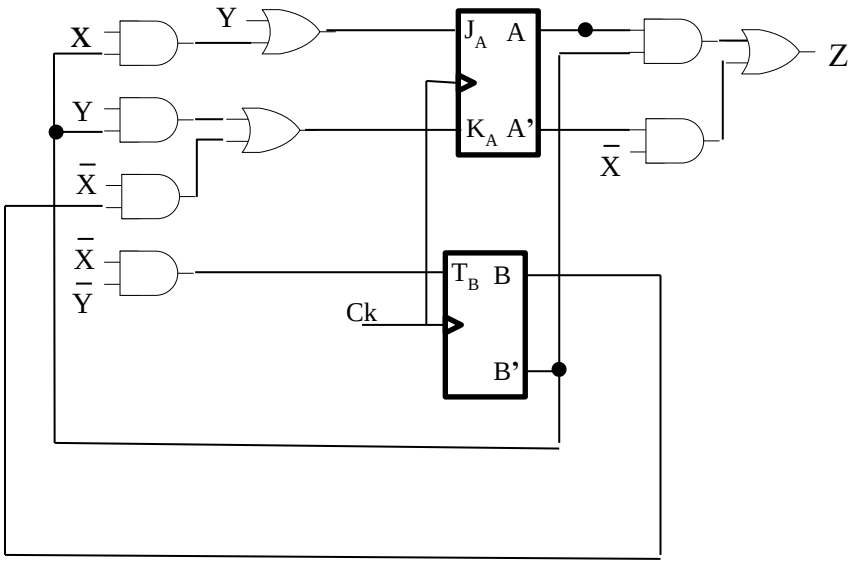
1. The state diagram shown below is implemented using three negative edge-triggered flip-flops with outputs labeled A,B,C. The output of the circuit is Z. Complete the timing diagram, assuming that the initial state is 101.



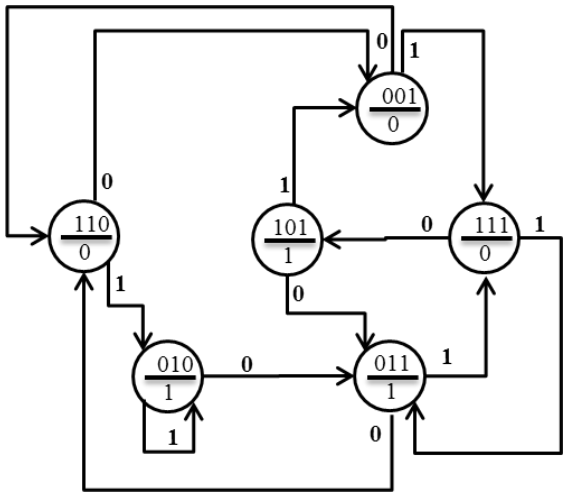


2. A sequential circuit is given below. The states in the transition diagrams are labeled AB, e.g., the state

corresponding to A=0, B=1 is denoted as 01. The inputs to the sequential circuit are X and Y, and its output is Z. Draw a complete state transition diagram for the circuit.



3. Design a circuit to implement the following state diagram. All the K-maps and circuit diagrams should be complete and clearly labeled.
   a) using T type positive edge triggered flip-flops and
   b) using D-type positive edge triggered flip-flops



4. Design Moore and Mealy state diagrams for the following: A circuit has a two-bit binary number (X1,X0) as inputs and an output Z. Z is 1 iff the most recent binary number

(X1,X0) is greater than the previous binary number.

5. Design Moore and Mealy state diagrams for the following:
   A circuit has a two-bit binary number (X1,X0) as inputs and three output lines Z2,Z1,Z0. The binary number (Z2,Z1,Z0) is equal to the two the sum of most recent input values. For the first pair of input values, use 00 as the previous pair.
   Ex.

X1:	0	1	0	1	0	1	0	0	0	0. .
X0:	1	1	1	0	1	1	0	0	1	1
Z2:	0	1	1	0	0	1	0	0	0	0
Z1:	0	0	0	1	1	0	1	0	0	1
Z0:	1	0	0	1	1	0	1	0	1	0