Figure 1: Typical FPGA or ASIC power management requirements
Figure 2: Step-down Configurations

General: A variety of microcontroller applications benefit from easy-to-implement, low-cost, step-down architectures for efficient power management. This includes high-efficiency, low-power, and low-voltage applications.

Function: Step-down (V_out < V_in)

Linear Regulator

Buck Integrated Regulator or Controller

A second switch replaces the controller in the architecture mentioned above, with high-efficiency at low currents (≤0.5A) or low duty cycles. When to use: Typically when V_out is 3x to 5x V_in.

Synchronous Buck

Non-Synchronous Buck

Figure 2: Step-down Configurations

Power Management Considerations for FPGAs and ASICs
LM5110 shown in parallel drive and synchronous rectifier drive applications.
6x one non-inverting, dual non-inverting, dual inverting, and one inverting

Offered in three industry standard configurations:

• Shutdown pin disables drivers for low-power standby modes

• Integrated under voltage lockout protection (2.8V typical)

• Short propagation delay times (25 ns typical)

• Each channel can sink/source 5A / 3A for very fast rise/fall times (20 ns / 10 ns into a 2 nF load)
Power Management Considerations for FPGAs and ASICs
3. **Push-Pull Transformer Balance Problem**

To monitor saturation of Transformer Core we will employ current sensors in $Q_1$ and $Q_2$ collectors to look for high current spikes.

We compare to $I_{\text{control}}(\text{ref})$ and we shut off $Q_1$ and/or $Q_2$ if $I > I_{\text{control}}$.

Due $V_{\text{on}}(Q_1) \neq V_{\text{on}}(Q_2)$ and $\Delta t(Q_1) \neq \Delta t(Q_2)$ we might have a slight offset each clock cycle and $i_{Lm}$ is not zero.

For $+V_g$ on dot for $+V_{-\text{sec}}$.

For $-V_g$ dot for $-V_{-\text{sec}}$.

$V_{\text{on}}(Q_1) = V_{\text{on}}(Q_2)$?
Even a small imbalance adds up after 100 switch periods and the transformer will ultimately saturate. Then for example the current on $i(Q_1)$ will shoot up when $L_m \rightarrow 0$.

Big i spike when transformer saturates at $nT$.

IC set to maximum peak current of TR spec.

Use $I_c$ (control) as a maximum to sense if $i_{Q_1}$ gets excessive and shut it down if it does. In practice we never build push pull converter with duty cycle control and voltage. Rather we use current programmed control of Chapter 11. Below we compare switch stress in the topologies of lectures 15 and 16.

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Final Solution to $V_oc$ across "2"
Primary controller: LM5030 100 V current-mode
Secondary controller: LM5642 dual synchronous bus

- $48 \, V_{IN}$, multiple outputs $\pm 12 \, V$, 1.8 V, and 1.5 $V_{OUT}$
- High efficiency $>90\%$
- Tight regulation $<2\%$
- Oscillators synchronized to a master clock
- User-programmable softstart and power on/off sequencing
- Available separately or together:
  - LM5030 (MSOP-10)
  - LM5642 (TSSOP-28)
LM5030

- Internal high-voltage (100 V) start-up regulator
- Fully integrated LM5030 includes: high bandwidth error amp, precision reference, programmable softstart, and dual-mode current sense

32 V to 76 V

27 V @ 30 A
Available separately or together:

- Programmable softstart and power on/off sequencing
- Oscillators synchronized to a master clock
- Tight regulation >2%
- High efficiency >90%
- 48 V IN, multiple outputs ±12 V, 1.8 V, and 1.5 V OUT

Primary controller: LM5030 100 V current-mode Push-Pull

Secondary controller: LM5642 dual synchronous buck
First we review the switch stress of the push-pull compared to the half and full bridge covered earlier.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Bipolar Power Switch</th>
<th>MOSFET Power Switch</th>
<th>Rectifier(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{in}$</td>
<td>$V_{oss}$</td>
<td>$V_n$, $I_p$</td>
</tr>
<tr>
<td>Push-pull</td>
<td>$2V_{in}$</td>
<td>$1.2P_{out}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{in(min)}$</td>
<td></td>
</tr>
<tr>
<td>Half-bridge</td>
<td>$V_{in}$</td>
<td>$2P_{out}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{in(min)}$</td>
<td></td>
</tr>
<tr>
<td>Full-bridge</td>
<td>$V_{in}$</td>
<td>$1.2P_{out}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{in(min)}$</td>
<td></td>
</tr>
</tbody>
</table>

Note that the push-pull is equivalent to the full bridge in switch stress and better than the half bridge. However, the push-pull is a dangerous circuit as it has a tendency towards core saturation which will cause the transformer input to look like a short and will likely kill the switches. This arises when the flux within the core is inadvertently non-symmetric so that a small DC offset occurs. Unfortunately, this small offset will cause a walk towards saturation over many switch cycles. Usually, current mode feedback must be employed rather than voltage feedback to control this difficulty of push-pull. Also possible, is active core re-balancing as illustrated on the next page.
New cascaded controller/100 V driver
“chipset” family

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Voltage-fed or current-fed</th>
<th>Controller</th>
<th>Driver(s)</th>
<th>Benefits/applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cascaded push-pull</td>
<td>Voltage-fed</td>
<td>LM5041</td>
<td>LM5102</td>
<td>High efficiency/medium power</td>
</tr>
<tr>
<td>Cascaded push-pull</td>
<td>Current-fed</td>
<td>LM5041</td>
<td>LM5102</td>
<td>High efficiency/medium power</td>
</tr>
<tr>
<td>Cascaded half-bridge</td>
<td>Voltage-fed</td>
<td>LM5041</td>
<td>LM5102 &amp; LM5100</td>
<td>High efficiency/medium to high power</td>
</tr>
<tr>
<td>Cascaded full-bridge</td>
<td>Current-fed</td>
<td>LM5041</td>
<td>LM5102 &amp; (2) LM5100</td>
<td>High efficiency/high power</td>
</tr>
</tbody>
</table>

Flexibility for multiple configurations: interleaved forward, cascaded push-pull, half-bridge, and full-bridge

LM5041 typical application

33 - 76 V
## Estimating the Significant Minimum Parameters of the Power

<table>
<thead>
<tr>
<th>Semiconductors</th>
<th>Bipolar Power Switch</th>
<th>MOSFET Power Switch</th>
<th>Rectifier(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology</td>
<td>$V_{CBO}$</td>
<td>$I_C$</td>
<td>$V_{DSS}$</td>
</tr>
<tr>
<td>Flyback</td>
<td>$1.7V_{in(max)}$</td>
<td>$2P_{out}$</td>
<td>$1.5V_{in(max)}$</td>
</tr>
<tr>
<td>One Transistor</td>
<td>$\frac{2P_{out}}{V_{in(min)}}$</td>
<td>$2V_{in}$</td>
<td>$1.5P_{out}$</td>
</tr>
<tr>
<td>Forward</td>
<td>$2V_{in}$</td>
<td>$V_{in}$</td>
<td>$2V_{in}$</td>
</tr>
<tr>
<td>Push-pull</td>
<td>$\frac{1.2P_{out}}{V_{in(min)}}$</td>
<td>$2V_{in}$</td>
<td>$1.2P_{out}$</td>
</tr>
<tr>
<td>Half-bridge</td>
<td>$V_{in}$</td>
<td>$\frac{2P_{out}}{V_{in(min)}}$</td>
<td>$V_{in}$</td>
</tr>
<tr>
<td>Full-bridge</td>
<td>$\frac{1.2P_{out}}{V_{in(min)}}$</td>
<td>$V_{in}$</td>
<td>$V_{in}$</td>
</tr>
</tbody>
</table>

**Notes:**
- Whoa! Flyback rectifier is hard to diodes.
- Whoa! Needs HV FETS.
- Half-Bridge sucks! Needs new FETS.
Universal Input

Fig. 1. Schematic of 2.75W LinkSwitch Link501 charger.

Performance Summary
Output Power: 2.75W
Efficiency: No load consumption:
230W, 230Vac
200mW, 115Vac

Input: Battery Charger
Output: 700V MOSFET

New Data
Pin 2: I = 0.2 A
Pin 3: V = 2.3 V
Input: 5.5 V at 500 mA
Output: V = I

Note: New data and controller on IC.
Fig. 3. LinkSwitch Control pin characteristic provides both duty cycle and current limit control to generate a CV/CC output.

Power supply output characteristic

- Constant voltage region
- Constant current region

Current limit control during constant current limit operation

Duty cycle control during constant voltage operation

Switching frequency reduced 42 kHz to 30 kHz

Control pin current lc

- Duty cycle
- 30%
- 75%
- 100%

Auto-restart

10% loss

Control pin current lc

Constant current region

Output voltage

Output current

Auto-restart

3%

- 3% loss
- below 3%

LCM

Flyback
Fig. 2. Typical LinkSwitch charger output V characteristic.

\[ V_n = 115 \text{ Vac} \]
\[ P_{in} = 208 \text{ mW} \]
\[ P_{in} = 250 \text{ mW} \]