Applications
- Blade servers
- N+1 redundant systems
- Telecom line cards
- RAID
- Merchant power

Features
- Ultra-fast, adjustable gate turn-off
- Internal charge pump
- Wide voltage operation range
- Adjustable turn-off threshold
- Complements TI’s TPS2490 hot swap controller
5. **Comparison of PWM Converters**

We now compare the old big three converters (buck, boost and buck-boost) to five new converter topologies that we will be introducing in lectures 14-16. All of the new five topologies will have transformer isolation. Moreover, as we will see each new topology has a specific power range over which it works best. Below we list converters in ascending order of the power level they can handle as well as the voltage levels. In general, the higher power and voltage level topologies have 2-4 switches rather than the single switch of the big three topologies.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Power Range (W)</th>
<th>( V_{\text{input}} ) Range</th>
<th>( V_{\text{output}} ) Range</th>
<th>In/Out Isolation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck</td>
<td>0–1000</td>
<td>5–1000</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Boost</td>
<td>0–150</td>
<td>5–600</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Buck-boost</td>
<td>0–150</td>
<td>5–600</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Half-forward</td>
<td>0–150</td>
<td>5–500</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Flyback</td>
<td>0–150</td>
<td>5–500</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Push-pull</td>
<td>100–1000</td>
<td>50–1000</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Half-bridge</td>
<td>100–500</td>
<td>50–1000</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Full-bridge</td>
<td>400–2000+</td>
<td>50–1000</td>
<td>Yes</td>
<td></td>
</tr>
</tbody>
</table>

Conversions @ 20KW with new IGBT switches

All 3 introduced in Ch 6

---

Where various transformer-isolated topologies are commonly used.
As the power level changes we also will need to determine which of the big eight PWM converter topologies is best suited to the required power level. *Choice of PWM topology will in turn determine the switch stress experienced by the power switches.* Moreover, the timing sequence for driving the various topologies will also vary. In particular, we will cover both switches drives at \( f_{sw} \) and switches synchronized at \( \frac{1}{2} \times f_{sw} \) in our discussions below. On the next page we briefly summarized what we learned in lecture 11 as regards switch topology and power as well as voltage and current levels in the associated switches.
Finally, the cost available to implement the power solution and relative merits of all of the above.

- Must be managed well or is it a battery that will be charged often? or is it a limited supply battery that might require the input source be larger reservoir like the line power?

- Efficiency requirements - will the input supply e.g. variation of the input supply e.g. Variation of the input source and regulation be large reservoir like microcontroller load that changes with various operating conditions?

- Output voltage level and regulation needed - is the output protected from surges? What maximum output voltage protection is required?

- States of the processor:

- Other considerations of the input source:

- Physical and environmental issues - e.g. any height limitations? How is the ventilation for taking away heat? Any area availability for the power solution?

- Impedance of the supply source? How far is it from the power solution?

- e.g. Surface mount vs. through hole, PCB line, contact limitations, lead-free, and solder reflow temperatures etc.

- What are the manufacturing requirements? What is the ambient temperature of operation?

- When selecting a device for the application, it is important to understand the following.

Gather needs
In lectures 16 and 17 we will cover the last of the big eight topologies. We need to employ these circuits to achieve kW power operation. With topology comes different switch stress. That is as the input voltage changes we use different topologies as shown below. The flyback has low parts count but high peak currents than those in a forward converter. The half bridge reduces switch voltage stress because only ½ the $V_{in}$ appears across the primary winding. The full bridge requires four switches, two of which require floating gate drive. The push-pull, as we will see below, also works but has a danger of CORE SATURATION. This could cause us to fry the switch if not careful to balance the core so that no imbalances or DC levels occur.

![Comparison of the PWM Switching Regulator Topologies](image)

<table>
<thead>
<tr>
<th>Topology</th>
<th>Power Range (W)</th>
<th>$V_{in}$ Range</th>
<th>Isolation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck</td>
<td>0–1000</td>
<td>5–1000</td>
<td>No</td>
</tr>
<tr>
<td>Boost</td>
<td>0–150</td>
<td>5–600</td>
<td>No</td>
</tr>
<tr>
<td>Buck-boost</td>
<td>0–150</td>
<td>5–600</td>
<td>No</td>
</tr>
<tr>
<td>Half-forward</td>
<td>0–150</td>
<td>5–500</td>
<td>Yes</td>
</tr>
<tr>
<td>Flyback</td>
<td>0–150</td>
<td>5–500</td>
<td>Yes</td>
</tr>
<tr>
<td>Push-pull</td>
<td>100–1000</td>
<td>50–1000</td>
<td>Yes</td>
</tr>
<tr>
<td>Half-bridge</td>
<td>100–500</td>
<td>50–1000</td>
<td>Yes</td>
</tr>
<tr>
<td>Full-bridge</td>
<td>400–2000+</td>
<td>50–1000</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Why high V for high power? Where various transformer-isolated topologies are commonly used.
- Thermal shutdown
- A sink/source driver
- Dual synchronizable to external clock
- Single resistor oscillator setting

<table>
<thead>
<tr>
<th>Benefit/Application</th>
<th>Driver</th>
<th>Controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>High efficiency/multi-output power</td>
<td>Optional</td>
<td>LM35642, LM35030</td>
</tr>
<tr>
<td>High efficiency/high power</td>
<td>(2) LM35100</td>
<td>LM35030</td>
</tr>
<tr>
<td>High efficiency/medium-high power</td>
<td>(1) LM35100</td>
<td>LM35030</td>
</tr>
<tr>
<td>High efficiency/medium power</td>
<td>Not Required</td>
<td>LM35030</td>
</tr>
</tbody>
</table>

**Configurations**

Half-bridge drivers and LM35642 dual synchronous buck controller. The LM35030 can be used as a chipset with the new 100 V LM5100.

Embedded telecommunication solutions

> > 90% efficiency
Fig. 3. A transformer-based dc-ac power stage such as this H-bridge circuit offers galvanic isolation in exchange for added weight, size, cost, and efficiency.
Full Bridge Primary

Cross-Connecting Case

1, H on, 2, 3 off

3, 2 on, 1, 4 off

$V_p = +V_g$ for $DT_{sw}$

Case $D = \frac{1}{2}$

$V_p = -V_g$ for $DT_{sw}$

Allows for trif. reset!

Key to success

$V_{sec}$ $nV_p$ $nV_p$ $t$
Resettin Lm of TRF by symmetric $\pm V_p$

- $Q_1, Q_{4h}$ on
- $T_{sw(prim)}$ or $2 \times T_{sw}$

- $Q_2, Q_{3h}$ on
- $f_{primary} = \frac{1}{T(0) + T(2)} = \frac{T_{sw}}{2}$

Switches

TRF
Resetting $L_m$ of $T_h$ via Bridge Drive

$T_{sw}(1): D_1, D_2$

$T_{sw}(2): D'_1, D'_2$

$\pm V_g$

Zero intervals are key

$V_g = 0$

In hangs!

$f_{primary} = \frac{1}{T_{sw}(1) + T_{sw}(2)} = \frac{f}{f_{sw}}$
primary, or by use of current programmed mode (Chapter 12).

Saturation can be prevented by placing a capacitor in series with

Magnetizing current slowly increases in magnitude.

Net volt-seconds are applied to primary winding.

These volt-seconds never add to exactly zero.

\[
\begin{align*}
(\text{Forward voltage drops}) & - Z F \left( \int_{\text{conduction time}}^{\text{conduction time}} \left( \frac{\partial}{\partial t} \left( \int_{\text{conduction time}}^{\text{conduction time}} \right) - Z F \right) \right) \\
\text{Volt-seconds applied to primary winding during next switching period:} & \\
(\text{Forward voltage drops}) & - Z F \left( \int_{\text{conduction time}}^{\text{conduction time}} \left( \frac{\partial}{\partial t} \left( \int_{\text{conduction time}}^{\text{conduction time}} \right) - Z F \right) \right) \\
\text{Volt-seconds applied to primary winding during first switching period:} & \\
\end{align*}
\]

Effect of nonidealities

Transformer volt-second balance
primary, or by use of current programmed mode (Chapter 11).

Saturation can be prevented by placing a capacitor in series with

Magnetizing current slowly increases in magnitude

Net volt-seconds are applied to primary winding

These volt-seconds never add to exactly zero.

\[ a = \frac{V_{in}}{f} \]

\[ a = \frac{V_{out}}{f} \]

Volts-seconds applied to primary winding during next switching period:

Volts-seconds applied to primary winding during first switching period:

Effect of nonidealities:

On transformer volt-second balance

\( V_{out} = V_{in} + V_{loss} \)

\( V_{out} = V_{in} - V_{loss} \)

No assurance: \( V_{out} \neq V_{in} \)
Fig. 10. Measured total loss of 150-kHz bridge transformer providing 12 V at 60 A.

Bridge Transformer Dissipation at 80°C

720-W output

Duty Cycle

- 70.0%
- 62.5%
- 60.0%
- 60.0%
- 55.0%
- 50.0%

Winding loss vs. Core loss

[Diagram showing loss distribution]
Flexibility of Bridge

\[ E_{AB} = D V_g - (1-D)V_g \]

\[ = (2D - 1)V_g \]

Diagram:
- Voltage sources labeled as \( V_g \)
- Resistance labeled as \( D \)
- Relationship graphed along axis

Useful for?
I_{sec} = \frac{V_o}{R} = i_L

i_p = i_{sec} \frac{N_p}{N_{sec}}

always sums to I_L \oplus 2f_{sw}

i_g = i_{LM} (@ f_{sw}) + i_p (@ 2f_{sw})

---

Always resets Trf. at f_{sw}
due to \frac{V_p}{p} = 2V_g

---

Center tap reference

3 primary currents
\[ V_{sec} = \frac{V_g}{n_p} \]

For \( V_g > 0 \):
- \( D_5 \) on, \( D_6 \) off
  \[ I = I_{load} \]
  \[ I_{D5} = I_{load} \]

For \( V_g < 0 \):
- \( D_5 \) off, \( D_6 \) on

For \( V_g = 0 \):
- \( I_L \) pulls both diodes
  \[ I_{Diode} = \frac{I_{load}}{2} \]
  \[ I_{D5} = I_{D6} = \frac{I_{load}}{2} \]

\[ i_{(secondary)} \]

\[ I_L \]

\[ D \]

\[ D' \]

\[ T_{SW} \] (primary)
Broadcast Family of PolyPhase DC/DC Controllers

LT3731 supports 12-phase operation and 240A output

- Low Output Noise and Less Output Flicker
- Fixed Frequency Operation

- Smallest Inductors and MOSFETs
- Lowest Thermal Stress
- 55% Current Balancing

V \text{IN} = 4.5V to 36V

No Heat Sinks

Atmel Size

Up to 600kHz/Phase

Synchronizable

No Need for External FET Driver ICs

Integrated MOSFET Drivers

Small Solution Size

60A, NO HEAT SINKS
Replace two Q by two C!

You lose \( \frac{1}{2} V_g \) of drive.

Again you lose \( \frac{1}{2} \) of drive.
<table>
<thead>
<tr>
<th>Benefit/Application</th>
<th>Driver</th>
<th>Controller</th>
<th>Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-output/multi-output power</td>
<td>Optional</td>
<td>LM5642, LM5630</td>
<td>Full-bridge</td>
</tr>
<tr>
<td>High efficiency/high performance</td>
<td>(2) LM5100</td>
<td>LM5630</td>
<td>Half-bridge</td>
</tr>
<tr>
<td>High efficiency/medium performance</td>
<td>(1) LM5100</td>
<td>LM5630</td>
<td>Push-Pull</td>
</tr>
<tr>
<td>High efficiency/medium performance</td>
<td>Not Required</td>
<td>LM5630</td>
<td></td>
</tr>
</tbody>
</table>

**Printer**: 6.16

**Note**: Half-bridge drivers and LM5642 dual synchronous buck controller. The LM5630 can be used as chipset with the new 100 V LM5700.
Fig. 7. Driving LEDs require precise timing, duty factor and amplitude.
Integration IA2521 LED Flash Driver

Features:
- Buck-boost, 2.7 - 4.5V input
- 95% efficiency with tiny inductor
- Separately controllable torch
- Flash rise time same as for Xenon tube
- Very low cost!

For more information visit www.integration.com
Or call Integration at (650) 969 4100

Modern Microwave applications.

One of the fastest-growing fabless semiconductor companies in Silicon Valley, Integration designs and delivers tested wafers and packaged ICs for Power Management, RF, and Digital circuits.
All Q off condition for "deadtime"

Given by the full input voltage. A similar situation occurs for the full bridge shown below which also alternatively places $V_{in}$ across the primary winding, but this time using four switches.

**Full Bridge**

We synchronize switches 1 and 4 together in time and then switches 2 and 3. Note that we place the full $V_{in}$ across two switches in series when the timing puts $Sw_{2-3}$ in the same sequence and $Sw_{1-4}$ in the alternative sequence. Hence, we reduce switch voltage stress when we employ the required high input voltage to reach high power levels. Again we have a trade-off as we employ more switches but their individual cost may well be much lower—hopefully a factor of ten.

On the next page we will summarize the switch sequence as well as the voltage ramp on the duty cycle circuit for the full bridge converter topology.

above w/o Secondary C.T.

Next Secondary with C.T.

What does center tap bring to the party?
a. First $T_s$ switch interval: $+V_g$ and zero applied sequentially

There are therefore two $T_{sw}$ intervals one with $+V_g$ and one with $-V_g$ across the primary. Below is that during the first $T_s$ in the primary with $+V_g$. $V_T$ switches between 0 and $V_g$ like non-isolated buck as follows during $T_{sw}$. During $D$ $V_g$ is applied and during $D'$ zero is applied.

Primary (during first $T_s$)

<table>
<thead>
<tr>
<th>During D</th>
<th>During $D'$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1$ &amp; $Q_4$ on</td>
<td>To achieve $V_T = 0$</td>
</tr>
<tr>
<td>$V_T = V_g$</td>
<td>either of two ways:</td>
</tr>
<tr>
<td>$I_m = V_g/L$</td>
<td>1. All $Q_1$ - $Q_4$ off, $V_T = 0$</td>
</tr>
<tr>
<td>$i_{L}(t) = \text{constant if } R_L = 0$</td>
<td>2. $Q_1$, $Q_3$ on, $V_T = 0$</td>
</tr>
</tbody>
</table>

Core reset?

b. Second $T_{sw}$ interval: $-V_g$ and zero applied

The primary circuit looked at during the second $T_s$ timing interval is different $T_{sw} \rightarrow 2T_{sw}$ because $-V_g$ is applied during $D$ and zero during $D'$.
and switch period:

Primary (During $T_s \rightarrow 2T_s$)

- During D
  - $Q_1$ & $Q_2$ on
  - $V_T = -V_g$

- During $D'$
  - Achieve $V_T = 0$
  - by either of two ways:
    1. All $Q_1$-$Q_4$ off
    2. $Q_2$, $Q_4$ on

- So $V_T = 0$
- Equal $V$ on both sides.

- $V_T$ switches between $-V_g$ and 0 in primary.

By symmetry we reset the core of the transformer $L_m$ over $2T_s$.

Up during D of the first $T_s$ and down during D of second $T_s$.

$\langle V_{Lm} \rangle_{2T_s} = 0$

Because of the switching configuration the transformer waveforms are at a frequency $f_s/2$, not at $f_{sw}$.

2. Secondary Voltage $V_s$ Timing:

- During first $T_s$ interval
  - One diode full tilt $I_{sec}$
    - During D
      - $V$ on secondaries
      - is $nV_g = V_s$
      - * on coils tell diode $D_5$ on and diode $D_6$ off

- During second $T_s$ interval
  - $I_{sec}$ per diode
  - Due to flywheel

Find on your own for D $Q_2$, $Q_3$ and $D_6$ are on while for $D'$ diodes $D_5$

- Each diode $I/2$
- Each diode staircase

5
and $D_6$ are on.

2. Input and output currents
   $i_{\text{out}} = i_{D_5} + i_{D_6}$. How it splits is uncertain, but if at anytime it splits equally then: $i_{D_5} = i_{D_6} = \frac{i_{\text{out}}}{2}$.

During first $T_s$ interval $i_{\text{in}}(\text{transformer})$ = ? When $i_{D_5} = i_{D_6}$

- $V_{T} = 0$
- means $V_{GSC} = 0$

At the output $i_{D_5} + i_{D_6}$ while in the primary $i_{D_5}$ causes $n_i D_5$ $i_{D_6}$ causes $n_i D_6$

With all $Q$ off $i_{\text{prim}} = 0$

Review the dot convention on a two turn transformer that says:

- if $n_1 i_1$ is positive $\Rightarrow +n_1$ then
- is negative $\Rightarrow -n_2 i_2$

<table>
<thead>
<tr>
<th>Watch Dots $i_1$</th>
<th>$n_1 i_1 + n_2 i_2 = 0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coming into the dot in secondary and into dot of primary</td>
<td></td>
</tr>
</tbody>
</table>

At the primary on top of the page we have three currents.
- $i_{D_5}$ and $i_{D_6}$ flow in opposite directions with respect to the coil dots:
- $i_{\text{in}}$ and $i_{D_6}$ are assumed flowing into the dot

\[ i_{\text{in}} - n_1 D_5 + n_1 D_6 = 0 \Rightarrow i_{\text{in}} = 0 \]
During the first $T_s$ we find during interval D the two equations below
\[ i_m = i_1 - n_i_d_5 + n_i_d_6 \]  
\[ i(out) = i_{d_5} + i_{d_6} \]
Transformer input
Transformer output
During the second $T_s$ period $T_s \rightarrow 2T_s$ during the same interval D we get the same result for $i_m$ and $i_{out}$. Note in the first $T_s$ with $+V_g$ applied $i_{d_5} \neq 0$ but $i_{d_6} = 0$. Where as in the second $T_s$ with $-V_g$ applied $i_{d_5} = 0$ but $i_{d_6} \neq 0$.

$\Rightarrow$ Switching ripple at $f_s$
$\Rightarrow$ Transformer ripple occurs at $f_s/2$!
Fig. 2: Synchronous rectifier truth table and drive logic.

Control drives required for freewheeling VFD.
Redrawing the single-chip controller as two separate controllers simplifies the analysis of controller operation.

For simplicity, the circuit of Fig. 1 has a common 5-V supply for one another turn on during each phase of a clock cycle.
Fig. 2. Shown here are the waveforms for the Fig. 1 circuit operating under no-load conditions with a common input voltage of 5 V to both controller channels. These waveforms include the switching nodes of the master controller (switching waveform shown on Channel 1) and the slave controller (switching waveform shown on Channel 2), as well as the inductor currents for L1 (Channel 3) and L2 (Channel 4).
Fig. 3. Switching waveforms and inductor currents for the circuit of Fig. 1 are shown here as in Fig. 2 with the circuit operating no-load. However, the input voltage on the master controller (switching waveform shown on Channel 1) has been reduced to 3.3 V, while the input voltage on the slave controller (switching waveform shown on Channel 2) remains at 5 V.

Reduced to 3.3 V, the Channel 1 pulse width at zero load increases to about 3.25 μs. This change reflects ...