Lecture 21
Switch and Parasitic Losses in PWM Converters

A. Passive Rectifier Diode Losses at $f_{SW}$, Active Switch Loss and Driver Circuit Issues

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a. Common Input Drive and Actual circuits
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Parasitic L or C terms

1. \(\frac{di}{dt}\)\(_{max}\) = \(\frac{V_L}{L_p}\), \(L_p\) due to wiring or core leakage flux

2. \(\frac{dv}{dt}\)\(_{max}\) = \(\frac{i_c}{C_p}\), \(C_p\) due to switch devices contiguous wiring, or ground shields

3. Transformer Ringing and example
Passive Rectifier Diode Losses at $f_{SW}$, Active Switch Loss and Driver Circuit Issues

A. Switch and Driver Losses

1. Overview of all Losses and Relative Contributions

We have seen previously that the various converter circuits each have losses that arise from the active switch, the rectifier diode, magnetic loss and other losses such as driver circuit energy loss. Below we summarize the situation for the big eight topologies. The losses are primarily in the switches (90%) but magnetic losses and driver circuit loss also account for 10% of loss. Below we will deal with diode loss in section 1 and active switch loss in section 2. Section 3 covers driver circuit issues.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Power Switch Type</th>
<th>Overall Estimated Efficiency (%)</th>
<th>Power Switch and Drive (%)</th>
<th>Output Rectifier (%)</th>
<th>Magnetic (%)</th>
<th>Miscellaneous (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck</td>
<td>×</td>
<td>72</td>
<td>42</td>
<td>48</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Boost</td>
<td>×</td>
<td>74</td>
<td>55</td>
<td>35</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Buck-boost</td>
<td>×</td>
<td>77</td>
<td>55</td>
<td>35</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Flyback</td>
<td>×</td>
<td>75</td>
<td>48</td>
<td>42</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Half-forward</td>
<td>×</td>
<td>77</td>
<td>48</td>
<td>42</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Push-pull</td>
<td>×</td>
<td>69</td>
<td>50</td>
<td>40</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Half-bridge</td>
<td>×</td>
<td>69</td>
<td>50</td>
<td>40</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Full-bridge</td>
<td>×</td>
<td>65</td>
<td>40</td>
<td>50</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

The losses are primarily in the switches (90%) but magnetic losses and driver circuit loss also account for 10% of loss. Below we will deal with diode loss in section 1 and active switch loss in section 2. Section 3 covers driver circuit issues.
2. Rectifier Diode Losses at $f_{SW}$
   a. Output Filter Capacitance and Storage Charge Effects

Shown below is the output circuit in which the rectifier diode operates for the forward and flyback converter topologies. Note below that the choice of the output capacitor, $C_O$, effects the diode operation as does the values of the diode stored charge, $Q$, and the diode reverse recovery time, $T_{RR}$.

![Output Circuit Diagrams](image)

The output circuits for forward and flyback-mode converters. (a) Center-tapped forward-mode output circuit. (b) Noncenter-tapped (full wave) output circuit. (c) Flyback-mode output circuit.

1. $C_O$ Effects on Rectifier Diode Current

The choice of $C_O$ is often set by the output ripple requirements that we set for the output. This choice for $C_O$ in turn will effect the peak and RMS value of current through the rectifier diode. Hence, the diode loss will depend on $C_O$ choice. Note that the value of $C_O$ will depend on

$$C_O = \frac{I_{out}(\text{max})x(l - D(\text{min}))}{f_{SW}xV(\text{ripple})}$$

The $C_O$ ESR and ESL are parasitic elements which can play a
large role especially in the flyback topology which has no series inductor to limit high current flow into the $C_O$ capacitor. ESR causes the capacitor to get hot and lowers its life in the circuit. ESR also increases the output ripple voltage. ESL with $C_O$ could cause overshoot of the ripple waveforms as we show later in section B of this lecture. A typical overshoot waveform is shown.

2. Storage Charge Effects

Below we will outline both switch delay and additional loss terms in real switches due to diode stored charge.

Diodes release stored charge when they try to turn off. That is for a brief time, $t_{rr}$, with reverse polarity voltage applied we find that diodes still draw large currents, termed reverse recovery currents.

Diodes: $\mu s \leq t_r \leq 30$ nsec

of currents of $\geq 10$ A

- $I_{RM}$ is maximum reverse current the diode conducts.
- $Q_{rr}$ is stored charge in diode released during on cycle.

The first estimate of diode loss is the black box guess based upon average power needs. However, peak and RMS effects will refine this estimate once the circuit waveforms are determined.
The same occurs for SCR circuits, Lecture 22, as shown below. Thyristor has active turn-on but turn-off is like a diode with current going negative to a large peak value due to stored charge. The key delay interval in a thyristor is not $t_{rr}$ but rather $t_Q$, the time from first zero current to the time of zero voltage. In between power loss occurs as we shall see in detail in lecture 22.

![Thyristor Diagram](image)

### b. Three Major Diode Types

There are three major silicon diode technologies to choose from:

- **Schottky** for low $V_F < 0.6$ volts with $T_{RR} =< 10$ ns. However, we cannot block high voltages with Schottky diodes
- **Ultra-fast** with $V_F = 1.0$ volts and with $T_{RR} =< 40$ ns. We have the best trade-off here between the two parameters yet still achieve large blocking voltages
- **Fast** diodes with $V_F = 1.3$ volts and with $T_{RR} =< 140$ ns

Compare $f_{SW}$ diodes with line-frequency diodes which have:
- $V_{on} \approx 0$, but $t_{off} = t_{rr}$ requires $\approx 10-100 \mu s$ for $I_{on}$: 1-10A. Also for line frequency diodes $V$(blocking): 2 kV and $I_{max}$: kA. The fastest power diode at mains frequency has $t_{off} \approx 1$ msec
Slow recovery diodes (line-frequency diodes) have very small forward voltage drop compared to fast recovery diodes. Fast recovery diodes usually have a higher transient forward voltage drop along with a higher on-state voltage as these diodes have gold doping to speed the charge neutralization via extra recombination sites. In short, diode properties are tailored for their ultimate use. A variety of diode types are commercially sold.

<table>
<thead>
<tr>
<th>Diode Technology</th>
<th>$V_F$ (V)</th>
<th>$T_{rr}$ (ns)</th>
<th>$V_{R(max)}$</th>
<th>Relative Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast recovery</td>
<td>1.2-1.4</td>
<td>150</td>
<td>1000</td>
<td>1.0</td>
</tr>
<tr>
<td>Ultrafast recovery</td>
<td>0.9-1.0</td>
<td>25-80</td>
<td>1000</td>
<td>1.4</td>
</tr>
<tr>
<td>Schottky</td>
<td>0.2-0.6</td>
<td>&lt;10</td>
<td>200</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Notice the tradeoff between $V_F$ and $T_{RR}$ in all the devices. We need to choose the smallest $T_{RR}$, the design can afford economically. The forward voltage drop, $V_F$, effects DC conduction loss while $T_{RR}$ effects dynamic loss. The limitation with $V_F$ and $T_{RR}$ is due to the choice of silicon as the diode material and the lack of trench isolation in traditional diode structures. We will cover more about diodes and even SiC as a new material for diode construction in lecture 22. Schottky diodes are the best choice for low dynamic loss, but have limited reverse voltage ratings of 100 volts. We note that at MHz switch frequency that rectifier loss often dominates total losses, while for ultra-low voltages diodes may not even be suitable as discussed below.

c. Diode Selection for Low Voltage Buck

In the flyback circuit below: $D = D' = 0.5$. The flyback behaves like a buck-boost. Does this duty cycle choice provide any variation of the output voltage from duty cycle alone?? So to achieve 3 volts output, we will have to employ the transformer turns ratio as follows.
Compare secondary switch operation with two different choices for the diode and as third choice a synchronous Power MOSFET.

**Bipolar Diode**  
$V_{on} = 0.9$  
$R_{on} = 15 \text{ m}\Omega$

**Schottky Diode**  
$V_{on} = 0.4$  
$R_{on} = 25 \text{ m}\Omega$

**MOSFET**  
$V_{on} = 0$  
$R_{on} = 25 \text{ m}\Omega$

For $D = D'$ the turns ratio is $170/3.3 = 52$ to 1 and $I_{out}(\text{average}) = 25/3.3 = 7.6 \text{ A}$. The secondary current (buck-boost) as well as the diode current equals twice $I_{out}$ or 15.2 A. When the diode is on the total voltage drop across various diodes are:

1. Bipolar Diode: $V_{on} = 0.9 + (15 \text{ m}\Omega) \times 15.2 \text{ A} = 1.13 \text{ V}$
2. Schottky Diode: $V_{on} = 0.4 + (25 \text{ m}\Omega) \times 15.2 \text{ A} = 0.8 \text{ V}$
3. MOSFET: $V_{on} = (25 \text{ m}\Omega) \times 15.2 \text{ A} = 0.4 \text{ V}$

Clearly for Power sources having $V_{out} < 3\text{ V}$ synchronous power MOSFET’s should replace diodes. Most modern microprocessors operate below 3V yet draw over 100 W. MOSFET: In summary, $R_{ON}$ can be m\Omega if we use a big power FET the current, I, may be bipolar and we need not worry about discontinuous mode operation ever occurring.
4. **Active Switch Loss**
   
a. **Overview**
   
Both DC and dynamic losses occur. At low switch frequencies the DC loss dominates while at some switch frequency the AC loss will exceed the DC loss for all higher frequencies. Hence, we can say that only at extremes of $f_{SW}$ will a single loss mechanism dominate. Otherwise, two types of losses occur in real switches: DC loss and dynamic switching loss.

b. **Review of DC Losses**

DC Loss has two parts the on state and the off state.

ON: \[ I_{rms} \cdot R_{ON} \]

OFF: \[ I_{rms} \cdot V_{ON} \]

The comparison of the MOSFET, the IGBT and the bipolar transistor is well known at DC. We repeat this comparison below.
c. Dynamic Active Switch Loss Without Storage Charge

Dynamic switching loss at the switch frequency, \( f_{sw} \), occurs during commutation between the two static states above.

During a \( D + D' = 1 \) switch period four states exist: two are static and two are dynamic.

**Static Energy Loss:** On and off
\[
W_{\text{static}} = W_{\text{on}} + W_{\text{off}}
\]
\[
W_{\text{on}} = \int i_{\text{on}}v_{\text{on}} \, dt \text{ over the } DT_s \text{ on time where } i_{\text{on}} \text{ and } v_{\text{on}} \text{ are usually constant.}
\]
\[
W_{\text{off}} = \int i_{\text{off}}v_{\text{off}} \, dt \text{ over the } D'T_s \text{ off time where } i_{\text{off}} \text{ and } v_{\text{off}} \text{ are usually constant.}
\]

**Dynamic Energy Loss:** On/off and off/on transitions
\[
W_{\text{dynamic}} = W(\text{turn off}) + W(\text{turn on})
\]
Here depending on the circuit topology the switching trajectories maybe quite different for the two transitions. We must calculate \( W_{\text{dynamic}} \) by piecewise integration over each time period.

Total Power Loss = \( DV_{\text{on}}I_{\text{on}} + (1-D)V_{\text{off}}I_{\text{off}} + f_{sw}W_{\text{dynamic}} \)

Clearly as \( f_{sw} \) increases the dynamic loss will at some \( f_{sw}(\text{critical}) \) equal the static loss. Above \( f_{sw}(\text{critical}) \) dynamic switching loss
always dominates.

Now let's calculate $W(\text{dynamic})$ the losses during switching or commutation. To simplify matters first we assume rectangular switching which is characteristic of inductive load as shown:

![Rectangular switch commutation for an inductive load.](image)

This and other cases were solved before in lecture 4 as well as the general case for equal turn-on and turn-off with a commutation parameter “$a$” to find:

$$W(\text{dynamic}) = V_{\text{off}} I_{\text{on}} t(\text{switch}) / a, \quad 1.2 \leq a \leq 6$$

When unsure $a = 2$ is a good first guess. The major unknown is $t(\text{switch})$ which varies from device to device.

- $t(\text{MOSFET}) = 10 - 100$ ns (fast)
- $t(\text{diode or thyristor}) = 1 - 20$ µs (slow)

Below we assume linear switching where losses occur twice each $T_s$ period due to rising and falling currents and voltages during the on/off and off/on transitions. The DC current source in the switch circuit below could represent inductive current flow that is not interrupted immediately by a change initiated on the switch caused by the control signal.

Hence the turnoff voltage of the transistor is large before the current is zero as shown below:

- During switch turn-on $t_{ri}$ is the linear ramp current rise while $t_{fr}$ is the linear ramp voltage fall. During switch turn-off $t_{vr}$ is the voltage rise time and $t_{fi}$ is the current fall time.
For DC switch conditions:
1. \( W_{sw}(on) = \frac{V_{di0} ton}{2} \)
2. \( W_{sw}(off) = \frac{V_{di0} toff}{2} \)

For AC switch conditions:
Note that:
\( t_{off} = t_{rv} + t_{fi} \)
1. \( W_{sw}(off) > W_{sw}(on) \) due to large values of \( t_{fi} \)
\( t_{on} = t_{ri} + t_{fu} \)
2. \( W_T = W(on) + W(off) \)
\( P_T = W_{fs} \)

D. Dynamic Active Switch Loss With Storage Charge

In the converter topology below the diode stored charge, \( Q_{rr} \), makes switching loss even worse, especially for transistor turn-on and diode turn-off. Incidentally, the diode will fail if \( di/dt \) and \( dv/dt \) are too big (creating an internal hot spot in the center of the pn-junction, since the recombination in the diode junction is slower at the edges.). The \( Q_{rr} \) divided by \( t_{rr} \) for the diode causes a big peak current \( i_r = Q_{rr}/t_{rr} \). Snap recovery diodes have small \( t_{rr} \) but big \( i_{rr} \) whereas soft recovery diodes have bigger \( t_{rr} \) and lower \( i_{rr} \). Every switch choice has its implications.
Reverse diode \( i \) flows through the transistor

\[
\int i_D \, dt \rightarrow Q_r \text{ (total stored charge)}
\]

If \( t_1 - t_2 \rightarrow 0 \) (super fast diode)
then \( V_A = V_g \)

\[ i_A = i_L - i_B \]

The transistor switching energy is:

\[
W = \int V_g (i_L - i_D) \, dt = V_g i_L t_r + V_g Q_r
\]

\[ P = W_T f_{sw} \]

To reduce \( W \) we tend to use faster response diodes with \( t_r \rightarrow 0 \) and hence a minimum of stored charge \( i_d t_r = Q_r \) occurs. Super fast diodes, that employ gold doping to achieve low \( t_r \), do have other problems. What are they?? Again we trade off \( V_{ON} \) and \( t_r \).
In addition we find with low $t_r$ diodes we find:
1. Higher on Voltage in steady state
2. Even bigger transient forward voltage drops at initial turn on
3. More possibility for diode ringing and EMI
Different diode suppliers make other compromises for performance!

4. Switch Drives for MOS Based Switches
   a. Overview
Switches control 100-1000 times the power level of their losses. So a switch can control 100 kW with only 100 watts loss.
All of the driver circuits we will discuss below are based upon the MOS input circuit. This applies to MOSFET’s, IGBT’s and MOS controlled thyristors(MCT’s). The last will be covered in lecture 22.
We therefore know that the waveforms at the gate as regards voltage and current will look as shown on page 15 because of a Common Input Circuit.

See the following page for a set of waveforms for the MOS gate input. The driver circuit will provide only nanoamperes in steady state but Amperes of pulsed turn-on and turn-off peak current. This condition is unique to MOS input gates.

The best way to achieve the above requirements is to employ a bipolar Totem-pole driver that switches between the rails as we will see below in part b. That is we alternatively apply + and – $V$(rail) to the input gate. This is a precarious situation as the wire lead to the gate has some inductance and the MOS input has capacitance. As a consequence, we have a series L-C that is asked to handle very large currents. This is a condition that will easily oscillate, causing the gate voltage to vary widely and out of control at the resonant frequency set by L-C and not by the switch frequency. We will see this situation later. For now we will neglect the series L-C circuit on the gate input.
The figure below captures the waveforms on a MOSFET, an IGBT as well as a MCT input stage, neglecting the series L-C. Note that:

- $V_{GS}$ is typically 10 volts to achieve full-on. $V_{GS} = 20$ is ok

- The input looks like a capacitor which means you need HIGH charging and discharging currents but LITTLE DC current

- The Miller capacitance across the gate to drain is amplified by any gain and opposes the gate drive to cause the plateau on the gate waveforms
b. Driver Circuits

Buffering the control IC for driving MOSFETs at higher frequencies or those MOSFETs with a large $C_{GS}$.

(a) Driving a power MOSFET from an uncommitted transistor output.
(b) Driving a power MOSFET from a totem-pole driver.
(c) Transformer-coupled power MOSFET driver.

Above we give three suitable driver circuits for MOS switches. A series gate resistor is recommended on the MOSFET—can you tell why?
B. Parasitic L and C effects also cause switch loss

1. Overview

\[ \frac{1}{2} L*i^2 \text{ from wiring or leakage inductance of a core stores energy during on-time, current peaks} \]

Device capacitance will charge, storing energy \( \frac{1}{2}CV^2 \)

\[ L_p \text{ is fixed by wiring, core leakage, and packages} \]

\[ L(wiring) \approx 5nH/cm \text{ (typical)} \]

\[ C_p \text{ depends on the solid state device chosen. Usually } C_{DS} \approx \frac{C_0}{\sqrt{V_{ds}}} \]

These stored energies will also be lost during switching and switches themselves will be additionally stressed due to large peak V and I values during transitions.

\[ L_p \text{ also limits } \left( \frac{di}{dt} \right)_{\text{max}} = \frac{V}{L} \]

\[ C_p \text{ also limits } \left( \frac{dv}{dt} \right)_{\text{max}} = \frac{i}{C} \]

\[ L_p \text{ and } C_p \text{ acting together cause resonant ringing effects with excessive } V \text{ and } I \text{ beyond those expected without ringing} \]
2. Erickson Problem 4.9

For a switching frequency of 10 kHz, engineers measured $I_{Lp}$, $V_{Cp}$ and damped ringing @ 5 MHz. By measuring peak values and $\omega$ of ringing we can estimate energy that is ringing.

Parasitic circuit causes ringing.
Damped oscillation tells us that there is also a series $R$

The measured quantities are:

- $i_{Lp} = 0.5A$
- $v_{Cp} = 200V$

For resonance: $\omega_r = \frac{1}{\sqrt{LC}} = 5MHz$

$\sqrt{\frac{L}{C}} = \text{characteristic impedance which is } 400 \, \Omega.$

$R_o = \frac{200 \, V}{1/2 \, A} = 400\Omega$

$\Rightarrow L_p = 12.7 \, mH, \, C_p = 79.6 \, pF$

The energy oscillates between the $L$ and $C$ but the series $R$ causes power dissipation as it oscillates between them.

$E_{sw}(\text{lost to ringing}) = 1/2 \, Cv^2 = 1/2 \, Li^2$

$E_{sw} = 1.6\mu J \text{ each occurrence}$
$f_{sw}$ sets off the onset ringing each $T_s$ seconds

$P_{sw} = E_{sw} \cdot f_{sw} = 100 \text{ kHz}$
$P_{sw} = 0.16 \text{ Watts}$

In general given the two frequencies being such that $f_r >> f_{sw}$, we find:

$$P_{sw} = f_{sw} \cdot \frac{1}{2} i_L^{(\text{peak})} \frac{V_L^{(\text{peak})}}{2\pi f_r i_L^{(\text{peak})}}$$

$$= \left( \frac{f_{sw}}{f_r} \right) \frac{i_{pk} V_{pk}}{4\pi}$$

3. GATE Waveform **OSCILLATION** due to parasitics

We will show on the next two pages that the wire into the gate itself has a parasitic inductance associated with it. When included into the gate circuit, which has input capacitance, we have a series L-C circuit which could oscillate, causing the switch to repeatedly toggle on and off at the L-C resonant frequency, not at $f_{sw}$. This oscillation is undesired as it causes undesired additional switch losses.

We will show on page 20 the case WITH NO BASE RESISTANCE. Then on page 21 we will add base resistance to remove the oscillation from the gate and get a step waveform at the gate, thereby avoiding the undesired toggling of the switch at the resonant frequency. Turn the pages and peruse the results.
Next we add series gate resistance to purposefully slow down the gate switching and eliminate the L-C resonant behavior. This returns us to the case of gate voltages crisply changing at $f_{SW}$. 
Ciss=22n

L3 75n
R4 2
M3

V1 PULSE -5 15 2U 1N 1N 5U 10U

add series R