1. The amplifier shown below is biased to operate at $g_m = 1 \text{ mA/V}$. The voltage gain of the circuit is limited at the lower end by the source degeneration (DC gain) and at the high end by the transistor speed limitation. The gain roll-off at the lower frequency is determined by the RC constant at the source node of the transistor. i.e.

$$f_L = \frac{1}{2\pi \left( \frac{1}{g_m R_s} \right) C_s}$$

Neglecting $r_o$ (i.e. $r_o$ is infinite), 1). find the DC gain. 2). find $C_s$ value that places $f_L$ at 20 Hz.

![Amplifier Circuit Diagram](image)

2. The NMOS transistor in the common source amplifier circuit shown below is biased to have $g_m = 5 \text{ mA/V}$. Assume transistor output impedance is significantly higher than the load resistance.

![NMOS Amplifier Circuit Diagram](image)
1). Find overall midband voltage gain of the circuit, $A_M$, when the input coupling capacitor to $V_{sig}$ is feeding $V_{sig}$ to the amplifier input without any loss.
2). Find roll-off frequency caused by the input coupling capacitor and the total resistance at the transistor gate node, $f_{p1}$.
3). Find $f_L$ caused by the capacitor at the source node of the transistor and the total resistance at the source node. (we also call this $f_{p2}$).
4). Find output roll-off frequency caused by the capacitor at the drain node of the transistor and the total resistance at the drain node, $f_{p3}$.

3. Consider the low-frequency response of the common source amplifier shown below. Let $R_{sig} = 0.5M\Omega$, $R_G = 2M\Omega$, $g_m = 3mA/V$, $R_D = 20k\Omega$, $R_L = 10k\Omega$. Ignore $r_o$, find $A_M$. Also, design the coupling and bypass capacitors to locate the three low-frequency poles at $f_{p1} = 3Hz$, $f_{p2} = 50Hz$, and $f_{p3} = 10Hz$, with capacitors specified only to a single significant digit.