1. In an active-loaded differential amplifier of the form shown in figure (a), all transistors are characterized by $k'(W/L) = 3.2 \text{ mA/V}^2$, and $|V_A| = 20\text{V}$. Find the bias current $I$ for which the gain $v_o/v_{id} = 100\text{V/V}$.

2. Consider the active-loaded MOS differential amplifier of figure (a) in two cases:
   a) Current source $I$ is implemented with a simple current mirror.
   b) Current source $I$ is implemented with the modified Wilson current mirror shown in the figure (b).

   For the simple mirror $R_{SS} = r_0|Q_S$ and for the Wilson mirror $R_{SS} \approx g_m r_d r_o S$, and assuming that all transistors have the same $|V_A|$ and $k'(W/L)$, show that for case (a) $CMRR = 2(V_A/V_{OV})^2$ and for case (b) $CMRR = 2\sqrt{2}(V_A/V_{OV})^3$, where $V_{OV}$ is the overdrive voltage that corresponds to a drain current of $I/2$. For $k'(W/L) = 10\text{mA/V}^2$, $I = 1\text{mA}$, and $|V_A| = 10\text{V}$, find CMRR for both cases (in dB).

3. Consider an active-loaded differential amplifier figure (a) with the bias current source implemented with the modified Wilson mirror of figure (b) with $I = 200\mu\text{A}$ (shown below). The transistors have $|V_t| = 0.5\text{V}$ and $k'(W/L) = 5 \text{ mA/V}^2$. What is the lowest value of the total power supply $(V_{DD} + V_{SS})$ that allows each transistor to operate with $|V_{DS}| \geq |V_{GS}|$? (Wilson
mirror has the same output impedance as the cascode mirror. The minimum power supply voltage allowed can be calculated assuming that Vds and Vgs for all the transistors are the same.

3.

4. Consider the circuit in the figure shown below with the device geometries, in μm, shown in the table. Let $I_{REF} = 225\mu A$, $|V_t| = 0.75V$ for all devices, $\mu n C_{ox} = 180\mu A/V^2$, $\mu p C_{ox} = 60\mu A/V^2$, $|V_{A}| = 9V$ for all devices, $V_{DD} = V_{SS} = 1.5V$.

Determine the width of $Q_6$, $W$, that will ensure that the op amp will not have a systematic offset voltage (i.e. $(W/L)_6/(W/L)_4 = 2^* ((W/L)_7/(W/L)_5))$. Then, for all devices evaluate $I_D$, $|V_{OV}|$, $|V_{GS}|$, $g_m$, and $r_o$.

Provide your results in a table similar to the table below. Also find $A_1$ (the DC gain for the first stage amplifier), $A_2$ (the DC gain for the second stage amplifier), the open-loop voltage gain (i.e. the DC gain of the entire circuit), the input common-mode range, and the output voltage range. Neglect the effect of $V_A$ on the bias current.

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<table>
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<tr>
<th>Transistor</th>
<th>$Q_1$</th>
<th>$Q_2$</th>
<th>$Q_3$</th>
<th>$Q_4$</th>
<th>$Q_5$</th>
<th>$Q_6$</th>
<th>$Q_7$</th>
<th>$Q_8$</th>
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<tbody>
<tr>
<td>$W/L$</td>
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<td>30/0.5</td>
<td>10/0.5</td>
<td>10/0.5</td>
<td>60/0.5</td>
<td>W/0.5</td>
<td>60/0.5</td>
<td>60/0.5</td>
</tr>
</tbody>
</table>