1. Sketch the p-channel counterpart of the current-source circuit in the figure shown below. Note that the circuit should more appropriately be called a current sink, the corresponding PMOS circuit is a current source. Let $V_{DD} = 1.8\, V$, $|V_t| = 0.5\, V$, $Q_1$ and $Q_2$ be matched, and $\mu_p C_{ox} = 100\mu A/V^2$. Find the device $W/L$ ratios and the value of the resistor that sets the value of $I_{REF}$ so that a nominally 80$\mu A$ output current is obtained. The current source is required to operate for $V_o$ as high as 1.6V. Neglect channel-length modulation.

2. For the current-steering circuit shown in the figure below, find $I_o$ in terms of $I_{REF}$ and device $W/L$ ratios of four transistors.
3. The current-steering circuit shown in the figure below is fabricated in a CMOS technology for which \( \mu_n C_{ox} = 200 \mu A/V^2 \), \( \mu_p C_{ox} = 80 \mu A/V^2 \), \( V_{tn} = 0.6 V \), \( V_{tp} = -0.6 V \), \( V'_{An} = 10 V/\mu m \), \( |V'_{Ap}| = 12 V/\mu m \). If all devices have \( L = 0.8 \mu m \), design the circuit so that \( I_{REF} = 20 \mu A \), \( I_2 = 100 \mu A \), \( I_3 = I_4 = 20 \mu A \), and \( I_5 = 50 \mu A \). Use the minimum possible device widths needed to achieve proper operation of the current source \( Q_2 \) for voltages at its drain as high as +1.3V and proper operation of the current sink \( Q_5 \) with voltages at its drain as low as -1.3V. Specify the widths of all devices and the value \( R \). Find the output resistance of the current source \( Q_2 \) and the output resistance of the current sink \( Q_5 \).