Thermal-Sensitive Design and Power Optimization for a 3D Torus-Based Optical NoC

Kang Yao*, Yaoyao Ye*, Sudeep Pasricha†, Jiang Xu‡
*Dept. of Micro/Nano Electronics, Shanghai Jiao Tong University, Shanghai, China
†Dept. of Electrical and Computer Engineering, Colorado State University, Fort Collins, CO, USA
‡Dept. of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong, China

***Abstract*—In order to overcome limitations of traditional electronic interconnects in terms of power efficiency and bandwidth density, optical networks-on-chip (NoCs) based on 3D integrated silicon photonics have been proposed as an emerging on-chip communication architecture for multiprocessor systems-on-chip (MPSoCs) with large core counts. However, due to thermo-optic effects, wavelength-selective silicon photonic devices such as microresonators, which are widely used in optical NoCs, suffer from temperature-dependent wavelength shifts. As a result, on-chip temperature variations cause significant thermal-induced optical power loss which may counteract the power advantages of optical NoCs. To tackle this problem, in this work, we present a thermal-sensitive design and power optimization approach for a 3D torus-based optical NoC architecture. Based on an optical thermal modeling platform which models the thermal effect in optical NoCs from a system-level perspective, a thermal-sensitive routing algorithm is proposed for the 3D torus-based optical NoC to optimize its power consumption in the presence of on-chip temperature variations. Simulation results show that in an 8x8x2 3D torus-based optical NoC under a set of real applications, as compared with a matched 3D mesh-based optical NoC with traditional dimension order routing, the power consumption is reduced by 25% if thermal tuning for microresonators is not utilized, by 19% if thermal tuning is utilized for microresonators, and by 17% if athermal microresonators are used.**

***Index Terms*—Optical network-on-chip, chip multiprocessor, thermo-optic effect, temperature sensitivity.**

I. Introduction

As the scale of transistors enters the deep nanometer region, the number of transistors available on a single chip has increased to several billions. By enabling energy-efficient parallel processing at lower clock frequencies, multiprocessor systems-on-chip (MPSoCs) are a natural platform for embedded systems as well as high-performance computing. Network-on-chip (NoC) architectures have been widely proposed as a new generation of on-chip communication architectures, which could scale better than on-chip shared buses and ad-hoc networks as the number of cores increases [1], [2]. However, due to the limitations of traditional electronic interconnects in power efficiency and bandwidth density, as well as issues of high-frequency crosstalk noise and parasitic capacitance in deep-submicron integrated circuit design, there are still bandwidth, power efficiency and reliability bottlenecks in traditional NoCs based on electronic interconnects.

This work is sponsored by Shanghai Sailing Program, and NSFC (Project 61602298).

Corresponding author: Yaoyao Ye. Email: yeyaoyao@sjtu.edu.cn

With the booming developments in nanoscale silicon photonic technologies for short-haul communications, silicon photonics based optical interconnects are emerging as a promising new approach to moving on-chip data at high speeds and low power. Compared to traditional electronic interconnects, optical interconnects can enable significantly increased bandwidth density, low power consumption, and low latency. By integrating optical interconnects in NoC architectures, optical NoCs can overcome many of the most serious on-chip communication issues [3]–[7]. Most of the prior works on optical NoCs are based on silicon photonic devices including optical waveguides and silicon microresonators (MRs). Considering the high efficiency of electronic interconnects in on-chip local communication as well as for control, optical NoCs are often controlled and configured in the electronic domain. Three-dimensional (3D) integration technologies provide the support for realizing mixed-technology electronic-controlled optical NoCs [8].

However, one of the major challenges in optical NoC designs is thermal sensitivity, which is an intrinsic characteristic of photonic devices. Due to the fact that the power density on chip is uneven and the thermal conductivity of packaging materials is limited, chip temperature fluctuates temporally as well as spatially. The temperature can rise quickly from room temperature after a cold start, and vary by more than 30^oC across a steady-state chip under typical operating conditions [9]. As a result of thermo-optic effects, wavelength-selective silicon photonic devices such as microresonators, which are widely used in optical NoCs, suffer from temperature-dependent wavelength shifts [10]. The emission wavelength of on-chip lasers, such as VCSELs (vertical cavity surface-emitting lasers), also shifts with ambient temperatures [11], while the power efficiency degrades at high temperatures [12]. The thermal related wavelength mismatch between the laser located in the source node and the microresonators in intermediate nodes along a photonic path can cause significant additional optical power loss. An investigation of related thermal issues shows that if we take the thermal regulation power into account, optical interconnects may not have advantages in power efficiency as compared with their electrical counterparts [13]. In order to mitigate thermal effects in optical NoCs, run-time thermal management techniques such as OS-based workload migration and DVFS (dynamic voltage and frequency scaling) have been proposed

to reduce the on-chip temperature gradients [14]–[16]. Due to the limitations of these thermal management techniques, device-level thermal compensation techniques are still in need. Thermal tuning by local microheaters is one such device-level solution, however, it is relatively slow and power inefficient [17], [18]. Additionally, microresonators with low temperature dependence as well as athermal microresonators have been demonstrated by applying proper polymer materials [19], [20]. However, there are still compatibility issues when implementing athermal microresonators with CMOS technology. Furthermore, some efforts have been made to overcome the thermal challenges in optical NoCs from system-level perspectives [16], [21]–[26]. In [23], the authors proposed a thermal-aware methodology to design optical NoCs with distributed CMOS-compatible VCSELs, based on steady-state thermal simulations and SNR (signal-to-noise ratio) analysis. In [21], [22], the authors systematically modeled thermal effects in optical NoCs and proposed several low-temperature-sensitivity techniques. In [24], a system-level proactive thread migration technique and a device-level thermal island framework were proposed to alleviate the thermal issues in optical NoCs.

To further tackle the thermal issue in optical NoC designs, in this work, we present a novel thermal-sensitive design and power optimization approach for a 3D torus-based optical NoC architecture in the presence of on-chip temperature variations. The rest of the paper is organized as follows. In Section II, we present the proposed thermal-sensitive design and power optimization methodology. Section III presents simulation results and comparisons in terms of thermal-induced energy efficiency and network performance. Last, Section IV concludes.

II. Thermal-Sensitive Design and Power Optimization

In this section, we propose a thermal-sensitive design and power optimization approach for a 3D torus-based optical NoC architecture (Figure 1). Based on optical thermal models that characterize thermal effects in optical NoCs from a system-level perspective, a thermal-sensitive routing mechanism is proposed for the 3D torus-based optical NoC to optimize its power consumption in the presence of on-chip temperature variations.

A. 3D Torus-based optical NoC architecture

Regular network topologies, such as mesh and torus, are preferred in NoC designs because of their predictable scalability in terms of performance and power consumption. In order to improve the NoCs performance with shorter interconnection lengths, NoC architectures based on 3D network topologies have been proposed [27]–[29]. It has been demonstrated that as compared to its 2D implementation, the 3D mesh-based NoC can improve performance significantly with higher integration densities and smaller footprints. As compared to 3D mesh topology, the 3D torus topology takes advantage of the wrap-around links among edge nodes to offer better path diversity and better load balance.

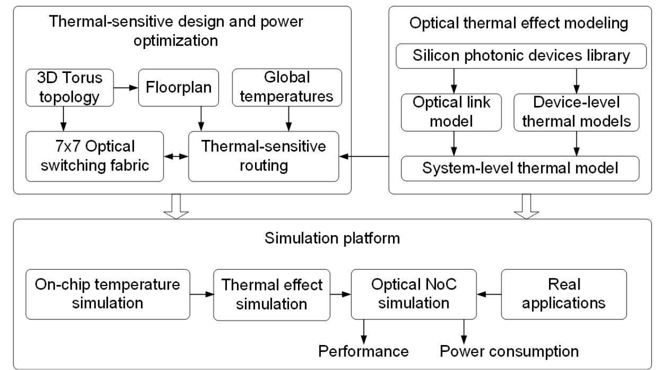

Fig. 1. The proposed thermal-sensitive design and power optimization approach for a 3D torus-based optical NoC architecture

Figure 2 shows the topology of a 3D torus-based optical NoC architecture, where each router is connected to a local processor core. Each processor is assigned a unique ID of (x_i, y_i, z_i) for addressing, and the local router has the same address. The proposed 3D torus-based optical NoC uses circuit switching, in which an optical path is reserved before payload transmission. An overlapped electronic control network is used for optical path configuration and maintenance. Before a packet transmission, a single-flit path-setup packet would be routed in the electronic control network for path reservation. The payload data is transmitted along the reserved optical path after the path setup. High-speed optical transmission is achieved in this architecture without buffering in intermediate routers.

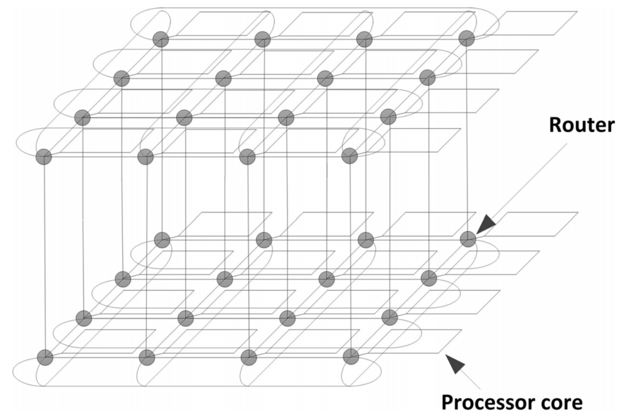

Fig. 2. A 3D torus-based optical NoC architecture

B. Hybrid optical-electronic router architecture

In the 3D torus-based optical NoC, hybrid optical-electronic routers are used to interconnect processor cores. The hybrid optical-electronic router architecture (Figure 3) is composed of a 7×7 fully-connected optical switch, an electronic control unit, and an electronic/optical (E/O) interface. The electronic control unit includes a thermal-sensitive routing unit and an adaptive power control unit. The 7×7 fully-connected

optical switch is responsible for directing optical signals in the network, while the electronic control unit implements the routing algorithm and power control. In addition, the electronic control units in the network are interconnected into an electronic control network with metallic interconnects for control purposes, which includes selecting optical path configurations and delivering temperature information. The E/O interface, which is in charge of serialization, deserialization, and E/O conversions, is used to facilitate communications between the electronic and optical domain.

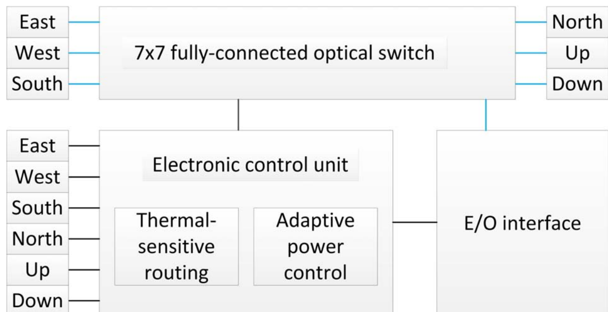

Fig. 3. A hybrid optical-electronic router architecture

In [29], a reduced 7×7 optical switch was proposed specially for dimension-order routing in a 3D mesh-based optical NoC. In this paper, we extend it to a 7×7 fully-connected optical switch (Figure 4), which can support any routing algorithms including the newly proposed thermal sensitive routing scheme. The 7×7 fully-connected optical switch is built from basic optical switching elements (BOSEs) which are based on wavelength-selective microresonators, optical waveguides, and optical terminators [29]. By powering on/off the microresonator, the basic optical switching element implements 1x2 optical switching functions. The 7×7 fully-connected optical switch has seven bidirectional ports, including injection/ejection, up, down, east, west, south, and north ports. The local processor core is connected by the injection/ejection ports through an O/E interface while other ports are connected to neighboring optical switches. The proposed 7×7 fully-connected optical switch inherits the low-loss feature from the reduced 7×7 optical switch [29]. The ports are aligned to their intended directions. Compared to the reduced 7×7 optical switch for dimension-order routing only proposed in [29], our new port-to-port switching functions in the proposed 7×7 fully-connected optical switching fabric include switchings from south to east/west, from north to east/west, from up to east/west/south/north, from down to east/west/south/north.

C. Thermal-sensitive Routing for Power Consumption Reduction

The traditional dimension-order routing (e.g. XYZ routing) is a low-complexity deterministic algorithm, which is particularly suitable for mesh or torus-based networks. Its simplicity and efficiency is due to the fact that it is a deterministic routing approach which determines a path with minimum information (the source address and the destination address). However according to our previous studies, the worst-case thermal-induced power consumption of deterministic dimension order routing is significant in the presence of on-chip temperature variations. In this section, we propose a thermal-sensitive routing mechanism which selects a path according to runtime on-chip temperature conditions. By avoiding paths with severe thermal-induced optical power loss, the power consumption for a packet transmission can be significantly reduced.

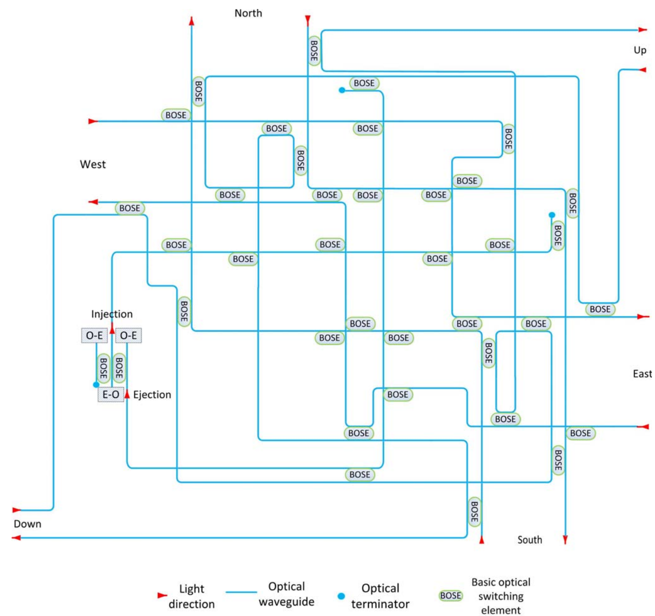

Fig. 4. A 7x7 fully-connected optical switching fabric

1) Optical thermal model: As a result of the thermo-optic effect, material refractive index is temperature dependent and follows Equation (1), where n_0 is the refractive index at room temperature, dn/dT is the thermo-optic coefficient of the material, and ΔT is the temperature variation. Physical measurements show that the thermo-optic coefficient of silicon is on the order of $10^{-4}/K$ and is nonlinear over a large temperature range at 1550nm wavelength [30].

$$n = n_0 + \frac{dn}{dT}\Delta T \tag{1}$$

The thermo-optic effect will cause changes in the device characteristics. As shown in Equation (2), the resonant wavelength of a single-microresonator basic optical switching element λ_{BOSE} shifts approximately linearly with temperature T_{BOSE}, where λ_{BOSE_0} is the resonant wavelength at room temperature T_0, and ρ_{BOSE} is defined as the temperature-dependent wavelength shift of the basic optical switching element.

$$\lambda_{BOSE} = \lambda_{BOSE_0} + \rho_{BOSE}(T_{BOSE} - T_0) \tag{2}$$

As shown in Equation (3), the lasing wavelength of VCSELs λ_{VCSEL} also red-shifts approximately linearly with temperature T_{VCSEL}, where λ_{VCSEL_0} is the lasing wavelength

at room temperature T_0, and ρ_{VCSEL} is defined as the temperature dependent wavelength shift of VCSEL.

$$\lambda_{VCSEL} = \lambda_{VCSEL_0} + \rho_{VCSEL}(T_{VCSEL} - T_0) \quad (3)$$

Besides, the output power of a VCSEL degrades at higher operating temperatures. Assuming that the VCSEL is driven by current I which is above the threshold but before the point where the output power starts to decrease with the current, we can express the output optical power P_{out} by Equation (4), where I is the driving current, α is the minimum threshold current, T_{th} is the temperature at which the threshold current is the minimum, β is a coefficient related to the temperature dependance of the threshold current, ε is the slope efficiency at 0^oC, and γ is a positive coefficient.

$$P_{out} = (I - \alpha - \beta(T_{VCSEL} - T_{th})^2)(\varepsilon - \gamma \cdot T_{VCSEL}) \quad (4)$$

If using an off-chip VCSEL as the laser source, the lasing wavelength can be fixed by equipping with a temperature control unit. If using an on-chip VCSEL as the laser source, the temperature-dependent wavelength shift and power efficiency degradation should be taken into account in the thermal model.

Temperature variations across the chip will result in wavelength mismatches between the laser wavelength and the resonant wavelengths of intermediate switching elements in the path. As shown in Equation (5), the wavelength mismatch results in additional optical power loss (in dB) in switching. 2δ is the 3-dB bandwidth of the basic optical switching element, κ^2 is the fraction of power coupling between the waveguide and the ring, and κ_p^2 is the power loss per round-trip of the ring [31]. When $2\kappa^2 \gg \kappa_p^2$, nearly full power transfer can be achieved at the peak resonance, exhibiting a low insertion loss. A deviation from the peak resonant wavelength would result in more power loss in an active switching especially if with a narrow 3-dB bandwidth. For a basic optical switching element working at the 1550nm wavelength range, if the quality factor is on the order of 5000, a 10^oC temperature change would make the power spectrum shift about *0.5nm* and result in a power loss variation of about *10dB*.

$$L = 10log((\frac{2\kappa^2 + \kappa_p^2}{2\kappa^2})^2 \cdot (1 + \frac{(\lambda_{VCSEL} - \lambda_{BOSE})^2}{\delta^2}) \quad (5)$$

2) Thermal-sensitive routing: Based on the optical thermal models presented above, we propose a thermal-sensitive routing mechanism to reduce thermal-induced power consumption in the presence of on-chip temperature variations. The routing algorithm determines a path to transmit a packet from the source to the destination. In traditional deterministic routing such as dimension-order routing, a deterministic path is decided based only on the source address and the destination address. However, in the presence of on-chip temperature variations, some paths which are under high temperature variations suffer from severe optical power loss. In order to avoid such paths, we propose to introduce adaptiveness in routing by considering on-chip temperature conditions when making routing decisions.

Figure 5 shows the proposed thermal-sensitive routing unit. It is composed of a shortest path routing unit, a temperature table, and an optical thermal-effect modeling unit. The proposed thermal-sensitive routing works as a source routing mechanism. It needs global temperature information to make routing decisions, so the overhead of this routing algorithm includes the on-chip temperature sensing and the broadcasting of global temperature information. For each packet to be transmitted, the shortest path routing unit reads the header flit of the packet to get the source id and destination id, and then it finds out the shortest paths between the source and destination. The found shortest paths are considered as candidate paths, and they will be compared for thermal-induced optical power loss by the optical thermal-effect modeling unit. The temperature table keeps the global temperature information at the granularity of each processor core. Considering that the on-chip temperature could fluctuate temporally, the temperature table will receive updates from other nodes. The optical thermal-effect modeling unit gets all the candidate paths information from the shortest path routing unit, and reads the temperature table for global temperature information. It then calculates the thermal-induced optical power loss for each candidate path, according to the optical thermal models presented in the previous section. The path with the minimum thermal-induced optical power loss will be selected out of all the candidate paths.

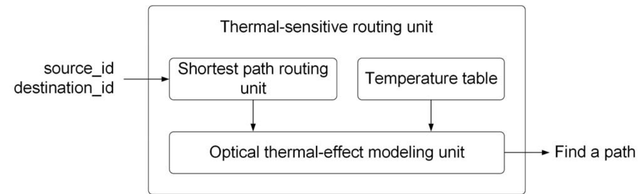

Fig. 5. The proposed thermal-sensitive routing unit

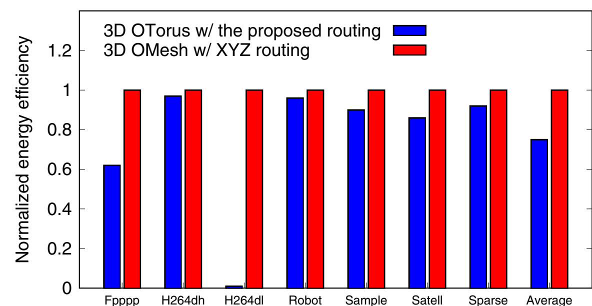

Fig. 6. Normalized energy efficiency for real applications, without thermal tuning, $0.62nm$ 3-dB bandwidth

III. SIMULATION RESULTS AND COMPARISONS

We evaluated the energy efficiency and performance of a 3D 8x8x2 torus-based optical NoC. We assumed 40Gbps data-link bandwidth. In order to show the advantages of the proposed 3D torus-based optical NoC with thermal-sensitive routing, we

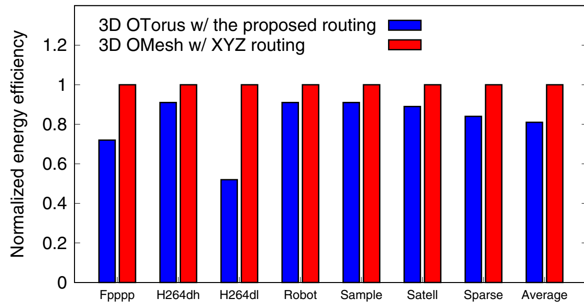

Fig. 7. Normalized energy efficiency for real applications, with thermal tuning, $0.62nm$ 3-dB bandwidth

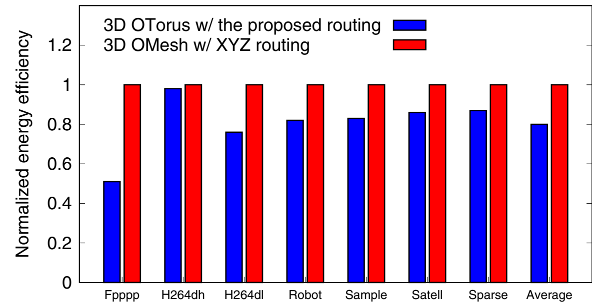

Fig. 10. Normalized energy efficiency for real applications, with thermal tuning, $0.775nm$ 3-dB bandwidth

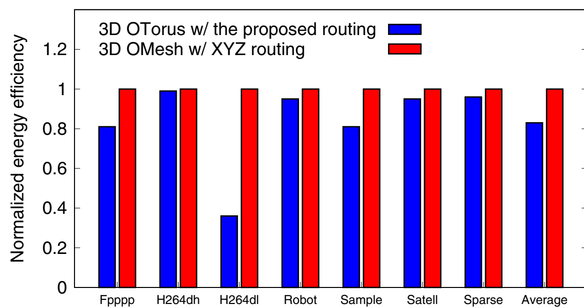

Fig. 8. Normalized energy efficiency for real applications, with athermal MRs, $0.62nm$ 3-dB bandwidth

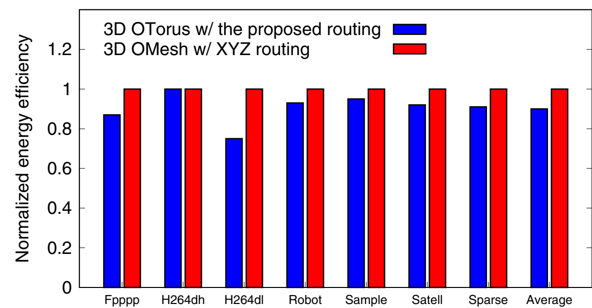

Fig. 11. Normalized energy efficiency for real applications, with athermal MRs, $0.775nm$ 3-dB bandwidth

use a matched 3D 8x8x2 mesh-based optical NoC with the traditional XYZ routing as a baseline for comparison. SystemC-based cycle-accurate simulators are developed for network simulations of the proposed 3D torus-based optical NoC and the baseline 3D mesh-based optical NoC. Network simulations are conducted under several real applications including FPPPP, H263E, H264DH, H26DL, ROBOT, SAMPLE, and SPARSE. For each application, traffic information is used to simulate the on-chip temperature distributions by McPAT [32] and HotSpot [33]. Two traditional techniques have been proposed to compensate for the temperature-dependent wavelength shift in microresonators, including the active thermal tuning with local microheaters and the passively temperature-compensated athermal microresonators [17] [20]. The athermal microresonators usually have a limited range of working temperatures, beyond which the microresonators would be thermal sensitive. In our case study, we assume that the athermal microresonators are working within their required temperature range.

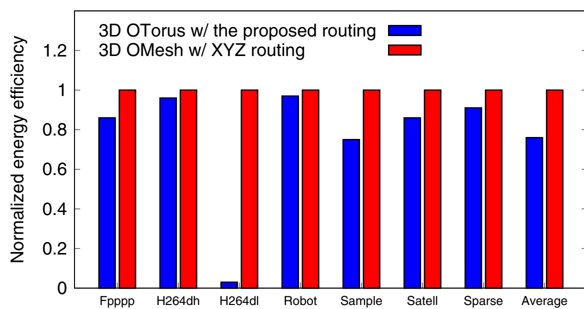

Fig. 9. Normalized energy efficiency for real applications, without thermal tuning, $0.775nm$ 3-dB bandwidth

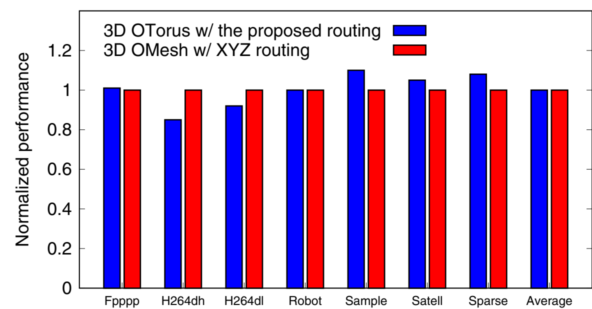

Fig. 12. Normalized performance for real applications, without thermal tuning, $0.62nm$ 3-dB bandwidth

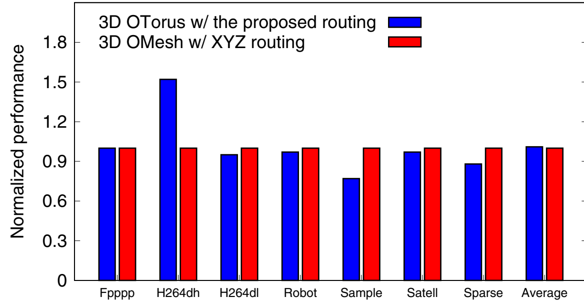

Fig. 13. Normalized performance for real applications, with thermal tuning, $0.62nm$ 3-dB bandwidth

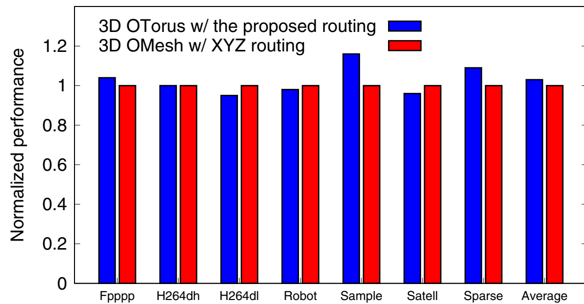

Fig. 14. Normalized performance for real applications, with athermal MRs, $0.62nm$ 3-dB bandwidth

We assume the laser wavelength and resonant wavelength of microresonators are 1550nm at room temperature.

A. *Thermal-induced energy efficiency*

The energy consumption for a packet transmission in the proposed 3D torus-based optical NoC involves the energy consumed for payload transmission in the optical domain and the energy consumed in the electronic domain for control purposes. Since the size of the control packets is small, the energy consumed in the electronic domain only takes

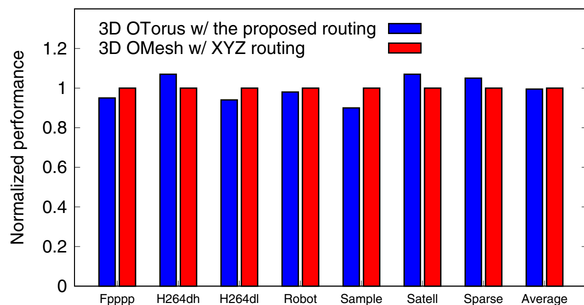

Fig. 15. Normalized performance for real applications, without thermal tuning, $0.775nm$ 3-dB bandwidth

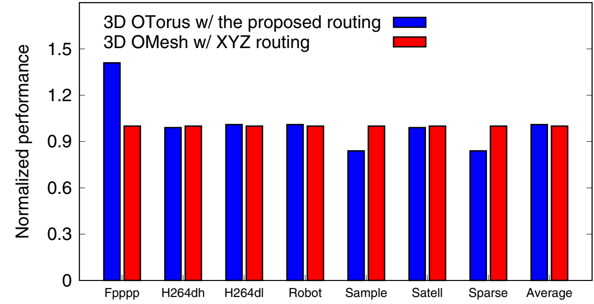

Fig. 16. Normalized performance for real applications, with thermal tuning, $0.775nm$ 3-dB bandwidth

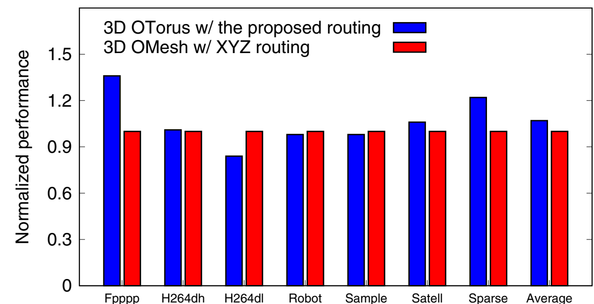

Fig. 17. Normalized performance for real applications, with athermal MRs, $0.775nm$ 3-dB bandwidth

a small proportion of overall communication energy, with the energy consumption in O/E interfaces accounting for the major proportion of the total energy consumption. The energy consumed by a payload transmission includes the energy consumed by the O/E interfaces, and the energy consumed by thermal tuning for microresonators [17]. For the evaluation of O/E conversions power consumption, we use the VCSEL model in [12], the serializer and deserializer designs in [34], and the VCSEL driver and TIA-LA circuit designs in [35]. The photodetector model is based on a Ge waveguide photodetector monolithically integrated in 130nm CMOS process with a sensitivity of $-14.2dBm$ for 10^{-12} of bit error rate (BER) [36].

Figures 6-8 show the normalized energy efficiency of the proposed 3D 8x8x2 torus-based optical NoC under different real application workloads, when the 3-dB bandwidth of BOSEs is 0.62nm. If thermal tuning is not utilized for microresonators (Figure 6), the proposed thermal-sensitive routing would reduce the average energy efficiency by 25%. If thermal tuning is utilized for microresonators (Figure 7), the proposed thermal-sensitive routing would reduce the average energy efficiency by 19%. If athermal microresonators are used (Figure 8), the proposed thermal-sensitive routing would reduce the average energy efficiency by 17%. The thermal-related energy efficiency is sensitive to the 3dB bandwidth

of BOSEs. As shown in Figure 9 to Figure 11, when the 3-dB bandwidth of BOSEs is 0.775nm, the proposed thermal-sensitive routing would reduce the average energy efficiency by 24% if thermal tuning for microresonators is not utilized; by 20% if thermal tuning is utilized; by 10% if athermal microresonators are used.

B. Network performance

Figures 12-14 show the normalized performance of the proposed 3D 8x8x2 torus-based optical NoC under different real application workloads, when the 3-dB bandwidth of BOSEs is 0.62nm. We can observe that the average network performance is almost the same with the traditional XYZ routing, without sacrificing performance. This is due to the fact that the proposed thermal-sensitive routing always chooses a path from shortest paths. As shown in Figures 15-17, when the 3-dB bandwidth of BOSEs is 0.775nm, we can get the same conclusions.

IV. CONCLUSIONS

In this work, we propose a thermal-sensitive design and power optimization approach for a 3D torus-based optical NoC architecture. Based on an optical thermal modeling platform which models the thermal effects in optical NoCs from a system-level perspective, a thermal-sensitive routing algorithm is proposed for the 3D torus-based optical NoC architecture to optimize its power consumption in the presence of on-chip temperature variations. Simulation results show that in an 8x8x2 3D torus-based optical NoC under a set of real application workloads, as compared with a matched 3D mesh-based optical NoC with the traditional dimension order routing, the power consumption is reduced by 25% if thermal tuning for microresonators is not utilized, by 19% if thermal tuning is utilized for microresonators, and by 17% if athermal microresonators are used.

REFERENCES

[1] W. Dally and B. Towles, "Route packets, not wires: on-chip interconnection networks," in *Proc. Design Automation Conf.*, 2001, pp. 684–689.

[2] L. Benini and G. De Micheli, "Networks on chip: a new paradigm for systems on chip design," in *Proc. Design, Automation and Test in Europe Conference and Exhibition*, 2002, pp. 418–419.

[3] S. Bahirat and S. Pasricha, "UC-PHOTON: A novel hybrid photonic network-on-chip for multiple use-case applications," in *11th Int. Symp. Quality Electronic Design*, 2010, pp. 721–729.

[4] K. H. Mo, Y. Ye, X. Wu, W. Zhang, W. Liu, and J. Xu, "A hierarchical hybrid optical-electronic network-on-chip," in *IEEE Computer Society Annual Symp. VLSI*, July 2010, pp. 327–332.

[5] L. Ramini, A. Ghiribaldi, P. Grani, S. Bartolini, H. T. Fankem, and D. Bertozzi, "Assessing the energy break-even point between an optical noc architecture and an aggressive electronic baseline," in *2014 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2014, pp. 1–6.

[6] S. Werner, J. Navaridas, and M. Lujn, "Amon: An advanced mesh-like optical noc," in *2015 IEEE 23rd Annual Symposium on High-Performance Interconnects*, Aug 2015, pp. 52–59.

[7] S. Faralli, N. Andriolli, F. Gambini, P. Pintus, G. Preve, M. Chiesa, R. Ortuno, O. Liboiron-Ladouceur, and I. Cerutti, "Bidirectional transmissions in a ring-based packaged optical noc with 12 add-drop microrings," in *2016 IEEE Photonics Conference (IPC)*, Oct 2016, pp. 621–622.

[8] Y. Ye, L. Duan, J. Xu, J. Ouyang, M. K. Hung, and Y. Xie, "3D optical networks-on-chip (NoC) for multiprocessor systems-on-chip (MPSoC)," in *3D System Integration, IEEE International Conference on*, Sept. 2009, pp. 1–6.

[9] K. Skadron, M. R. Stan, K. Sankaranarayanan, W. Huang, S. Velusamy, and D. Tarjan, "Temperature-aware microarchitecture: Modeling and implementation," *ACM Trans. Archit. Code Optim.*, vol. 1, no. 1, pp. 94–125, 2004.

[10] V. Padgaonkar and A. Arbor, "Thermal effects in silicon based resonant cavity devices," *NNIN REU Research Accomplishments*, 2004.

[11] S. Mogg, N. Chitica, U. Christiansson, R. Schatz, P. Sundgren, C. Asplund, and M. Hammar, "Temperature sensitivity of the threshold current of long-wavelength InGaAs-GaAs VCSELs with large gain-cavity detuning," *IEEE J. Quantum Electronics*, vol. 40, no. 5, pp. 453–462, May. 2004.

[12] A. Syrbu, A. Mereuta, V. Iakovlev, A. Caliman, P. Royo, and E. Kapon, "10 Gbps VCSELs with high single mode output in 1310nm and 1550 nm wavelength bands," in *Conf. Optical Fiber communication/National Fiber Optic Engineers*, 2008, pp. 1–3.

[13] R. K. Dokania and A. B. Apsel, "Analysis of challenges for on-chip optical interconnects," in *Proc. 19th ACM Great Lakes Symp. VLSI*, 2009, pp. 275–280.

[14] Z. Li, M. Mohamed, X. Chen, E. Dudley, K. Meng, L. Shang, A. R. Mickelson, R. Joseph, M. Vachharajani, B. Schwartz, and Y. Sun, "Reliability modeling and management of nanophotonic on-chip networks," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. PP, no. 99, pp. 1–14, 2010.

[15] T. Zhang, J. L. Abelln, A. Joshi, and A. K. Coskun, "Thermal management of manycore systems with silicon-photonic networks," in *2014 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2014, pp. 1–6.

[16] S. V. R. Chittamuru and S. Pasricha, "Spectra: A framework for thermal reliability management in silicon-photonic networks-on-chip," in *2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID)*, Jan 2016, pp. 86–91.

[17] F. Gan, T. Barwicz, M. Popovic, M. Dahlem, C. Holzwarth, P. Rakich, H. Smith, E. Ippen, and F. Kartner, "Maximizing the thermo-optic tuning range of silicon photonic structures," in *Photonics in Switching*, Aug. 2007, pp. 67–68.

[18] M. Geng, L. Jia, L. Zhang, L. Yang, P. Chen, T. Wang, and Y. Liu, "Four-channel reconfigurable optical add-drop multiplexer based on photonic wire waveguide," *Opt. Express*, vol. 17, no. 7, pp. 5502–5516, Mar. 2009.

[19] J.-M. Lee, D.-J. Kim, H. Ahn, S.-H. Park, and G. Kim, "Temperature dependence of silicon nanophotonic ring resonator with a polymeric overlayer," *J. Lightwave Technol.*, vol. 25, no. 8, pp. 2236–2243, Aug 2007.

[20] V. Raghunathan, J. Hu, W. N. Ye, J. Michel, and L. C. Kimerling, "Athermal silicon ring resonators," in *Integrated Photonics Research, Silicon and Nanophotonics*, 2010, p. IMC5.

[21] Y. Ye, J. Xu, X. Wu, W. Zhang, X. Wang, M. Nikdast, Z. Wang, and W. Liu, "System-level modeling and analysis of thermal effects in optical networks-on-chip," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. PP, no. 99, pp. 1–14, 2012.

[22] Y. Ye, Z. Wang, P. Yang, J. Xu, X. Wu, X. Wang, M. Nikdast, Z. Wang, and L. H. K. Duong, "System-level modeling and analysis of thermal effects in wdm-based optical networks-on-chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 11, pp. 1718–1731, Nov 2014.

[23] H. Li, A. Fourmigue, S. L. Beux, X. Letartre, I. O'Connor, and G. Nicolescu, "Thermal aware design method for vcsel-based on-chip optical interconnect," in *2015 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2015, pp. 1120–1125.

[24] D. Dang, S. V. R. Chittamuru, R. Mahapatra, and S. Pasricha, "Islands of heaters: A novel thermal management framework for photonic nocs," in *2017 22nd Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan 2017, pp. 306–311.

[25] S. V. R. Chittamuru, S. Desai, and S. Pasricha, "Reconfigurable silicon-photonic network with improved channel sharing for multicore architectures," in *Proceedings of the 25th edition on Great Lakes Symposium on VLSI*. ACM, 2015, pp. 63–68.

[26] S. Bahirat and S. Pasricha, "Meteor: Hybrid photonic ring-mesh network-on-chip for multicore architectures," *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 13, no. 3s, p. 116, 2014.

[27] B. Feero and P. Pande, "Networks-on-chip in a three-dimensional environment: A performance evaluation," *Computers, IEEE Transactions on*, vol. 58, no. 1, pp. 32–45, Jan. 2009.

[28] H. Gu and J. Xu, "Design of 3D optical network on chip," in *Photonics and Optoelectronics, Symposium on*, Aug. 2009, pp. 1–4.

[29] Y. Ye, J. Xu, B. Huang, X. Wu, W. Zhang, X. Wang, M. Nikdast, Z. Wang, W. Liu, and Z. Wang, "3-d mesh-based optical network-on-chip for multiprocessor system-on-chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 4, pp. 584–596, April 2013.

[30] F. G. Della Corte, M. Esposito Montefusco, L. Moretti, I. Rendina, and G. Cocorullo, "Temperature dependence analysis of the thermo-optic effect in silicon by single and double oscillator models," *J. Applied Physics*, vol. 88, no. 12, pp. 7115–7119, Dec. 2000.

[31] S. Xiao, M. H. Khan, H. Shen, and M. Qi, "Compact silicon microring resonators with ultra-low propagation loss in the C band," *Opt. Express*, vol. 15, no. 22, pp. 14 467–14 475, 2007.

[32] S. Li, J. H. Ahn, R. D. Strong, J. B. Brockman, D. M. Tullsen, and N. P. Jouppi, "Mcpat: An integrated power, area, and timing modeling framework for multicore and manycore architectures," in *2009 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, Dec 2009, pp. 469–480.

[33] W. Huang, S. Ghosh, S. Velusamy, K. Sankaranarayanan, K. Skadron, and M. R. Stan, "Hotspot: a compact thermal modeling methodology for early-stage vlsi design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 5, pp. 501–513, May 2006.

[34] J. Poulton, R. Palmer, A. Fuller, T. Greer, J. Eyles, W. Dally, and M. Horowitz, "A 14-mW 6.25-Gb/s transceiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2745–2757, Dec. 2007.

[35] C. Kromer, G. Sialm, C. Berger, T. Morf, M. Schmatz, F. Ellinger, D. Erni, G.-L. Bona, and H. Jackel, "A 100-mW 4 x 10 Gb/s transceiver in 80-nm CMOS for high-density optical interconnects," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2667–2679, Dec. 2005.

[36] G. Masini, G. Capellini, J. Witzens, and C. Gunn, "A 1550nm, 10Gbps monolithic optical receiver in 130nm CMOS with integrated Ge waveguide photodetector," in *4th IEEE Int. Conf. Group IV Photonics*, 2007, pp. 1–3.