Sudeep Pasricha

Assistant Professor
Department of Electrical & Computer Engineering
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Research Interests

Embedded systems, advanced on-chip interconnects (optical, carbon nanotube, 3D), networks-on-chip, power-aware design, system-level modeling languages and design methodologies, computer architecture, VLSI CAD.

Education

2005-2008	Ph.D. in Computer Science	University of California, Irvine
2002-2005	M.S. in Computer Science	University of California, Irvine
1996-2000	B.E. in Electronics and Communications Engineering	Delhi Institute of Technology, India

Employment

2008-	Assistant Professor	Colorado State University, Fort Collins, CO, USA
2005-2008	Research Assistant	Center for Embedded Computer Systems, UC Irvine, USA
2003–2005	Design Engineer Intern	Conexant Systems Inc, Newport Beach, CA, USA
2003	Teaching Assistant	University of California, Irvine, USA
2002–2003	Research Assistant	University of California, Irvine, USA
2000–2002	Associate Design Engineer	STMicroelectronics, Noida, India and Crolles, France
2000	Student Researcher	Delhi Institute of Technology, Delhi, India
1999–2000	Software Engineer Intern,	HCL Technologies, Gurgaon, India
1999	Software Engineer Intern	CMC Ltd, New Delhi, India

Honors and Awards

- Bob and Barbara Kleist PhD Dissertation Award (UCI), 2007-2008
- Joseph Fischer Memorial Award for Outstanding Achievement in Computer Science (UCI), 2006-2007
- Center for Pervasive Communications and Computing (CPCC) Fellowship Award, 2004-2007
- Best Paper Award, Asia and South Pacific Design Automation Conference (ASPDAC) , 2006
- Best Paper Award Nomination, Design Automation Conference (DAC), 2005
- DAC Student Mentor Award, Design Automation Conference (DAC), 2005
- (2^{nd} place) Best Poster Award, Southern California Embedded Systems Symposium (SCESS), 2003
- DAC Young Student Award, Design Automation Conference (DAC), 2003
- Regents Fellowship, Department of Information and Computer Science, (UCI), 2002-2003
- Best Student in Electronics and Communications Award, Delhi Institute of Technology, India, 1996-1997
- National Mathematics Olympiad, Outstanding Performance Merit Award, Govt of India, 1994-1996
- Ramanujan Society of Born Mathematicians Award, All India 7^{th} Rank, 1994

Selected Publications

Books:

B1 – S. Pasricha and N. Dutt, “On-Chip Communication Architectures”, *Morgan Kauffman, ISBN 978-0-12-373892-9, Apr 2008*

Journals:

J13 – S. Pasricha, F. Kurdahi, N. Dutt, "Evaluating Carbon Nanotube Global Interconnects for Chip Multiprocessor Applications", To appear in IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2009

J12 – S. Pasricha, Y. Park, F. Kurdahi, N. Dutt, "CAPPS: A Framework for Power-Performance Trade-Offs in Bus Matrix Based On-Chip Communication Architecture Synthesis", To appear in IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2009

J11 – G. Madl, S. Pasricha, N. Dutt, S. Abdelwahed, "Cross-abstraction Functional Verification and Performance Analysis of Chip Multiprocessor Designs", *IEEE Transactions on Industrial Informatics (TII), pp. 5(3):241-256, Aug 2009*

J10 – D. Cho, S. Pasricha, I. Issenin, N. Dutt, Y. Paek , "Adaptive Scratch Pad Memory Management for Dynamic Behavior of Multimedia Applications", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (TCAD), Vol. 28, No. 4, pp. 554-567, Apr 2009*

J9 – S. Pasricha, Y. Park, F. Kurdahi, N. Dutt, "System-level PVT Variation Aware Power Exploration of On-Chip Communication Architectures", *ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 14, No. 2, pp. 20:1-20:25, Mar 2009*

J8 – S. Pasricha, N. Dutt, "Trends in Emerging On-Chip Interconnect Technologies", *IPSJ Transactions on System LSI Design Methodology, Vol. 1, Sep 2008*

J7 – S. Pasricha, N. Dutt and M. Ben-Romdhane, "Fast Exploration of Bus-based Communication Architectures at the CCATB Abstraction", *IEEE Transactions on Embedded Computing Systems (TECS), Feb 2007*

J6 – S. Pasricha, N. Dutt and M. Ben-Romdhane, "BMSYN: Bus Matrix Communication Architecture Synthesis for MPSoC", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (TCAD), vol.26, no.8, pp.1454-1464, Aug 2007*

J5 – S. Pasricha and N. Dutt, "A Framework for Co-synthesis of Memory and Communication Architectures for MPSoC", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 26, No. 3, pp. 408-420, Mar 2007*

J4 – C. Shin, P. Grun, N. Romdhane, C. Lennard, G. Madl, S. Pasricha, N. Dutt and M. Noll, "Enabling Heterogeneous Cycle-Based and Event-Driven Simulation in a SPIRIT-Enabled Design Flow", *Kluwer Journal on Design Automation of Embedded Systems (DAES), Feb 2007*

J3 – S. Pasricha, N. Dutt, E. Bozorgzadeh and M. Ben-Romdhane, "FABSYN: Floorplan-aware Bus Architecture Synthesis”, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI) Vol 14, No. 3, pp 241-253, Mar 2006*

J2 – S. Pasricha, M. Luthra, S. Mohapatra, N. Dutt, N. Subramanian, "Dynamic Backlight Adaptation for Low Power Handheld Devices", *IEEE Design and Test (IEEE D&T), Special Issue on Embedded Systems for Real Time Embedded Systems, Sep-Oct 2004*

J1 – S. Pasricha, S. Mohapatra, M. Luthra, N. Dutt and N. Subramanian, "Co-optimization of Streaming Multimedia QoS and Backlight Power Consumption for Mobile Handheld Devices", *Journal of Korean Multimedia Society (KSSM), Dec 2003*

Conferences:

C28 – S. Bahirat, S. Pasricha, "Exploring Hybrid Photonic Networks-on-Chip for Emerging Chip Multiprocessors", *To appear, IEEE/ACM CODES+ISSS Oct 2009*

C27 –S. Pasricha, "Exploring Serial Vertical Interconnects for 3D ICs", *IEEE/ACM DAC, Jul 2009*

C26 – R. Kost, D. Connors, S. Pasricha, "Characterizing the Use of Program Vulnerability Factors for Studying Transient Fault Tolerance in Multi-core Architectures", *Workshop on Compiler and Architectural Techniques for Application Reliability and Security (CATARS) Jun, 2009*

C25 – A. Gupta, S. Pasricha, N. Dutt, F. Kurdahi, K. Khouri, M. Abadir, "On-Chip Communication Architecture Based Thermal Management for SoCs", *IEEE VLSI-DAT, Apr 2009*

C24 – S. Pasricha, N. Dutt, F. Kurdahi, "Dynamically Reconfigurable On-Chip Communication Architectures for Multi Use-Case Chip Multiprocessor Applications", *IEEE Asia & South Pacific Design Automation Conference (ASPDAC), Jan 2009*

C23 – S. Pasricha, F. Kurdahi, N. Dutt, "Exploring Carbon Nanotube Bundle Global Interconnects for Chip Multiprocessor Applications", *IEEE VLSI Design Conference (VLSID), January 2009*

C22 – L. A. D. Bathen, S. Pasricha, N. Dutt, "A Framework for Memory-aware Multimedia Application Mapping on Chip-Multiprocessors", *IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia) Oct 2008*

C21 – Y. Park, S. Pasricha, F. Kurdahi, N. Dutt, "Methodology for Multi-Granularity Embedded Processor Power Model Generation for an ESL Design Flow", *IEEE/ACM CODES+ISSS Oct 2008*

C20 – S. Pasricha, F. Kurdahi, N. Dutt, "System Level Performance Analysis of Carbon Nanotube Global Interconnects for Emerging Chip Multiprocessors", *IEEE/ACM NanoArch Jun 2008*

C19 – H. Homayoun, S. Pasricha, M. Makhzan, A. Veidenbaum, "Dynamic Register File Resizing to Improve Embedded Processor Performance and Energy-delay Efficiency", *IEEE/ACM DAC Jun 2008*

C18 – D. Cho, S. Pasricha, I. Issenin, N. Dutt and Y. Paek, "Compiler Driven Data Layout Optimization for Regular/Irregular Array Access Patterns", *ACM LCTES Jun 2008*

C17 – H. Homayoun, S. Pasricha, M. Makhzan, A. Veidenbaum, "Improving Performance and Reducing Energy-Delay with Adaptive Resource Resizing for Out-of-Order Embedded Processors", *ACM LCTES Jun 2008*

C16 – S. Pasricha, Y. Park, F. Kurdahi, N. Dutt, "Incorporating PVT Variations in System-level Power Exploration of On-Chip Communication Architectures", *IEEE VLSI Design Conference (VLSID 2008), Bangalore, India, January 2008*

C15 – S. Pasricha, N. Dutt, "ORB: An On-chip Optical Ring Bus Communication Architecture for Multi-Processor Systems-on-Chip", *IEEE Asia & South Pacific Design Automation Conference (ASPDAC 2008)*, *Seoul, Korea, January 2008*

C14 – Y. Park, S. Pasricha, F. Kurdahi, N. Dutt, "System Level Power Estimation Methodology with H.264 Decoder Prediction IP Case Study", *IEEE International Conference on Computer Design (ICCD 2007), Great Lakes, CA, Oct 2007*

C13 – S. Pasricha, N. Dutt, "On-chip Communication Architecture Synthesis for High Performance MPSoCs", *SRC TechConnect, Nov 2007*

C12 – S. Pasricha, Y. Park, F. Kurdahi, N. Dutt, "System-Level Power-Performance Trade-Offs in Bus Matrix Communication Architecture Synthesis", *IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis* (*CODES+ISSS 2006)*, *Seoul, Korea, October 2006*

C11 – G. Madl, S. Pasricha, Q. Zhu, L. Bathen and N. Dutt, "Formal Performance Evaluation of AMBA-based System-on-Chip Designs", *6th Annual ACM Conference on Embedded Software (EMSOFT 2006)*, *Seoul, Korea, October 2006*

C10 – S. Pasricha and N. Dutt, "COSMECA: Application Specific Co-Synthesis of Memory and Communication Architectures for MPSoC", *IEEE Design Automation and Test in Europe Conference (DATE 2006)*, *Munich, Germany, March 2006*

*** C9 –** S. Pasricha, N. Dutt and M. Ben-Romdhane, "Constraint-Driven Bus Matrix Synthesis for MPSoC", *IEEE Asia & South Pacific Design Automation Conference (ASPDAC 2006)*, *Yokohama, Japan, January 2006* **(Best Paper Award)**

C8 – S. Pasricha, N. Dutt and M. Ben-Romdhane, "Using TLM for Exploring Bus-based SoC Communication Architectures", *IEEE Conference on Application-specific Systems, Architectures and Processors (ASAP 2005), Samos, Greece, July 2005*

*** C7 –** S. Pasricha, N. Dutt, E. Bozorgzadeh and M. Ben-Romdhane, "Floorplan-aware Automated Synthesis of Bus-based Communication Architectures", *IEEE Design Automation Conference (DAC 2005), Anaheim, CA, June 2005* ***(Best Paper Award Candidate)***

C6 – S. Pasricha, N. Dutt and M. Ben-Romdhane, "Automated Throughput-driven Synthesis of Bus-based Communication Architectures", *IEEE Asia South Pacific Design Automation Conference (ASPDAC 2005)*, *Shanghai, China, January 2005*

C5 – S. Pasricha, N. Dutt, M. Ben-Romdhane, "Fast Exploration of Bus-based On-chip Communication Architectures", *IEEE International Conference on Hardware-Software Codesign and System Synthesis* (*CODES+ISSS 2004)*, *Stockholm, Sweden, September 2004*

C4 – S. Pasricha, N. Dutt and M. Ben-Romdhane, "Extending the Transaction Level Modeling Approach for Fast Communication Architecture Exploration", *IEEE Design Automation Conference (DAC 2004), San Diego, CA, June 2004*

C3 – S. Pasricha, S. Mohapatra, M. Luthra, N. Dutt and N. Subramanian, "Reducing Backlight Power Consumption for Streaming Video Applications on Mobile Handheld Devices", *IEEE Embedded Systems for Real-Time Multimedia (ESTIMEDIA 2003)*, *Newport Beach, CA, October 2003*

C2 – S. Pasricha and A. Veidenbaum, "Improving Branch Prediction Accuracy in Embedded Processors in the Presence of Context Switches" *IEEE International Conference on Computer Design (ICCD 2003), San Jose, CA, October 2003*

C1 – S. Pasricha, "Transaction Level Modeling of SoC using SystemC 2.0" *Synopsys User Group Conference (SNUG 2002), Bangalore*, *May 2002*

Tutorials at Major Conferences

T4 – S. Pasricha, N. Dutt, L. Benini, “On-Chip Communication Architectures: Buses, Networks-on-Chip, and Beyond ”, *Full day tutorial at 41st IEEE/ACM International Symposium on Microarchitecture (MICRO 2008), Lake Como, Italy, Nov 2008*

T3 – S. Pasricha, K. Lahiri, and N. Dutt, “Modeling, Analysis and Design of Bus-based SOC Communication Architectures”, *Half day tutorial presented at IEEE Design Automation and Test in Europe Conference, (DATE 2007), Nice, France, April 2007*

T2 – S. Pasricha, K. Banerjee, L. Benini, K. Lahiri and N. Dutt, "SoC Communication Architectures: Technology, Current Practice, Research and Trends", *Full day tutorial presented at IEEE VLSI Design Conference (VLSID 2007), Bangalore, India, January 2007*

T1 – S. Pasricha and N. Dutt, "SoC Communication Architectures: Current Practice, Research and Trends", *Half day tutorial presented at IEEE Asia and South Pacific Design Automation Conference (ASPDAC 2006), Yokohama, Japan, January 2006.*

Published Software

S1 – EXPRESSION: Architecture Description Language (ADL) based Retargetable Compiler-Simulator tool-suite *(available at http://www.ics.uci.edu/~aces)*

PhD Forum

S. Pasricha, "COMMSYN: On-Chip Communication Architecture Synthesis for Multi-Processor System-on-Chips", *IEEE Design Automation and Test in Europe, (DATE 2007), Nice, France, April 2007*

Professional Service

Technical Program Committee (TPC) Member

- ACM/IEEE International Symposium on Networks-on-Chip (NOCS), 2010
- IEEE International Conference on VLSI Design (VLSID) 2010
- IEEE International Conference on HW/SW Codesign and System Synthesis (CODES+ISSS) 2009
- IEEE/ACM SIGDA Design Automation Conference PhD Forum (DAC PhD Forum) 2009
- IEEE International Conference on VLSI Design (VLSID) 2009 **(Track Chair)**
- IEEE International Symposium on Quality Electronic Design (ISQED) 2009
- IEEE International Symposium on Quality Electronic Design (ISQED) 2008

Organizing Committee

- IEEE/ACM ICCAD CADathlon, 2009 **(Vice Chair)**

Technical Session Chair

- IEEE International Conference on VLSI Design (VLSID) 2009
- IEEE International Conference on HW/SW Codesign and System Synthesis (CODES+ISSS) 2008
- IEEE International Conference on Computer Design (ICCD) 2007

Reviewer

Books

- Springer Lecture Notes in Computer Science
- Elsevier Systems on Silicon Series

Journals

- ACM Transactions on Design Automation of Electronic Systems (TODAES), 2005-
- ACM Transactions on Embedded Computing Systems (TECS), 2004-
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2005-
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2005-
- IEEE Transactions on Computers (Computers), 2006-
- IEEE Design and Test of Computers (D&T), 2007-
- Kluwer Design Automation for Embedded Systems (DAES), 2007-

Conferences

- IEEE/ACM Design Automation Conference (DAC), 2003-
- IEEE International Conference on Computer-Aided Design (ICCAD), 2003-
- IEEE/ACM Design Automation and Test in Europe (DATE), 2004-

- IEEE/ACM/ Intl. Conf. on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2004-
- IEEE/ACM Asia South Pacific Design Automation Conference (ASPDAC), 2003-
- IEEE International Conference on VLSI Design (VLSID), 2000
- International Conf. on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), 2004-
- International SoC Design Conference (ISOCC), 2006-
- IEEE International Conference on Computer Design (ICCD), 2006-
- IEEE International Symposium on Quality Electronic Design (ISQED) 2007-

Memberships

- CSU Information Science and Technology Center (ISTeC) Education Advisory Committee, 2008-
- Association for Computing Machinery (ACM), 2006-
- ACM Special Interest Group on Design Automation (SIGDA), 2006-
- Member, Institute of Electrical and Electronics Engineers (IEEE), 2002-

Teaching Experience

Assistant Professor, Colorado State University

Fall 2009	Hardware/Software Design of Embedded Systems (graduate course)
Spring 2009	Hardware/Software Design of Embedded Systems (graduate course)
Fall 2008	Digital System Design (senior undergraduate course)

Graduate Student Instructor, University of California Irvine

Spring 2008	On-Chip Communication Architectures (graduate seminar course)

Teaching Assistant, University of California Irvine

Spring 2003	High Performance Compilers and Program Optimization (undergraduate course)
Winter 2003	Introduction to Computer Science: Programming in Java (undergraduate course)