CV: Mahdi Nikdast

Last updated: July 3, 2018

Contents

1 Personal Information **2**
1.1 Contact Information . . . 2
1.2 Education . . . 2
1.3 Awards and Honors . . . 2
1.4 Professional Appointments . . . 3
1.5 Professional Society Membership . . . 3

2 Research Activities **4**
2.1 Research Interest Statement . . . 4
2.2 Publication Citations . . . 4
2.3 Research Grants and Contracts . . . 4
2.4 Equipment Grants . . . 5
2.5 Research and Development Tools . . . 5
2.6 Books . . . 5
2.7 Book Chapters . . . 5
2.8 Journal Articles . . . 5
2.9 Conference Proceedings and Presentations . . . 7
2.10 Other Publications . . . 9
2.11 Refereed Conference Poster Presentations . . . 9
2.12 Thesis . . . 10
2.13 Invited Talks . . . 10

3 Educational Activities **12**
3.1 Ph.D. Thesis Committee Member . . . 12
3.2 Teaching Experience at CSU . . . 12
3.3 Courses Developed at CSU . . . 12
3.4 Professional Development (Participated) . . . 12

4 Professional Activities **13**
4.1 Editorial Activities . . . 13
4.2 Conference Steering Committee . . . 13
4.3 Conference Organizing Committee (General Chair) . . . 13
4.4 Conference Organizing Committee (Technical Program Committee Chair) . . . 13
4.5 Conference Organizing Committee (Other Chaired Positions) . . . 13
4.6 Special Session Organizing Committee . . . 13
4.7 Technical Program Committee (TPC) Member . . . 14
4.8 Conference Technical Session Chair . . . 14
4.9 Referee/Reviewer Activities . . . 14
4.10 University, College, and Department Service . . . 15

1 Personal Information

1.1 Contact Information

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Web: http://www.engr.colostate.edu/∼mnikdast

1.2 Education

Degree	*Date*	*University*
Ph.D.	Dec. 2013	Hong Kong University of Science and Technology (HKUST)
B.Sc.(Hons)	May 2005	Azad University, Iran

Doctoral Dissertation:
Signal-to-noise Ratio (SNR) in Optical Interconnection Networks: Analysis, Modeling, and Comparison

1.3 Awards and Honors

[1] ACM Great Lakes Symposium on VLSI (GLSVLSI) **Best Paper Award Candidate** for the paper "DeEPeR: Enhancing Performance and Reliability in Chip-Scale Optical Interconnection Networks", Chicago, IL 2018

[2] IEEE Design Automation and Test in Europe (DATE) Conference and Exhibition **Best Paper Award** for the paper "Modeling Fabrication Non-Uniformity in Chip-Scale Silicon Photonic Interconnects" in Test and Robustness Track, Germany, 2016

[3] IEEE/ACM Design Automation Conference (DAC) Travel Grant, USA, 2016

[4] Natural Sciences and Engineering Research Council of Canada (NSERC) CREATE Postdoctoral Fellowship (SiEPIC Program), Canada, 2015-2017

[5] IEEE/OSA Asia Communications and Photonics (ACP) Conference **Best Poster Paper Award** for the paper "Photonic Integrated Circuits under Process Variations" - The Optical Society, Hong Kong, 2015

[6] IEEE Design Automation and Test in Europe (DATE) Conference and Exhibition - Ph.D. Forum Travel Grant, France, 2015

[7] Regroupement Strategique en MicroSystemes du Quebec (ReSMiQ) Postdoctoral Fellowship, Canada, 2014-2016

[8] IEEE/ACM Design Automation Conference (DAC) - Ph.D. Forum Travel Grant, USA, 2014

[9] HKUST School of Engineering Fellowship for Outstanding Graduate Students, Hong Kong, 2012-2013

[10] HKUST Postgraduate Scholarship, Hong Kong, 2009-2013

[11] AMD Technical Forum and Exhibition (AMD-TFE) **Best Project Award (2nd place)** for the project "A Formal Analysis of Crosstalk Noise in Mesh-Based Optical Networks-on-Chip for Chip Multiprocessors", Taiwan, 2010

[12] AMD Travel Grant, 2010

[13] Azad Univresity Scholarship for Outstanding Undergraduate Students, Iran, 2006-2009

1.4 Professional Appointments

Sep. 2017–present
Assistant Professor, Department of Electrical and Computer Engineering, Colorado State University, USA

Sep. 2014–Aug. 2017
Postdoctoral Fellow, Computer and Software Engineering Department, Polytechnique Montreal (In collaboration with McGill University), Canada

Feb. 2014–Aug. 2014
Visiting Scholar, Electronic and Computer Engineering Department, HKUST, Hong Kong

Sep. 2009–Jan. 2014
Graduate Research Assistant, Electronic and Computer Engineering Department, HKUST, Hong Kong

1.5 Professional Society Membership

2014–present
IEEE Member

2015–present
ACM Member

2010–2014
IEEE Graduate Student Member

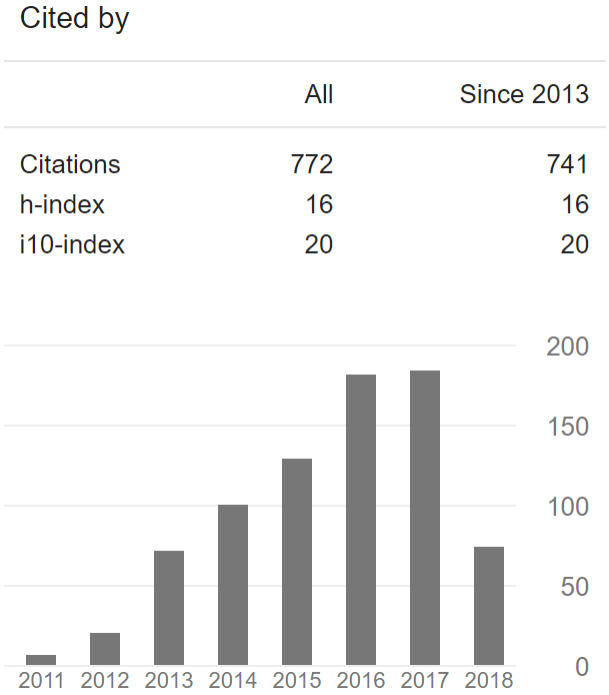
2 Research Activities

2.1 Research Interest Statement

My primary research goals are focused on design methodologies and development of high performance computing and communication systems employing emerging technologies while emphasizing on energy-efficiency and robustness. Some topics of interest are: High Performance Computing, Silicon Photonics, Heterogeneous Embedded and Computing Systems, Interconnection Networks, Systems Modeling and Simulation, Design for Reliability and Energy Efficiency, Advanced Computer Architectures, and Computer Vision.

2.2 Publication Citations

(Google Scholar as of 1 July, 2018)



2.3 Research Grants and Contracts

[RG1] Co-Principal Investigator: "Energy-Efficient and Reliable Communication with Silicon Photonics for Terascale Datacenters-on-Chip," CCF:SHF:Small, National Science Foundation (NSF), Oct. 2018 to Sep. 2021, $450,000.

[RG2] Principal Investigator: "High Performance Computing Systems Integrating Silicon Photonics," Colorado State University Faculty Startup, Sep. 2017 to Sep. 2020, $300,000.

[RG3] Principal Investigator: "Workshop on Silicon Photonics for High Performance Computing," Sponsorship from Mentor Graphics (Siemens Business) and CSU WSJ College of Engineering, April 2018 to May 2018, $7,500.

2.4 Equipment Grants

[EG1] Principal Investigator: "Automated Testing Probe Station," Colorado State University (ESTC), April 2018, $10,000.

2.5 Research and Development Tools

[RD1] CLAP: Crosstalk and Loss Analysis Platform for Optical Interconnects. *Developed at the Hong Kong University of Science and Technology*. 2009-2014.

[RD2] OTEMP: Optical Thermal Effect Modeling Platform for Optical Interconnects (Contributed). *Developed at the Hong Kong University of Science and Technology*. 2009-2014.

[RD3] MCSL – Realistic Networks-on-Chip Traffic Patterns (Contributed). *Developed at the Hong Kong University of Science and Technology*. 2009-2014.

2.6 Books

[B1] **M. Nikdast**, G. Nicolescu, S. Le Beux, and J. Xu (Editors), *Photonic Interconnects for Computing Systems: Understanding and Pushing Design Challenges*. River Publishers, May 2017, ISBN 9788793519800, 412 pp.

2.7 Book Chapters

[BC1] **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Impact of Fabrication Non-uniformity on Silicon Photonics Networks-on-Chip", *Photonic Interconnects for Computing Systems: Understanding and Pushing Design Challenges*. River Publishers, May 2017, ISBN 9788793519800, Chapter 12, pp. 355-385.

[BC2] F. Gohring, **M. Nikdast**, F. Hessel, O. Liboiron-Ladouceur, and G. Nicolescu, "Optical Interconnection Networks: The Need for Low-Latency Controllers", *Photonic Interconnects for Computing Systems: Understanding and Pushing Design Challenges*. River Publishers, May 2017, ISBN 9788793519800, Chapter 3, pp. 73-107.

2.8 Journal Articles

(Total: 22)

[J1] M. Bahadori, **M. Nikdast**, S. Rumley, L. Y. Dai, N. Janosik, T. V. Vaerenbergh, A. Gazman, Q. Cheng, R. Polster, and K. Bergman, "Design Space Exploration of Microring Resonators in Silicon Photonic Interconnects: Impact of the Ring Curvature," *IEEE Journal of Lightwave Technology*, vol. 36, no. 23, pp. 2767-2782, July 2018.

[J2] R. Ayari, **M. Nikdast**, I. Hafnaoui, G. Beltrame, and G. Nicolescu, "HypAp: a Hypervolume-Based Approach for Refining the Design of Embedded Systems," *IEEE Embedded Systems Letters*, vol. 9, no. 3, pp. 57-60, September 2017.

[J3] **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Chip-Scale Silicon Photonic Interconnects: a Formal Study on Fabrication Non-Uniformity," *IEEE Journal of Lightwave Technology*, vol. 32, no. 16, pp. 3682-3695, August 2016.

[J4] L. H. K. Duong, Z. Wang, **M. Nikdast**, J. Xu, P. Yang, Zh. Wang, R. Maeda, H. Li, X. Wang, S. Le Beux, and Y. Thonnart, "Coherent and Incoherent Crosstalk Noise Analyses in Inter/Intra-chip Optical Interconnection Networks," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 24, no. 7, pp. 2475-2487, July 2016.

[J5] F. Gohring, R. Priti, **M. Nikdast**, F. Hessel, O. Liboiron-Ladouceur, and G. Nicolescu, "Design and Modelling of a Low-Latency Centralized Controller for Optical Integrated Networks," *IEEE Communications Letters*, vol. 20, no. 3, pp. 462-465, March 2016.

[J6] **M. Nikdast**, J. Xu, X. Wu, X. Wang, Z. Wang, Zh. Wang, and P. Yang, "Crosstalk Noise in WDM-based Optical Networks-on-Chip: a Formal Study and Comparison," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 23, no. 11, pp. 2552-2565, November 2015.

[J7] X. Wu, J. Xu, Y. Ye, X. Wang, **M. Nikdast**, Z. Wang, and Zh. Wang, "An Inter/Intra-chip Optical Network for Manycore Processors," *IEEE Transactions on Very Large Scale Integration Systems*, vol.23, no. 4, pp. 678-691, April 2015.

[J8] X. Wang, J. Xu, W. Zhang, X. Wu, Y. Ye, Z. Wang, **M. Nikdast**, and Zh. Wang, "Actively Alleviate Power-Gating-Induced Power/Ground Noise Using Parasitic Capacitance of On-Chip Memories in MPSoCs," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 23, no. 2, pp. 266-279, February 2015.

[J9] **M. Nikdast**, J. Xu, L. H. K. Duong, X. Wu, Z. Wang, X. Wang, and Zh. Wang, "Fat-Tree-Based Optical Interconnection Networks Under Crosstalk Noise Constraint," *IEEE Transactions on Very Large Scale Integration Systems*, vol.23, no.1, pp. 156-169, January 2015.

[J10] Y. Ye, Z. Wang, J. Xu, X. Wu, X. Wang, **M. Nikdast**, Zh. Wang, and L. H. K. Duong, "System-Level Modeling and Analysis of Thermal Effects in WDM-Based Optical Networks-on-Chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol.33, no. 11, pp. 1718-1731, November 2014.

[J11] L. H. K. Duong, **M. Nikdast**, S. Le Beux, J. Xu, X. Wu, Z. Wang, P. Yang, "A Case Study of Signal-to-Noise Ratio in Ring-Based Optical Networks-on-Chip," *IEEE Design and Test of Computers*, vol.31, no. 5, pp. 55-65, October 2014.

[J12] X. Wu, J. Xu, Y. Ye, Z. Wang, **M. Nikdast**, and X. Wang, "SUOR: Sectioned Undirectional Optical Ring for Chip Multiprocessor," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 10, no. 4, pp. 1-25, June 2014.

[J13] Z. Wang, J. Xu, X. Wu, Y. Ye, W. Zhang, **M. Nikdast**, X. Wang, and Zh. Wang, "Floorplan Optimization of Fat-Tree Based Networks-on-Chip for Chip Multiprocessors," *IEEE Transactions on Computers*, vol. 63, no. 6, pp. 1446-1459, June 2014.

[J14] X. Wu, Y. Ye, J. Xu, W. Zhang, W. Liu, **M. Nikdast**, and X. Wang, "UNION: a Unified Inter/Intra-Chip Optical Network for Chip Multiprocessors," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 22, no. 5, pp. 1082-1095, May 2014.

[J15] **M. Nikdast**, J. Xu, X. Wu, W. Zhang, Y. Ye, X. Wang, Z. Wang, and Zh. Wang, "Systematic Analysis of Crosstalk Noise in Folded-Torus-Based Optical Networks-on-Chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 3, pp. 437-450, March 2014.

[J16] W. Liu, X. Wang, J. Xu, W. Zhang, Y. Ye, X. Wu, **M. Nikdast**, and Z. Wang, "On-Chip Sensor Networks for Soft-Error Tolerant Real-Time Multiprocessor Systems-on-Chip," *ACM Journal of Emerging Technologies in Computing Systems*, vol. 10, no. 2, pp. 1-20, March 2014.

[J17] Y. Xie, **M. Nikdast**, J. Xu, X. Wu, W. Zhang, Y. Ye, X. Wang, Z. Wang, and W. Liu, "A Formal Worst-Case Analysis of Crosstalk Noise in Mesh-Based Optical Networks-on-Chip," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 21, no. 10, pp. 1823-1836, October 2013.

[J18] Y. Ye, J. Xu, B. Huang, X. Wu, W. Zhang, X. Wang, **M. Nikdast**, Z. Wang, W. Liu, and Zh. Wang, "3D Mesh-based Optical Network-on-Chip for Multiprocessor System-on-Chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 4, pp. 584-596, April 2013.

[J19] Y. Ye, J. Xu, X. Wu, W. Zhang, X. Wang, **M. Nikdast**, Z. Wang, and W. Liu, "System-Level Modeling and Analysis of Thermal Effects in Optical Networks-on-Chip," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 21, no. 2, pp. 292-305, February 2013.

[J20] Y. Ye, J. Xu, X. Wu, W. Zhang, W. Liu, and **M. Nikdast**, "A Torus-based Hierarchical Optical-Electronic Network-on-Chip for Multiprocessor System-on-Chip," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 8, no. 1, pp. 1-26, February 2012.

[J21] S. Nasrolahi, **M. Nikdast**, and M. Mahdavi, "The Semantic Web: A New Approach for Future World Wide Web," *International Journal of Computer, Electrical, Automation, Control and Information Engineering*, vol. 3, no. 10, pp. 2474-2479, October 2009.

[J22] A. M. Shafiee, M. Montazeri, and **M. Nikdast**, "An Innovational Intermittent Routing Algorithm in Network-on-Chip," *International Journal of Computer and Information Engineering*, vol. 2, no. 9, pp. 2907-2909, September 2008.

2.9 Conference Proceedings and Presentations

(Total: 26)

[C1] **M. Nikdast**, G. Nicolescu, and O. Liboiron-Ladouceur, "Improving Microresonator Reliability in Silicon Photonic Integrated Circuits," *IEEE Optical Interconnect (OI) Conference*, Santa Fe, NM, 2018, pp. 3-4.

[C2] **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "DeEPeR: Enhancing Performance and Reliability in Optical Interconnection Networks," *ACM Great Lakes Symposium on VLSI (GLSVLSI) Conference*, Chicago, IL, 2018, pp. 63-68. **(Best Paper Award Candidate)**

[C3] F. Gohring, **M. Nikdast**, Y. Xiong, F. Hessel, O. Liboiron-Ladouceur, and G. Nicolescu, "Silicon Photonic Interconnects: Minimizing the Controller Latency," *ACM Great Lakes Symposium on VLSI (GLSVLSI) Conference*, Chicago, IL, 2018, pp. 323-328. **(Invited)**

[C4] **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Enabling Efficient Tolerance Analysis in Silicon Photonic Integrated Circuits," *Progress in Electromagnetic Research Symposium (PIERS)*, Shanghai, 2016, pp. 783-783. **(Invited)**

[C5] **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "An Analytical Study of Process Variations in Silicon Photonic Integrated Circuits," *Photonics North (PN)*, Quebec City, QC, 2016, pp. 1-2. **(Invited)**

[C6] **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Modeling Fabrication Non-Uniformity in Chip-Scale Silicon Photonic Interconnects," *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, Dresden, 2016, pp. 115-120. **(Best Paper Award, Test Track)**

[C7] **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Photonic Integrated Circuits: A Study on Process Variations," *Optical Fiber Communications Conference and Exhibition (OFC)*, Anaheim, CA, 2016, paper W2A.22.

[C8] **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-ladouceur, "Silicon Photonic Integrated Circuits under Process Variations," *Asia Communications and Photonics Conference*, Hong Kong, 2015, paper ASu2A.12. **(Best Poster Paper Award)**

[C9] F. Gohring, R. Priti, **M. Nikdast**, F. Hessel, O. Liboiron-Ladouceur, and G. Nicolescu, "A Low-Latency Centralized Controller for MZI-Based Optical Integrated Networks," *International Conference on Photonics in Switching (PS)*, Florence, 2015, pp. 118-120.

[C10] L. H. K. Duong, **M. Nikdast**, J. Xu, Z. Wang, Y. Thonnart, S. Le Beux, P. Yang, X. Wu, and Zh. Wang, "Coherent Crosstalk Noise Analyses in Ring-Based Optical Interconnects," *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, Grenoble, 2015, pp. 501-506.

[C11] **M. Nikdast**, L. H. K. Duong, J. Xu, S. Le Beux, X. Wu, Z. Wang, P. Yang, and Y. Ye, "CLAP: a Crosstalk and Loss Analysis Platform for Optical Interconnects," *IEEE/ACM International Symposium on Networks-on-Chip (NoCS)*, Ferrara, 2014, pp. 172-173.

[C12] Y. Ye, X. Wu, J. Xu, **M. Nikdast**, Z. Wang, and X. Wang, "System-Level Analysis of Mesh-Based Hybrid Optical-Electronic Network-on-Chip," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Beijing, 2013, pp. 321-324. **(Invited)**

[C13] X. Wang, J. Xu, W. Zhang, X. Wu, Y. Ye, Z. Wang, **M. Nikdast**, and Zh. Wang, "Active Power-Gating-Induced Power/Ground Noise Alleviation Using Parasitic Capacitance of On-Chip Memories," *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, Grenoble, 2013, pp. 1221-1224.

[C14] W. Liu, Z. Wang, X. Wu, J. Xu, B. Li, W. Zhang, Y. Ye, Z. Wang, and **M. Nikdast**, "A Network-on-Chip Benchmark Suite Based on Real Applications," *Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW)*, China, 2013. **(Invited)**

[C15] Y. Ye, X. Wu, J. Xu, W. Zhang, **M. Nikdast**, and X. Wang, "Holistic Comparison of Optical Routers for Chip Multiprocessors," *Anti-counterfeiting, Security, and Identification (ASIC)*, Taipei, 2012, pp. 1-5.

[C16] Y. Ye, J. Xu, X. Wu, W. Zhang, W. Liu, **M. Nikdast**, X. Wang, Z. Wang, and Zh. Wang, "Thermal Analysis for 3D Optical Network-on-Chip Based on a Novel Low-Cost 6×6 Optical Router," *Optical Interconnects Conference (OI)*, Santa Fe, NM, 2012, pp. 110-111.

[C17] Z. Wang, J. Xu, X. Wu, Y. Ye, W. Zhang, W. Liu, **M. Nikdast**, X. Wang, and Zh. Wang, "A Novel Low-Waveguide-Crossing Floorplan for Fat Tree Based Optical Networks-on-Chip," *Optical Interconnects Conference (OI)*, Santa Fe, NM, 2012, pp. 100-101.

[C18] Y. Ye, J. Xu, X. Wu, W. Zhang, X. Wang, **M. Nikdast**, Z. Wang, and W. Liu, "Modeling and Analysis of Thermal Effects in Optical Networks-on-Chip," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Chennai, 2011, pp. 254-259.

[C19] W. Liu, J. Xu, X. Wu, Y. Ye, X. Wang, W. Zhang, **M. Nikdast**, Z. Wang, "A NoC Traffic Suite Based on Real Applications," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Chennai, 2011, pp. 66-71.

[C20] W. Liu, J. Xu, X. Wang, Y. Wang, W. Zhang, Y. Ye, X. Wu, **M. Nikdast**, and Z. Wang, "A Hardware-Software Collaborated Method for Soft-Error Tolerant MPSoC," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Chennai, 2011, pp. 260-265.

[C21] Y. Xie, **M. Nikdast**, J. Xu, W. Zhang, Q. Li, X. Wu, Y. Ye, W. Liu, and X. Wang, "Crosstalk Noise and Bit Error Rate Analysis for Optical Network-on-Chip," *Design Automation Conference (DAC)*, Anaheim, CA, 2010, pp. 657-660.

[C22] X. Wu, Y. Ye, W. Zhang, W. Liu, **M. Nikdast**, X. Wang, and J. Xu, "UNION: A Unified Inter/Intra-Chip Optical Network for Chip Multiprocessors," *IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch)*, Anaheim, CA, 2010, pp. 35-40. **(Invited)**

[C23] H. Ahmadi and **M. Nikdast**, "Age-Based Adaptive Routing Algorithm for Network-on-Chip," *Iranian Student Conference in Electrical Engineering (ISCEE)*, Tabriz, 2009.

[C24] M. Davarpanah, A. Mohamad Shafiee, **M. Nikdast**, and M. Montazeri, "A Predetermined Routing Algorithm for Network-on-Chip," *Iranian Conference on Electrical Engineering (ICEE)*, Tehran, 2009.

[C25] A. M. Shafiee, **M. Nikdast**, and M. Montazeri, "Parameterized Intermittent Routing Algorithm in Networks-on-Chip," *IEEE International Conference on Emerging Trends in Computing (ICETiC)*, India, 2009.

[C26] B. Soleimani, E. Shahabian, M. yavari, and **M. Nikdast**, "A Novel Heuristic for Solving the 8 Puzzle Problem Based on IDA Method," *Iranian Student Conference in Electrical Engineering (ISCEE)*, Zanjan, 2008.

2.10 Other Publications

[A1] **M. Nikdast**, "Research Papers: Writing Tips and Top-Tier Targets," *IEEE Potentials*, vol. 36, no. 3, pp. 26-29, May-June 2017.

[A2] **M. Nikdast**, "Research Tips for First-Year Ph.D. Students," *IEEE Potentials*, vol. 35, no. 3, pp. 18-20, May-June 2016.

[A3] S. Sinha and **M. Nikdast**, "Finding Happiness and Satisfaction During Your Ph.D. Program," *IEEE Potentials*, vol. 34, no. 3, pp. 36-38, May-June 2015.

2.11 Refereed Conference Poster Presentations

[P1] **M. Nikdast**, G. Nicolescu, and O. Liboiron-Ladouceur, "Fault-Tolerant Optical NoCs: An Approach Based on Microresonators Design Space Exploration," *Design Automation Conference (DAC)*, San Francisco, 2018. (Late Breaking Results Submission)

[P2] **M. Nikdast**, G. Nicolescu, J. Trajkovic, and O. Liboiron-Ladouceur, "Photonic Integrated Circuits: a Study on Process Variations," *IEEE/OSA Montreal Networking Event and Poster Competition*, Montreal, QC 2017.

[P3] **M. Nikdast**, "Silicon Photonic Interconnects: Design Opportunities and Challenges," *University of Concordia Postdoctoral Research Day*, Montreal, QC 2015.

[P4] **M. Nikdast**, "Optical Interconnects for Computing Systems: a Formal Study on Signal-to-Noise Ratio," *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, Grenoble, 2015. (Ph.D. Forum)

[P5] **M. Nikdast** and J. Xu, "On the Impact of Crosstalk Noise in Optical Networks-on-Chip," *Design Automation Conference (DAC)*, San Francisco, 2014. (Ph.D. Forum)

[P6] Z. Wang, J. Xu, X. Wu, X. Wang, Zh. Wang, **M. Nikdast**, P. Yang, "Holistic Modeling and Comparison of Inter-Chip Optical and Electrical Interconnects," Design Automation Conference (DAC), San Francisco, CA 2014. (Work in Progress)

[P7] W. Liu, J. Xu, X. Wu, Y. Ye, X. W., W. Zhang, **M. Nikdast**, and Z. Wang, "MCSL: A Realistic Traffic Benchmark Suite for Network-on-Chip Studies," *Design Automation Conference (DAC)*, San Francisco, CA 2011. (Work in Progress)

[P8] W. Liu, J. Xu, X. Wang, Y. Wang, W. Zhang, Y. Ye, X. Wu, *M. Nikdast*, and Z. Wang, "A Low-Overhead Hardware-Software Collaborated Approach for Soft-Error Tolerance," *Design Automation Conference (DAC)*, San Diego, CA 2011. (Work in Progress)

[P9] **M. Nikdast**, J. Xu, X. Wu, Y. Ye, W. Liu, and X. Wang, "A Formal Analysis of Crosstalk Noise in Mesh-Based Optical Networks-on-Chip for Chip Multiprocessors," *AMD Technical Forum and Exhibition (AMD-TFE)*, Taipei, 2010. **(Best Project Award, Second place)**

[P10] W. Liu, X. Wang, J. Xu, X. Wu, Y. Ye, and **M. Nikdast**, "A Case Study of On-Chip Sensor Networks for Soft-Error Tolerant Multiprocessor Systems-on-Chip," *AMD Technical Forum and Exhibition (AMD-TFE)*, Taipei, 2010.

[P11] **M. Nikdast** and M. Montazeri, "Analysis of Different Routing Algorithms in NoCs," *Iranian Student Conference in Electrical Engineering (ISCEE)*, Zanjan 2008.

2.12 Thesis

[T1] **M. Nikdast**, "Signal-to-Noise Ratio in Optical Interconnection Networks: Analysis, Modeling, and Comparison," Ph.D. Dissertation, *The Hong Kong University of Science and Technology (HKUST)*, Hong Kong, December 2013.

2.13 Invited Talks

[IT1] Multiprocessor Computing Systems Integrating Silicon Photonic Interconnects. *Ingram School of Engineering, Texas State University*, TX, USA, April 2017.

[IT2] Multiprocessor Computing Systems Integrating Silicon Photonic Interconnects. *Electrical and Computer Engineering Department, Colorado State University*, CO, USA, February 2017.

[IT3] Silicon Photonic Interconnection Networks for Multiprocessor Computing Systems: Let's Meet in the Middle!. *Electrical and Computer Engineering Department, University of Toronto*, ON, Canada, November 2016.

[IT4] Enabling Tolerance Analysis in Silicon Photonic Integrated Circuits. *Progress in Electromagnetics Research Symposium (PIERS) - Special Session on Nanophotonics and Integration*, Shanghai, China, August 2016.

[IT5] An Analytical Study of Process Variations in Silicon Photonics Integrated Circuits. *Photonics North Conference*, QC, Canada, May 2016.

[IT6] Fabrication Non-Uniformity in Silicon Photonic Interconnects. *Optical/Photonic Interconnects for Computing Systems (OPTICS) Workshop*, Dresden, Germany, March 2016.

[IT7] CLAP: a Crosstalk and Loss Analysis Platform for Optical Interconnects. *IEEE/ACM International Symposium on Networks-on-Chip (NoCs) - Special Session on Silicon Photonic Interconnects*, Ferrara, Italy, September 2014.

[IT8] Formal Worst-case Analysis of Crosstalk Noise in Mesh-based Optical Networks-on-Chip. *Networks-on-Chip Workshop - HKUST*, Hong Kong, October 2012.

[IT9] A Formal Analysis of Crosstalk Noise in Mesh-Based Optical Networks-on-Chip for Chip Multiprocessors. *AMD Technical Forum and Exhibition*, Taipei, Taiwan, October 2010.

[IT10] Bit Error Rate Analysis in Optical Networks-on-Chip. *School of Electrical and Computer Engineering, University of Tehran*, Tehran, Iran, July 2010.

3 Educational Activities

3.1 Ph.D. Thesis Committee Member

Physical Layer Modeling and Optimization of Silicon Photonic Interconnection Networks *Dr. Meisam Bahadori, Columbia University, June 2018 (External Committee Member)*

3.2 Teaching Experience at CSU

ECE 580B6 *Silicon Photonics for Computing Systems, Fall 2018*

ECE 102 *Digital Circuit Logic, Spring 2018*

ECE 451 *Digital System Design, Fall 2017*

3.3 Courses Developed at CSU

ECE 580B6 *Silicon Photonics in Computing Systems*

3.4 Professional Development (Participated)

DAC Young Faculty Workshop *Design Automation Conference (DAC), Summer 2018*

DAC Young Faculty Workshop *Design Automation Conference (DAC), Summer 2016*

Clarifying Expectations for Supervision *McGill University, QC, Canada, Winter 2016*

Crafting Your Research Future *Center for Enhanced Learning and Teaching, HKUST, Spring 2013*

Prepare for Your Academic Career *Center for Enhanced Learning and Teaching, HKUST, Spring 2013*

Modern Engineering Research Methodology *ECE Department, HKUST, Spring 2012*

Effective Research Process *ECE Department, HKUST, Hong Kong, Spring 2011*

4 Professional Activities

4.1 Editorial Activities

2018-present
Guest Editor, Elsevier Journal on Sustainable Computing (SUSCOM).

2017-present
Guest Editor, ACM Journal on Emerging Technologies in Computing (JETC), Special Issue on Emerging Networks-on-Chip: Designs, Technologies, and Applications.

4.2 Conference Steering Committee

2018-present
North American Workshop on Silicon Photonics for High Performance Computing (SPHPC).

2015-present
International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS).

4.3 Conference Organizing Committee (General Chair)

2018-present
North American Workshop on Silicon Photonics for High Performance Computing (SPHPC).

4.4 Conference Organizing Committee (Technical Program Committee Chair)

2015-present
International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS).

4.5 Conference Organizing Committee (Other Chaired Positions)

2018
Publicity Chair - International Workshop on Network-on-Chip Architectures (NoCArc).

2018
Publication Chair - IEEE Computer Society Annual Symposium on VLSI (ISVLSI).

2017-present
Ph.D. Forum Chair - IEEE International Green and Sustainable Computing Conference (IGSC).

4.6 Special Session Organizing Committee

2018
Special Session on "Emergence of Silicon Photonics in High-Performance Computing: How can the VLSI Community Contribute?". *ACM Great Lakes Symposium on VLSI (GLSVLSI) Conference*, Chicago, IL.

4.7 Technical Program Committee (TPC) Member

2018
International Workshop on Network-on-Chip Architectures (NoCArc).

2018
IEEE Computer Society Annual Symposium on VLSI (ISVLSI).

2018
ACM SIGDA Ph.D. Forum - Design Automation Conference (DAC).

2018
ACM Great Lakes Symposium on VLSI (GLSVLSI).

2018
IEEE International Conference on High Performance Computing and Communications (HPCC).

2018
International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (AISTECS).

2017-present
IEEE International Green and Sustainable Computing Conference (IGSC).

4.8 Conference Technical Session Chair

2018
IEEE/ACM Design Automation Conference (DAC).

2018
ACM Great Lakes Symposium on VLSI (GLSVLSI).

2017
IEEE International Green and Sustainable Computing Conference (IGSC).

2017
International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS).

4.9 Referee/Reviewer Activities

Journals:
IEEE Photonics Technology Letters (PLT), since 2015.
IEEE Journal on Lightwave Technology (JLT), since 2015.
IEEE Transactions on Very Large Scale Integration (TVLSI), since 2013.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), since 2013.
IEEE Design and Test of Computers (D&T), since 2013.
IEEE Transactions on Parallel and Distributed Systems (TPDS), since 2013.
IEEE Transactions on Emerging Topics in Computing (TETC), since 2013.
IEEE Transactions on Multi-Scale Computing Systems (TMSCS), since 2013.
IEEE Transactions on Computers (TC), since 2013.
IEEE Computer Architecture Letters (CAL), since 2013.

ACM Transactions on Embedded Computing Systems (TECS), since 2013.
ACM Journal on Emerging Technologies in Computing (JETC), since 2013.
Elsevier Journal on Sustainable Computing (SUSCOM), since 2018.
Elsevier Journal of Systems Architecture (JSA), since 2013.
Elsevier Journal on Microprocessors and Microsystems (MICPRO), since 2013.
Elsevier International Journal for Light and Electron Optics (OPTIK), since 2013.
Elsevier Journal on Integration, the VLSI Journal (VLSI), since 2013.
Elsevier Journal on Computer Physics Communications (CPC), since 2013.

Conferences:
IEEE/ACM Design Automation Conference (DAC), since 2015.
IEEE/ACM Design Automation and Test in Europe (DATE) Conference and Exhibition, since 2015.
Asia and South Pacific Design Automation Conference (ASP-DAC), 2014-2016.
Embedded Systems Week (ESWEEK, CODES+ISSS, and CASES), 2014-2016.
IEEE International Conference on Computer Aided Design (ICCAD), 2014-2016.
IEEE Computer Society Annual Symposium on VLSI (ISVLSI), since 2016.
International Symposium on Networks-on-Chip (NOCS), 2013-2015.
IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2013-2015.

4.10 University, College, and Department Service

Committee: Engineering Student Technology Committee (ESTC)
Activity: Member, 2017 – present.