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SURVEY

A Survey on Optical Phase-Change Memory: The Promise and Challenges

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ABSTRACT Silicon photonics (SiPh) technology has facilitated the deployment of integrated photonics across different application domains, from ultra-fast communication in Datacom applications to energy-efficient optical computation in emerging hardware accelerators for machine learning. More recently, the integration of SiPh and phase change materials has created a unique opportunity to realize adaptable, reconfigurable, and programmable photonic platforms. In particular, the nonvolatile programmability in phase change materials has made them a promising candidate for implementing photonic memory cells and architectures. Accordingly, photonic memory systems and even in-memory photonic computing paradigms are on the rise, especially given their potential for improving data access in electronic and photonic processors. However, there are still many challenges in the design and fabrication of phase-change photonic integrated circuits, which need to be addressed. This article presents a comprehensive survey on the recent advances and challenges for the integration of phase change materials with contemporary photonic devices while focusing on the photonic memory application. In particular, we explore phase-change photonic memory from the material level to the architecture level by presenting an overview of different material-level characteristics of phase change materials with their optical, electrical, and thermal properties as well as their integration into SiPh devices and photonic memory architectures and their application for in-memory photonic computing. We also present a comparison with electronic memory and discuss open research challenges that must be addressed to further advance phase-change photonic memory towards successful integration into emerging computing systems.

INDEX TERMS Phase change materials, phase-change memory, in-memory photonic computing, photonic integrated circuits, silicon photonics.

I. INTRODUCTION

With the rapid growth in the diversity and amount of data in emerging data-oriented machine learning (ML) and artificial intelligence (AI) applications, the need for memories with higher cell densities, lower power consumption, higher scalability, longer lifetime, and higher bandwidth has risen. As the size and complexity of emerging applications increase, conventional CMOS-based volatile memories, such as SRAMs and DRAMs, are facing difficulties in meeting energy efficiency [1], scalability [2], [3], volume [4], speed, and bandwidth requirements [5]. These shortcomings motivate the consideration of alternative memory technologies in future computing systems, such as phase-change memories. Compared to other nonvolatile memories such as ReRAMs and Flash memories, phase-change memories offer higher stability, enhanced retention time, and higher switching speed [5], [6], [7], [8], [9].

Phase change materials (PCMs) can switch between the amorphous and crystalline states in the presence of an external energy source. Their unique and tunable switching dynamics upon exposure to an external energy source enable

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them to have two vastly different nonvolatile electrical and optical properties depending on their state. In early 1971, a research group from Bell Telephone Laboratories discovered nonvolatile characteristics of PCMs by using As-Te-I alloys in the very first phase-change-material-based devices, since the material showed two significantly distinct conductivity levels depending on its thermodynamic phase [10]. Later in 1987, many companies such as Intel, IBM, and HITACHI exploited these properties related to phase change materials to manufacture re-writable data storage devices, like CDs and DVDs [10].

Due to nonvolatile phase transitions between the two or more states in PCMs, phase-change memories have recently shown promise in new nonvolatile memory architectures to replace traditional DRAMs [11]. Memory cells based on PCMs may be written to and read from multiple times with substantially reduced area consumption, improved bandwidth, and higher scalability [2], [3]. The energy required to control the state of phase-change memories can be provided either via electrical current (through Joule heating) in electrically driven phase-change memories (EPCMs), or using optical signals (through optical absorption) like a laser pulse in optically driven phase-change memories (OPCMs). In EPCMs, data can be stored by changing the conductivity level induced by the phase transition of the PCM, which in turn depends on the amplitude and duration of the applied electrical current. In contrast, in OPCMs, data is stored in the optical transmission level induced by the phase transition of the PCMs depending on the power and duration of laser pulses. A single OPCM cell can have up to 32 transmission levels, which is enough to store up to five bits per cell [12]. This leads to about two times enhancement in memory performance, about four times lower read energy-per-bit and six times lower write energy-per-bit compared to conventional DRAMs [5], [12].

In addition to having more energy-efficient data storage, reducing energy and latency for data movement on electrical links has always been a challenging task in CMOS integrated circuits. For instance, on a modern CMOS computing system, 0.1–0.2 pJ/bit is required to transfer data over a 1-mm-long electrical interconnect used for on-chip communication, such as in the case of a processing core accessing an L2 cache bank. This number goes up to 1–4 pJ/bit over longer electrical links, such as in the case when a core accesses remote L3 cache banks. In addition, it takes up to 30 pJ/bit for off-chip communication when a core needs to access the CMOS main memory (i.e., DRAMs) [13], [14], [15]. While the absolute values of these energy costs may seem low, in fact, they are significantly higher than the energy budget required for future computing systems. This data movement overhead imposes severe limitations on the scalability of CMOS integrated circuits [13]. To address the aforementioned limitations, due to their compatibility with CMOS integrated technology, silicon photonic (SiPh) devices have been widely employed in emerging integrated circuits to exploit photons instead of electrons to transfer data [16]. In particular, state-of-the-art SiPh links have been used to support on-chip and off-chip communication with substantially lower energy consumption and latency over longer distances, with a higher bandwidth (e.g., ≈51.2 Tb/s compared to 112 Gb/s for state-of-the-art electrical links) [17]) than conventional electrical links. Thus, SiPh offers scalability with enhanced energy efficiency and performance and compatibility with contemporary CMOS fabrication technology, making it an attractive choice to support data movement in future processing chips. For example, the work in [5] suggests using SiPh links instead of electrical links to facilitate the data movement to and from OPCM cells to further minimize the latency and static power consumption in future photonic memory systems [5].

Despite the benefits that OPCMs may offer, research suggests that implementation of OPCM is challenging due to its essential need for electro-optical and opto-electrical conversions to convert the electrical signals coming from a memory controller to optical signals and vice versa. Consequently, one cannot simply replace a DRAM cell with an OPCM cell. Therefore, the entire memory architecture needs to be redesigned to make it compatible with OPCM arrays. In addition, OPCM cells are extremely sensitive to thermal variations stemming from the static power consumption of nearby photonic and electronic components. This can lead to variations in optical transmission level, hence increasing the write and read error rates [5]. A higher area consumption compared to conventional DRAM main memories can be considered as another challenge facing the implementation of OPCMs.

In this paper, we present a comprehensive survey on recent advances and challenges in the application of PCMs from material-level to system-level in photonic memory and in-memory computing systems. In addition, we discuss simulation methods and challenges facing the design of phase-change memories and in-memory computing units based on PCMs in detail. A few review papers on similar topics have been published in recent years. The work in [18] presents a survey on the application of PCMs for reconfigurable silicon photonics. Starting from a brief overview of the optical properties of PCMs, this work focuses on the application of PCMs in silicon-photonic switching networks and modulators. In addition, it presents a brief survey of the application of PCMs in photonic computing units. However, the paper's outlook and scope are limited to device-level designs. Hence, the challenges of PCM-based memory and in-memory computing systems have not been discussed. The work in [19] and [20] also presents a survey on photonic devices based on PCMs. However, these papers focus on the thermodynamic and switching properties of PCMs and their application in reconfigurable photonic devices, such as active plasmonics, metamaterials, and color displays. They do not discuss PCM-based photonic memory and in-memory computing systems and related open challenges, as it is done in this survey. The organization of this paper is as follows:

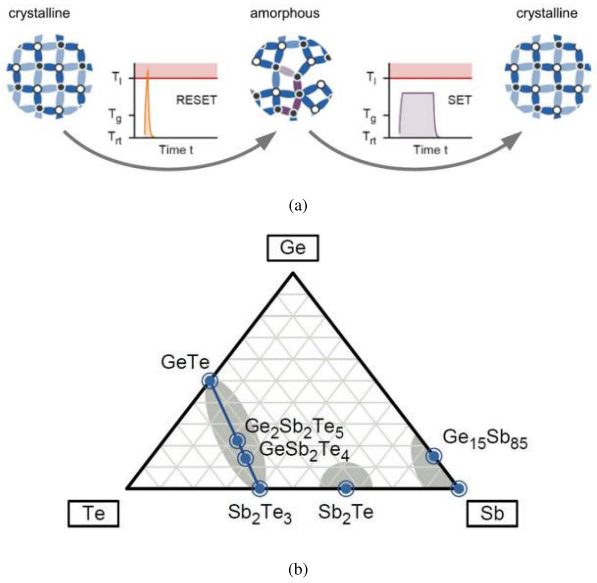

FIGURE 1. (a) Set and reset procedures in phase-change memories. (b) The most conventional Ge-Te-Sb alloys for nonvolatile photonic memory applications [18]. Permission: https://creativecommons.org/licenses/by/4.0/.

- **Section II** presents an overview and fundamentals of PCMs and their working mechanisms for memory applications, along with their thermal, electrical, and optical properties as well as their physical and thermodynamic properties.
- **Section III** provides an overview of the applications of PCMs in data storage cells for photonic memories and their different design approaches and read and write policies. Moreover, we review recent phase-change memory architectures and applications of PCMs to implement in-memory computing units for computationally expensive applications, such as ML and AI applications. Furthermore, this section describes the simulation of a single photonic memory cell based on GeSbTe alloys (GST) for photonic memory applications.
- **Section IV** presents a bottom-up overview of the design challenges of OPCMs and their architectures. Challenges such as power and latency trade-offs, the complexity of OPCM's designs, and endurance will be discussed in this section. Some of the state-of-the-art applications of phase change materials for programmable photonics and photonic tensor cores will be also discussed in this section.
- **Section V** concludes the paper and presents a summary of different applications of PCMs reviewed in this paper.

II. PHASE CHANGE MATERIALS: AN OVERVIEW

In this section, we present an overview of PCMs, including their thermal, optical, and electrical properties.

A. FUNDAMENTALS OF PHASE CHANGE MATERIALS

The molecular structure of a material can have a big impact on its optical and electrical characteristics. Furthermore, even the same material with a specific molecular structure at room temperature, such as silicon (Si), can have variable optical and electrical characteristics depending on its crystallographic orientation. When heated with an external energy source (i.e. electric field or optical signal), the temperature of PCMs starts to increase by absorbing the energy of the heat source. One important material parameter related to PCMs is the melting temperature (T_l). The regions of the material after exposure to the heat source that has a temperature above T_l will be melted and quenches (cools down with the rates higher than 10^9 K.S^{-1} [21]) in about 700 picoseconds [22]. The quenched region will have an amorphous structure regardless of the initial state of the material. This process is called reset (see Fig. 1(a)) or amorphization. The temperature distribution of the material with a given geometry can be obtained by solving the unsteady-transient heat flow equation [22]. The simulation approaches of PCM-based photonic devices will be explained in detail in Section III-E.

PCMs can repeatedly change their phase from amorphous (crystalline) to crystalline (amorphous) states (see Fig.1(a)). In addition, PCMs can be fully crystallized, fully amorphous, or partially crystallized/amorphous (intermediate state) depending on the duration and power of the heat source. Hence, different electrical and optical properties at each state can be achieved. Typically, we desire to have a low T_l because it will result in low power and fast reset (amorphization) of the material. Another important material parameter is the crystallization temperature (T_g). When the material in the intermediate state absorbs energy through an energy source, the regions of the material which have higher temperatures than T_g and lower than T_l will recapture the crystalline structure. This process is called set (see Fig. 1(a)) and can take hundreds of nanoseconds or higher [21]. High T_g is desirable to improve the phase stability of the material, which is crucial to enable reliable data retention in nonvolatile memories [23].

The response time of nonvolatile memory cells plays an important role in determining the average memory-access latency in memory systems. The average memory-access latency needs to be as low as possible. The reason for this is that in highly parallel processors, most of the time is consumed during the multiple access to the main memory per cycle, and having high average memory-access latency can act as a bottleneck for the speed of the whole system. Thus, the lower average memory-access latency leads to a higher speed of the whole processing system [24], [25]. The average memory latency can vary from hundreds of picoseconds to hundreds of nanoseconds depending on the architecture of the cell types and the memory architecture. High read and write latency of the memory cells lead to higher average memory latency and lower read and write throughput of the memory systems.

The average memory latency can be decreased by increasing the number of bits stored in a single OPCM cell [5]. The very first materials that showed such a fast response, as well as high optical contrast between the two phases to

store logic 1 or logic 0, were GeTe and GeTeSnAu alloys [26]. In addition, pseudo-binary alloys of GeTe-Sb_2Te_3 like $Ge_1Sb_4Te_7$, $Ge_1Sb_2Te_4$, and $Ge_2Sb_2Te_5$ (known as GST) were used for photonic memory applications (see Fig. 1(b)) [26]. The state-of-the-art OPCMs require 25 nanoseconds to be written and read [25]. In addition, PCMs must have a high optical transmission contrast (when the optical transmission level is being used to store the data) and a high resistance contrast for different states (when conductivity or resistance level is being used to store the data), long durability over time, and a large capacity to be considered as a suitable candidate for data storage applications. Among the aforementioned materials, GST is the most popular material for photonic nonvolatile data storage because of having distinctive optical transmission and resistance levels related to crystalline and amorphous states. Conventional PCMs (e.g., GST) have a fast transition speed and different distinctive optical and electrical properties depending on their phase. PCMs tend to maintain their state even when the external energy source is turned off, making them a promising alternative for developing nonvolatile photonic memory cells due to their dynamic and adjustable optical and electrical characteristics in each state [10], [26], [27], [28], [29], [30].

B. THERMAL PROPERTIES

One of the most important parameters related to PCMs is thermal conductivity which determines the rate of heat transfer in the material. As the thermal conductivity increases, the material is able to absorb and transfer the heat faster. In the previous section, we discussed how the energy of a heat source will be absorbed by the material where this energy will then trigger the phase transition of the PCM. PCMs have a relatively low thermal conductivity which means that they are unable to quickly absorb the energy from a material with low thermal conductivity. This makes the phase transition to be slow in PCMs. As we enhance the thermal conductivity of the material, lower energy will be needed to induce the phase transition in the material because a higher portion of the absorbed energy contributes to the temperature variation of the material [31]. The work in [32] and [33] reports experimental results on thermal conductivity for the most conventional PCMs (GST) in amorphous and crystalline states. We can see from Table 1 that for GST, the thermal conductivity for amorphous and crystalline GST is about 0.19 and 0.57 W/mK, respectively. This is relatively low compared to conventional semiconductor materials such as silicon with thermal conductivity of 148 W/mK at room temperature. Table 1 shows the thermal properties of different materials that can be used to obtain a single photonic memory cell for data storage.

Another important thermal property related to PCMs is the thermo-optic effect. So far, we have discussed how phase transitions in PCMs can be induced by optical or electrical signals. However, considering the physics of the devices, any change in the temperature of the material can impose a change in its optical properties, such as the material's refractive index and extinction coefficient via thermo-optic effect. The refractive index is a parameter that determines the group velocity of an electromagnetic wave in a medium. Also, the extinction coefficient is a parameter which describes the loss (absorption) of an electromagnetic wave in a medium. The thermo-optic coefficient of a material quantifies the changes in its optical properties in the presence of thermal variations. The work in [36] proposed analytical models to monitor the thermo-optic effect and changes in the refractive index and extinction coefficient in GST caused by temperature variations. The work in [36] suggests that the change in the refractive index (n) of PCMs leads to an excessive phase shift while the change in the imaginary part (κ) leads to additional attenuation caused by material loss. Therefore the ratio of the change in the real part of the refractive index to the change in the imaginary part of the refractive index ($\Delta n/\Delta k$) was used as a figure of merit for the proposed analytical models in [36]. They captured the real and the imaginary part of the thermo-optic coefficient of GST experimentally and showed that the real and imaginary parts of the crystalline and amorphous GST can change significantly under temperature variations.

C. ELECTRICAL PROPERTIES

The current flow in PCMs has a different nature in comparison to semiconductors. Because of their molecular structure, resistance in PCMs can be described by electrons hopping between traps in the PCM's lattice. Like any other molecular structure, the current in a PCM can be modelled via Poole-Frenkel transport of electrons through traps [10], [26]. Therefore, the current flow in a PCM depends on the distance and the potential barrier among traps. Due to the crystallographic structure of PCMs in amorphous state, the potential barrier between traps is higher. Thus, PCMs in the amorphous state have much higher resistance than in the crystalline state. By applying an electric field to a PCM, the potential barrier between traps can be lowered, and so will the resistivity of the PCM in the amorphous state. Experimental results show that such resistivity decreases linearly with an increase in the electric field [10]. Further increasing the applied electric field will lead to a collapse of the local electric field between traps, which leads to a negative resistance in the material and a sharp drop in the resistivity without any phase change. In a negative resistance state, switching off the voltage source will lead to regaining the original resistance level of the material in amorphous state in the absence of the electric field. Applying a sufficiently high electric field ($\approx$ 562 MV/m [37]) over a specific time period ($\approx$ 100 ns [37]) will lead to reaching crystallization temperature (T_c) and a phase change from amorphous to crystalline state.

A PCM in the crystalline state has higher conductivity compared to amorphous state. This property is nonvolatile and revertible, meaning that switching off the voltage source will not change the resistivity of the PCM in the crystalline

TABLE 1. Thermal properties of common phase change materials used in phase-change memory cells (a: amorphous and c: crystalline).

Material	Thermal Conductivity (W/mK)	Heat Capacity (C_p)—(J/gK)	Density (ρ)—(gr/cm^3)
a-GST [33]	0.19	0.213	5.87
c-GST [33]	0.57	0.199	6.27
a-GSST [34]	0.2 ± 0.02	1.5 ± 0.1	5.27
c-GSST [34]	0.48 ± 0.06	1.8 ± 0.1	5.53
Si_3N_4 [35]	10-43	0.673 - 1.100	2.37-3.25

state. The same procedure can be exploited to change a PCM's state from amorphous to crystalline [10], [26], [27], [28], [29], [30]. Depending on the electrical current's amplitude and duration, energy will be provided for a phase-change memory cell through joule's heating (Ohmic heating) to trigger the phase transition to perform write or reset.

D. OPTICAL PROPERTIES

Understanding the optical properties in PCMs is of the essence when it comes to their application in photonic integrated circuits. Depending on their state, PCMs have various optical characteristics. As a general rule and in comparison to the amorphous state, PCMs in the crystalline state are extremely absorbing due to their high extinction coefficient and this is the main reason for the optical transmission contrast they exhibit. This property makes PCMs suitable for implementing phase-change memories by storing logical bits and decoding them into the optical transmission levels of the material originating from phase transitions. PCMs can also take intermediate states, which means that some portion of them can be in the crystalline state while the remaining portion is in the amorphous state.

PCM's effective permittivity determines the electric polarizability. Electric polarizability describes the dipole moment of the material when subjected to an electric field and directly affects the material's dielectric constant and refractive index [40]. The effective permittivity (ε_{eff}) of a PCM in an intermediate state, can be estimated using the Lorenz mathematical model [22], [41]:

$$\frac{\varepsilon_{eff}(\lambda)-1}{\varepsilon_{eff}(\lambda)+2} = X_f \times \frac{\varepsilon_c(\lambda)-1}{\varepsilon_c(\lambda)+2} + \left(1-X_f\right) \times \frac{\varepsilon_a(\lambda)-1}{\varepsilon_a(\lambda)+2}. \tag{1}$$

Here, X_f is the crystalline fraction and takes a number between 0 and 1, illustrating the portion of the PCM which is in the crystalline state. Moreover, the wavelength-dependent dielectric permittivity function ($\varepsilon(\lambda)$) can be calculated as:

$$\varepsilon_a = n_a^2, \tag{2}$$
$$\varepsilon_c = n_c^2, \tag{3}$$

where n_c and n_a are the complex refractive indices of the PCM. Finally, using (1), the real and the imaginary part of the effective refractive index—which determines the phase delay and absorption of the light in a material—of a PCM in an intermediate (mixed) state can be estimated as [22]:

$$n_{eff} = \sqrt{\frac{\sqrt{(\varepsilon_1+\varepsilon_2)^2}+\varepsilon_1}{2}}, \tag{4}$$

$$k_{eff} = \sqrt{\frac{\sqrt{(\varepsilon_1+\varepsilon_2)^2}-\varepsilon_1}{2}}. \tag{5}$$

In (4) and (5), ε_2 and ε_1 are the real and imaginary part of $\varepsilon_{eff}(\lambda)$ in (1) [22].

The refractive index (n) and extinction coefficient of conventional (κ) PCMs are depicted in Fig. 2. We can observe that the materials in the crystalline state have a much higher extinction coefficient compared to their amorphous state. This means that materials in the crystalline state absorb more optical power compared to the amorphous state and convert it into heat to be used to trigger the phase transition. The amount of absorbed optical power in the crystalline state is significantly higher compared to the amorphous state because of the imaginary part of the refractive index in the crystalline state is higher compared to the amorphous state. The absorption coefficient—α (cm^{-1})—of PCMs can be calculated from their extinction coefficient (κ) for any given wavelength according to the following model [10]:

$$\alpha = \frac{4\pi\kappa}{\lambda}. \tag{6}$$

Note that when the extinction coefficient is higher, the absorption coefficient of the material is also higher, and hence laser pulses with lower power and duration are needed to trigger the phase transition. From Fig. 2(c), we can observe that GST has reasonably high absorption due to its high extinction coefficient in the crystalline and amorphous state for O-band (1260 nm–1360 nm) and C-band (1530 nm–1565 nm), compared to other PCMs which make the phase transitions efficient in terms of latency and energy consumption. It is also shown in Fig. 2 that the extinction coefficient in the amorphous state is lower than that in the crystalline state which, compared to the crystalline state, results in more transparency of PCMs in the amorphous state as well as lower absorption in this state.

III. PHOTONIC MEMORY BASED ON PHASE CHANGE MATERIALS

In this section, we review the state-of-the-art photonic memory storage cells as well as their advantages and challenges, recent work on photonic memory architectures, and finally, some recent efforts on using PCMs for photonic in-memory computing.

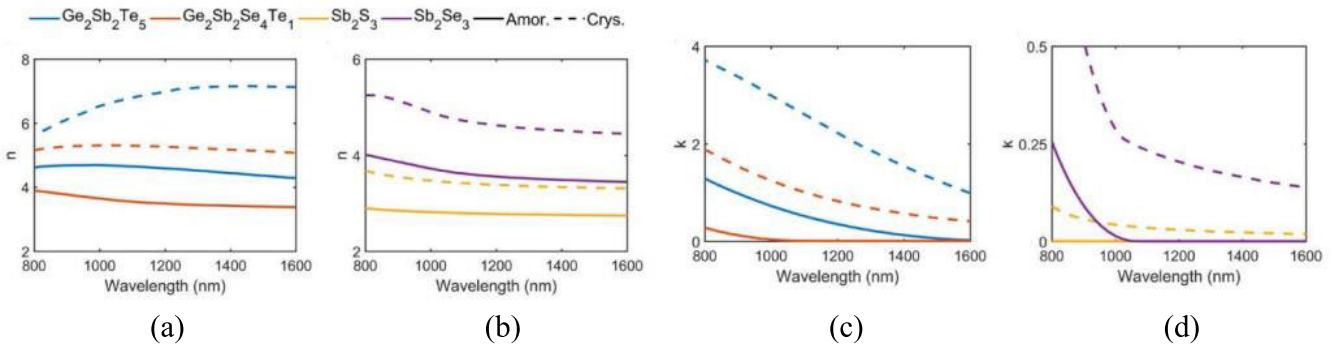

FIGURE 2. Refractive index profile of the most conventional phase change materials. *n* is the real part of the refractive index and *k* is the imaginary part of the refractive index (extinction coefficient) [38], [39]. Permission: https://creativecommons.org/licenses/by/4.0/.

A. EPCMs AND OPCMs

In Section II-A, we showed that to trigger phase transitions in a PCM, the material should absorb energy, which leads to temperature variation in the PCM. The required energy for a phase change can be provided by absorbing the energy from an external heat source with a specific duration and power level. For example, the required energy can be provided via electrical current or optical laser pulses. Because of light absorption in PCMs, optical signals can be used to trigger the phase transition and optically control PCMs.

In electrically controlled PCMs [42], [43], [44], electrical current or bias voltage can be used to trigger the phase transition in the PCMs. By applying an electric field, the joule heating in the PCM can trigger the phase transition. Depending on the amorphous/crystallized portion of the material, the resistance and optical transmission in the PCM will change. Eventually, the state of the PCM can be read via an optical or electrical read signal. For hybrid cells, it is possible to set the state of the phase-change memory cells using an optical signal and read the state using an electrical signal, and vice-versa [45], to reduce the energy consumption of the cells. To take advantage of the interesting properties of PCMs to implement phase-change memories, one should have a clear insight into their electrical and optical properties.

The most conventional way to exploit a PCM for memory architectures is to control the cells with an electrical field, known as electrically-driven phase-change memories (EPCMs). The work in [46] proposed a method to architect EPCMs to address the scalability issue of conventional DRAMs. Their baseline design showed higher energy consumption and latency compared to conventional DRAMs. However, they realized that using EPCMs instead of conventional DRAMs could help further scale the architecture. There are several other memory architecture designs based on EPCMs [6], [47], [48]. Table 2 lists some advantages and disadvantages of EPCM-based architectures compared to conventional DRAMs based on some recent work in this area. Compared to DRAMs, EPCMs can store a higher number of bits per cell (up to 2 bits per cell [5]), leading to multilevel cells (MLCs), and they are more scalable and stable under thermal variations. However, they suffer from higher latency and energy consumption (e.g., ≈50 ns for reset and ≈60 ns for read [5]), require additional circuitry such as charge pump circuits, and have lower endurance because of aging of EPCM cells (e.g., 1e8 writes compared to DRAMs that support >1e16 writes [6], [9], [46], [48], [49].

TABLE 2. Advantages and disadvantages of EPCMs compared to DRAMs.

Advantages	Disadvantages
Multilevel cell (MLC) [6], [9], [48]	Higher latency [46]
Scalability [46]	Higher energy consumption [6], [9], [48]
Thermal stability [50]	Charge pump circuit requirement [51]
—	Lower endurance [52]

Despite several advantages of EPCMs, such as enhanced MLC capacity with up to 2 bits per cell [5], [6], they suffer from high power consumption and latency. This limits the employment of EPCMs in emerging nonvolatile data storage architectures. To overcome these limitations, optically driven phase-change memories (OPCMs) have been recently introduced that use electromagnetic waves instead of electrons to control the state of phase-change memory cells. OPCMs will be discussed in detail in Section III-B. Here, we give a comparison of OPCMs against EPCMs. Most of the limitations related to EPCMs can be addressed by exploiting OPCMs in the optical domain. Table 3 highlights the comparison between OPCMs and EPCMs. Compared to EPCMs, OPCMs offer lower latency and power consumption (e.g., 60 to 130 pJ with 25 ns for read and write [12]), higher MLC capacity (up to 5 bits per cell [12]), and higher bandwidth (e.g., 1 GHz [53]) with a lifetime of 1e6–1e8 writes per cell [54]. However, such benefits come at the cost of using a complex electro-optic unit, re-design of read and write policies, accumulated optical loss and crosstalk upon scaling, need for silicon photonic links, and sensitivity to thermal variations. Due to the novel nature of OPCMS, the research related to exploiting OPCMs for scalable nonvolatile photonic memory architectures is constantly evolving [5], [12], [18], [36], [53], [55].

B. OPCM STORAGE CELLS

In this section, we first discuss the compatibility of silicon nitride and silicon platforms with PCMs as well as the benefits each platform offer when integrating with PCMs.

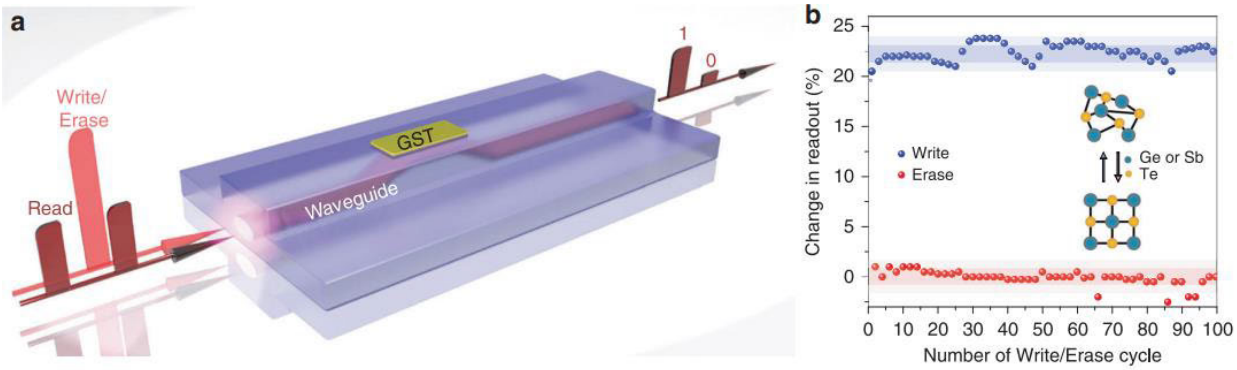

FIGURE 3. (a) Schematic of a photonic-memory cell using Si_3N_4 waveguide and GST. Write and erase can be performed by applying optical signals. (b) Transmission change for the amorphous and crystalline state. [57], [58]. Permission: https://creativecommons.org/licenses/by/4.0/.

TABLE 3. Advantages and disadvantages of OPCMs compared to EPCMs.

Advantages	Disadvantages
Low latency [18], [36], [55]	Need for electro-optic units [5]
Low energy consumption [55]	New read and write policies [5]
Higher MLC capacity [56]	Need for silicon photonic links [5]
Higher bandwidth [53]	Optical loss and crosstalk [13]
—	Sensitive to thermal variations [5], [36]

Moreover, we present a comprehensive review of different designs to implement single-bit and multi-bit OPCM cells and a comprehensive review of plasmonics-based OPCM cell's performance.

When it comes to integrating PCMs with state-of-the-art photonic integrated devices and circuits, the substrate material is very important as it will directly impact the system performance in terms of speed, energy efficiency, and footprint. Over the past few years, Si_3N_4 has been the preferred substrate to be integrated with PCMs due to its lower thermal conductivity ($\approx$43 $W.m^{-1}.K^{-1}$ [59]) compared to silicon ($\approx$148 $W.m^{-1}.K^{-1}$ [59]). Accordingly, the minimum energy required to trigger a nonvolatile amorphization is lower when using Si_3N_4 (e.g., 42 pJ) compared to silicon-based GST (e.g., 388.4 pJ) [59]. This makes the Si_3N_4 platform much more energy efficient compared to silicon platforms for PCM integration. However, silicon could offer other advantages over Si_3N_4 such as a smaller footprint, enhanced mode confinement, higher speed, and better integration with CMOS integrated circuits.

The work in [59] presented a detailed experimental analysis of the performance of silicon and silicon-nitride-based OPCMs. It was shown that integrating GST on top of a Si_3N4 waveguide leads to a propagation loss of 0.079–2.470 dB/μm, which is higher than silicon-based GST cells at 0.059–1.445 dB/μm in the C-band. The reason for the lower propagation loss in silicon-based OPCMs can be explained via refractive index contrast between silicon and GST. The refractive index contrast between silicon and GST is smaller than the refractive index contrast between silicon nitride and GST. This leads to lower scattering loss and reflections, and hence better matching of the optical mode in the underlying waveguide and GST. Therefore, a lower propagation loss is observed. The large refractive index contrast between silicon and the upper cladding of the waveguide (the air was considered as upper cladding in [59]) is another reason for the lower propagation loss of silicon-based OPCMs compared to those based on silicon nitride. The large contrast in the refractive index of silicon and air leads to better confinement of optical modes in silicon-based waveguide. Therefore, waveguides with smaller widths (e.g., 500 nm compared to 1.3 μm for silicon nitride [59]) will be needed so that the confined light in the waveguide can interact with GST. This reduces the evanescent coupling of the light to the GST, resulting in a lower propagation loss in silicon-based OPCMs compared to those based on silicon nitride [59].

In [59], it was shown that using silicon platforms can lead to a more compact footprint, higher energy consumption, and reduced amorphization time. Silicon compatibility with CMOS foundries makes it the preferred platform for Telecom, Datacom, data processing, and in-memory computing applications. On the other hand, silicon nitride is the preferred platform for photonic memories due to its lower thermal conductivity and hence higher energy efficiency. Higher thermal conductivity of silicon results in higher power dissipation to achieve the needed transmission contrast due to the presence of PCM, and this leads to the lower energy efficiency of silicon platforms compared to silicon nitride.

State-of-the-art reconfigurable SiPh integrated circuits operate based on the thermo-optic or free-carrier-dispersion effect of silicon. Such devices suffer from multiple limitations such as a large footprint (e.g., >100 μm) and high power consumption (e.g., >1 mW) [60]. This is one of the main motivations for using PCMs in SiPh integrated circuits. Regarding the choice of PCMs, among the different options we introduced in the previous section, GST is the most popular one to be integrated with silicon-on-insulator (SOI) and silicon nitride photonic devices. The reason for this is the high optical contrast between two amorphous and crystalline states in GST and the stability of crystallographic phases over time compared to other options [60]. Apart from GST,

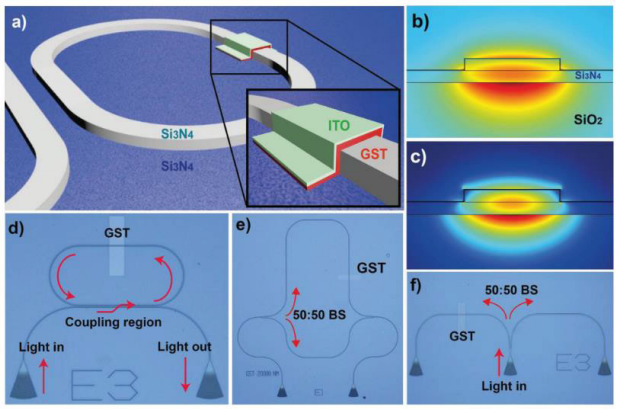

FIGURE 4. Different designs for photonic memory storage cells: a) Using partially etched MRRs. (b),(c) Simulated optical modes using COMSOL Multiphysics for a waveguide with GST on top in amorphous and crystalline state, respectively. (d),(e),(f) Fabricated storage cells with MRRs, MZIs, and beam splitters, respectively [62]. Permission: https://creativecommons.org/licenses/by/4.0/.

Ge-Sb-Se-Te alloys (GSST) are another type of PCMs with great promise to be integrated with photonic devices. GSST offers enhanced thermal conductivity (see Table 1) and lower optical power loss compared to GST. Optical loss is a parameter that lower the optical signal amplitude from the input to the output of a photonic device. Optical power loss is one of the main factors that limits the scalability of silicon photonic integrated circuits. GSST also shows better lifetime and thermal stability compared to GST [61].

Considering integrating GST with silicon nitride platforms to implement OPCM cells, the work in [53] proposed a design based on integrating a GST thin film with a length of 5 μm and a thickness of 10 nm with a silicon nitride ridge waveguide (see Fig. 3). This design is able to store a logic bit "0" or "1" depending on the state of the GST on top of the Si_3N_4 ridge waveguide. When the amorphous GST turned into the crystalline state upon exposure to an optical signal, the transmission of the GST changes by about 21%, which corresponds to logic bit "0" (erase procedure). This is achieved by applying intense laser pulses for a duration of 100 ns with a total energy of 533 pJ. Since the crystalline GST absorbs almost 80% of the input power, 430 pJ energy is needed to trigger the phase transition from crystalline to amorphous state. The reason for a lower energy requirement to change from the crystalline to amorphous state is the higher absorption coefficient (or higher extinction coefficient as shown in Figs. 2(c) and 2(d)) of GST in the crystalline state compared to that in the amorphous state. It was also demonstrated in [53] that the optical transmission contrast can be increased by increasing the length of the GST. The PCM-based photonic memory cell that was proposed in [53] is able to store only a single bit (either a "0" or a "1"). This puts additional limitations on the scalability and power consumption of photonic memory arrays build using such a cell to store more than one bit per cell based on this design. Leveraging the single storage cell proposed in [53], multiple optical storage cell structures can be designed using passive silicon photonic devices, such as those based on beam splitters, Mach–Zehnder interferometers (MZIs), and microring resonators (MRRs). Some of these example designs for a single optical storage cell are depicted in Fig. 4.

The work in [62] performed a detailed analysis of the performance of different photonic cells demonstrated in Fig. 4 with different geometries for broadband photonic applications. In this work, performance optimization of the cells was performed by altering the PCM cell geometry. It was shown for the race-track MRRs in Fig. 4(a) that different optical parameters, such as quality (Q)-factor, extinction ratio, and resonant wavelength, can be used to read the GST state because of the significant contrast between their values for the amorphous and crystalline state. For instance, it was shown that there can exist a significant difference in the Q-factor when the phase of the PCM (GST was used in [62]) changes from the amorphous to crystalline state. In addition, it was shown that the contrast between Q-factor of a single cell increases as the width of the GST cell increases. Using a single-cell OPCM, the work in [63] showcased how a single MRR-based OPCM cell can be scaled to 256 cells by cascading them to obtain an OPCM-based architecture with 512-bit capacity. The proposed architecture was also experimentally tested to store a small digital image. In this design, each OPCM cell is able to store only two bits. An optical pulse was used with a total energy of 890 pJ for amorphization of the GST in each cell, which makes this design extremely power-hungry as well as having high write latency. In addition, using this design in a photonic memory architecture leads to constraints on parallelism because of the lower MLC capacity (i.e., two bits per cell).

PCMs like GST show better optical transmission contrast in certain wavelength bands. This can be observed by considering the refractive index and extinction coefficient in PCMs depicted for different wavelengths in Fig. 2. As a result, having an OPCM cell design that can operate in a broad wavelength range is important. This is also helpful because of its effect on the scalability and energy efficiency of the OPCMs. Having OPCMs working with a broader wavelength range enables using a larger number of bit-lines to address, read, and write cells [5]. But realizing OPCMs working with a broader wavelength range is challenging because of PCMs' refractive index profile. Taking GST as an example, from Fig. 2(c), we can see that the change in the refractive index and extinction coefficient is significant under a wide wavelength range (e.g., 800–1600 nm in Fig. 2(c)). This will prevent having stable transmission levels over a wide range of wavelengths and can lead to a reduction in OPCMs' MLC capacity and variation in the transmission level of the cell over time.

The work in [61] showed that by using a PCM based on GSST ($Ge_2Sb_2Se_4Te_1$) one can achieve a 2-bit nonvolatile photonic storage cell to work with a broader wavelength range (1–18.5 μm) and with enhanced crystallization ability. GSST can be also exploited to tackle problems related to the variations in the optical properties of GST caused by thermal

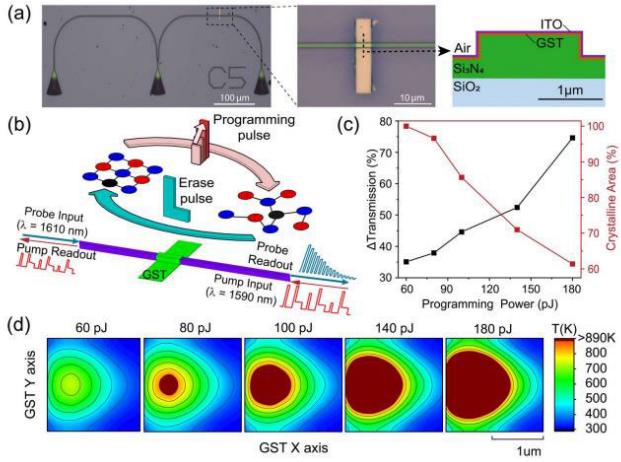

FIGURE 5. (a) Fabricated photonic memory storage cell. (b) Programming and erasing scheme of the cell in C-band and L-band. (c) Change in crystalline area of the cell and therefore transmission against the pulse energy. (d) Finite element modelling (FEM) simulation of the sample to solve the heat transfer equations in GST based on the input energy of the pulse. The dark regions have amorphous state [12]. Permission: https://creativecommons.org/licenses/by/4.0/.

variations in photonic applications [36] because of having a lower thermo-optic coefficient and being less susceptible to thermal variations, which results in having higher thermal stability. In [64], it was shown how using GSST instead of GST in MZI- and directional couplers (DC)-based photonic switches can enhance the insertion loss and crosstalk noise. For a single switching element using GSST, an insertion loss of 0.04–0.4 dB and crosstalk of −32 dB were obtained [64].

The attenuation coefficient is a parameter that can be used to analyze the switching dynamics of PCMs. The attenuation coefficient can be defined as the amount of optical power being absorbed by a PCM per unit length. The work in [65] developed analytical models to model the attenuation coefficient due to absorption of GST in the amorphous and crystalline state. Having such a model helps analyze and optimize the switching dynamics of GST for photonic switching networks and data storage applications. Leveraging such models, [65] aimed at optimizing different parameters such as thickness, width, and length of GST cells for fast and energy-efficient multilevel switching of optical data storage units and photonic switching networks. It was shown that as the width of the GST sample increases, the absorbed power in GST will increase and the input optical power will be attenuated evanescently along the length of GST.

As discussed before, PCMs can take amorphous state, crystallised state, or amorphous/crystalline (intermediate) state. Recall that by controlling the crystallization fraction of a PCM used in a phase-change memory cell, we can realize multilevel photonic memory data storage cells [11], [12]. Such a behavior is shown in Fig. 5 where the crystalline fraction of the PCM can be controlled through the input optical signal energy. From Fig. 5, we can see that for the given 2-μm-long GST sample, 180 pJ is needed to induce a 60% change in the crystallization fraction. Note that the initial state of the GST sample in this work was the crystalline state. The crystallization fraction of PCMs can be controlled by pulse amplitude modulation (PAM) or pulse width modulation (PWM).

The work in [12] experimentally realized up to a 5-bit OPCM cell by controlling the crystallization fraction which leads to obtaining up to 32 different transmission levels. A 50-ns laser pulse was used with variable amplitude (depending on the number of the bits) to program the cell as well as a 50-ns high amplitude laser pulse followed by a 200-ns low amplitude laser pulse to erase the cell. We can observe from Fig. 5 that programming the cell—which implies the phase transition of crystalline to amorphous—takes multiple pulses with the same duration but different power. In addition, [12] proposed a novel double-step pulse controlling for phase-change memory cells as well as a detailed analysis of pulse parameters on the multilevel cell dynamics.

Plasmonic devices are a category of photonic devices which deal with the interaction of free electrons (metals) and an electromagnetic wave, like light. Upon interaction with incident light, the free electrons in the metals start oscillating. The oscillation of electrons, which is called the plasmonic effect, can be modeled via the Drude model and it is called surface plasmon [66]. The latency and energy efficiency of a single phase-change memory cell can even be further enhanced by improving the PCM-based photonic memory cell's design. The work in [67] presented a novel method to enhance the switching capability of a GST cell in terms of latency and energy efficiency for photonic memories. In particular, it was shown that integrating the GST cell with two sub-micron nanoantennas (made with silver) can significantly enhance the light-matter interaction between SiN waveguide and GST through the plasmonic effect. Therefore, this leads to write/erase speed of 2–20 ns and write/erase energies of 2–15 pJ, which is about 2 orders of magnitude improved compared to contemporary multilevel GST cells for photonic memories.

As another example of exploiting the plasmonic effect to enhance the light-matter interaction in OPCM cells, the work in [68] proposed an all-optical OPCM cell using the plasmonic effect. It was shown that by integrating silver nanostructures with GST, the performance of an MRR-based OPCM cell in terms of insertion loss, optical transmission contrast, and area consumption can be significantly improved. Thus, higher number of bits can be stored in a single OPCM cell with lower area consumption and latency, which makes the memory more scalable and energy efficient. The schematic of the design is shown in Fig. 6. As it can be seen from the figure, the design consists of an MRR-based OPCM in which the GST is surrounded with silver nanostructures that lead to enhancement in the GST-light interaction through the plasmonic effect. Three different designs based on silver/GST fabrication were investigated. In the first design, the silver/GST structure was fabricated on top of the silicon-nitride waveguide and is called the non-embedded design (see Fig. 6 (b)). The second design includes fabricating the silver/GST structure halfway inside the silicon-nitride

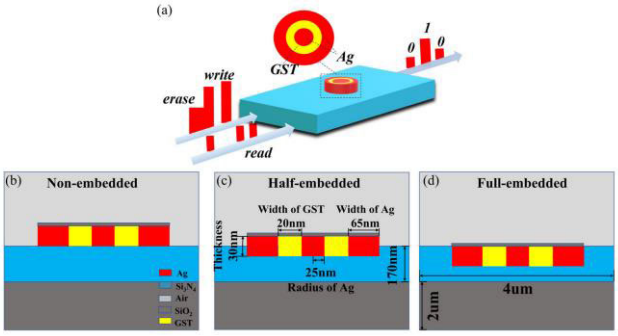

FIGURE 6. (a) Plasmonically enhanced all-optical MRR-based OPCM. (b) The silver/GST structure fabricated above a silicon-nitride waveguide. (c) The silver/GST structure fabricated halfway in a silicon-nitride waveguide. (d) The silver/GST structure fabricated in a silicon-nitride waveguide [68]. Permission: https://www.mdpi.com/openaccess.

waveguide and is called the half-embedded design (see Fig. 6 (c)). In the last design, the silver/GST structure was fabricated inside the silicon-nitride waveguide and is called the full-embedded design (see Fig. 6 (d)). The experiments in [68] showed 13.7% optical contrast between the amorphous and crystalline state when the silver/GST structure is fabricated above the silicon-nitride waveguide (the non-embedded design). This was significantly higher than the other two cases: 9.6% for the half-embedded and 6.1% for the full-embedded design. In addition, for the non-embedded case, a maximum insertion loss of 2.3 dB and a minimum insertion loss of 1 dB per cell was reported for the GST in the amorphous and crystalline state, respectively. The overall insertion loss was higher for the other two design cases. Finally, [68] showed that their design can gain from a more compact footprint per OPCM cell with dimensions of $50 \times 90\,nm^2$, which is significantly smaller compared to traditional OPCM cells.

C. OPCM ARCHITECTURES

As the size and complexity of data-driven applications increase, memories with a higher cell density, lower power consumption, and higher bandwidth are required to carry out computationally intensive operations. The work in [69] focused on simply replacing the electrical links with silicon photonic links without redesigning the memory architecture to enhance the latency of EPCMs. The approach requires multiple electro-optical (E-O) and opto-electrical (O-E) conversions to convert the electrical signals to optical signals and vice versa. As the number of O-E and E-O conversions increases, the energy efficiency in the memory architecture will decrease. Note that EPCM cells are being used in memory architectures because of their benefits in terms of scalability and thermal stability [46].

OPCMs can alleviate the scalability, power consumption, and bandwidth limitations of conventional memories, such as DRAMs. However, it is inefficient to simply exchange the EPCMs with OPCMs in the same architecture because the electrical signals coming from the memory controller cannot be directly employed to write, read, or program the OPCMs. Therefore, to adapt the OPCMs to state-of-the-art memory architectures, a complete redesign of the memory will be required to maintain the benefits of OPCMs. In particular, SiPh links integrated with photonic components [13], [70], [71], [72], [73] should be used to convert and communicate the data from electronic units (e.g., memory controller) to the OPCM-based main memory. This area is still evolving and researchers are trying to design energy-efficient and low-latency OPCM-based architectures for emerging computing systems.

The work in [5] presented a novel OPCM-based memory architecture called "COSMOS." In this work, to make the electronic part of the memory (i.e., the memory control unit) compatible with an array of OPCM cells to replace the DRAM, an electro-opto-electrical (E-O-E) unit is required. This unit has an essential role in converting the electrical signals from the memory control unit—such as row and column addresses, Read, Write, and Erase commands—to optical signals. The converted optical signals will be then transmitted through silicon photonic links to access the OPCM cells in the architecture. Fig. 7 shows the block diagram of the memory architecture designed in [5]. Each OPCM cell in the architecture can store 5-bit data using the design in [12]. The OPCM data storage cell in this design has a structure similar to the one proposed in [74], where silicon photonic MRRs are used to access the cells and different wavelengths address the cells in different row and column addresses. In [5], a detailed analysis was performed on the impact of different parameters related to OPCM cells, including the number of bits per cell (MLC capacity), number of silicon photonic links, and OPCM capacity on the overall performance of the memory.

The work in [5] showed that the execution time for a memory with 4-bit OPCM cells and 64 silicon photonic links is much lower compared to a memory with 2-bit EPCM cells and 64 electrical links, as well as higher read and write throughput and lower average latency. Regarding the effect of the MLC capacity, it was shown that as the MLC capacity of a single OPCM cell increases, the average memory (read and write) latency decreases by about 33%. This is because of the enhanced parallelism that an OPCM cell with a higher MLC capacity can offer. The energy-per-bit for read and write in [5] was reported to be, respectively, 243 and 44.5 pJ/bit for the EPCM, and to be 40.68 and 11.6 pJ/bit for the OPCM, showing a significant enhancement in the energy efficiency of the memory. The number of silicon photonic links and the average lifetime of the OPCM were explored in [5]. It was found that increasing the number of silicon photonic links from 64 to 256 can enhance the execution time of the memory by about 5 seconds. However, this comes at a cost of higher loss and crosstalk noise related to silicon photonic links. Increasing the MLC capacity from two to eight bits can also decrease the average lifetime from 16 years to six years. Finally, a detailed analysis was presented in [5] on the area consumption of OPCMs. The work reported a significant improvement in the area consumption of a 2 GB 3D stacked

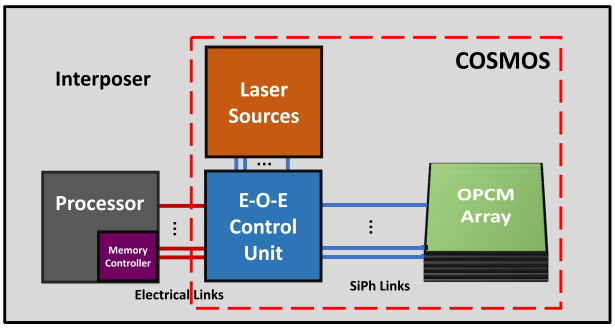

FIGURE 7. COSMOS Architecture [5].

8-bit OPCM (67.1 mm^2) compared to the equivalent DDR4 counterpart (224 mm^2).

D. PHASE CHANGE MATERIALS FOR PHOTONIC IN-MEMORY COMPUTING

With the increased complexity of deep learning algorithms and AI applications, there is a critical need for improving digital multiplier units in AI hardware accelerators. Indeed, matrix-vector multiplication, which is the core of every machine learning and deep learning model, is known to be the most time and energy-consuming operation in AI applications running on AI accelerators [75], [76]. Accordingly, the performance of electronic AI accelerators degrades as the complexity and the size of the models they run continue to grow. Emerging integrated photonic computing platforms have shown a great promise to perform multiplication and accumulation (MAC) operations with significantly lower latency and power consumption [75], [77], [78]. Because of using photons instead of electrons for data movement and computation, compared to conventional AI accelerators, photonic AI accelerators offer higher bandwidth and parallelism in the computation in addition to lower latency due to performing computations at light speed.

Several optical neural networks based on silicon photonic integrated circuits have been proposed, including coherent networks using MZIs [78], [79], [80], [81] and noncoherent networks using MRR banks [77], [82], [83], [84], [85], [86], [87], hence enhancing the hardware implementation of multiplication units with higher speed and lower computation energy consumption compared to electronic counterparts. Despite being beneficial compared to electronic accelerators, photonic AI accelerators suffer from inherent limitations, including optical loss and crosstalk noise [75], large footprint ($\approx$1000 μm for a deep neural network with two hidden layers), and sensitivity to thermal and process variations, which result in deterioration of the system's overall performance (e.g., drop in inferencing accuracy) as the network scales up [88], [89], [90], and [91].

PCMs can be integrated with photonic AI accelerators to address some of the limitations of photonic accelerators, such as large footprint and accumulated optical losses. Some of the state-of-the-art applications of PCMs in the implementation of photonic tensor cores will be discussed in Section IV.

In addition to using PCMs for photonic computing, recent work has shown that phase-change memories can be also used as part of in-memory computing units [92], [93], [94], [95]. Photonic computing units based on PCMs are beneficial due to lower static power consumption and smaller footprint [96]. The reason for this is the elimination of the bulky phase shifters in the photonic computing units (e.g. MZIs), and replacing them with smaller PCM cells that can be driven with an optical signal and without additional applied biasing to maintain the PCM state [97]. However, in data-driven applications, most of the power in the system is consumed not in the computing units but during the data transfer between processing units and the main memory due to the separation of the memory unit and processing units in Von Neumann architectures [24], [98]. This challenge still remains and it deteriorates the system's overall performance as the size and complexity of applications increase. This is one of the main motivations for using OPCMs for both computation and data storage, and this paradigm is called photonic in-memory computing [99].

The work in [100] and [101] showed that a single multilevel GST cell, which can be used as a phase-change memory, is able to perform a simple scalar multiplication. The design principles for implementing a simple PCM-based photonic multiplier are shown in Fig. 8. Based on the proposed design, a single scalar-scalar multiplication can be performed through the transmission level of the GST cell. The transmission level of the GST cell can be changed by changing the crystalline area of the GST similar to what we have seen in multilevel photonic memory cells [12]. Manipulation of the crystalline area of the GST in this design can be done through the modulation of the input optical signal's power and duration. Depending on the crystalline area of the GST cell, its transmission level, which represents the intended scalar value, varies. The GST's transmission level can act as a scalar that is multiplied by the input optical signal and propagates to the output of the cell. Note that the input optical signal to read the data from a cell must have lower energy than the programming signal that is used to set the cell to prevent a change in the transmission level of the GST.

The work in [102] presented a design for an in-memory photonic computing unit based on SOI platform integrating PCMs (i.e., GST). The schematic of this design is depicted in Fig. 9 (b). It was shown that by using slot-ridge waveguides one may increase the dynamic range of the weights to be used for in-memory computation. The main difference of the design in [102] with the one demonstrated in [100] is the enhancement made in the interaction between the mode confined in the underlying waveguide and the PCM cell. It was shown that this design is capable of storing more multilevel weights, hence an increase in the energy efficiency of the in-memory photonic computing unit.

From Figs. 9(d) and 9(f), it can be seen that the interaction between the electric field of the confined mode in the waveguide and the GST is significantly enhanced for the slot-ridge waveguide, compared to the conventional ridge waveguide

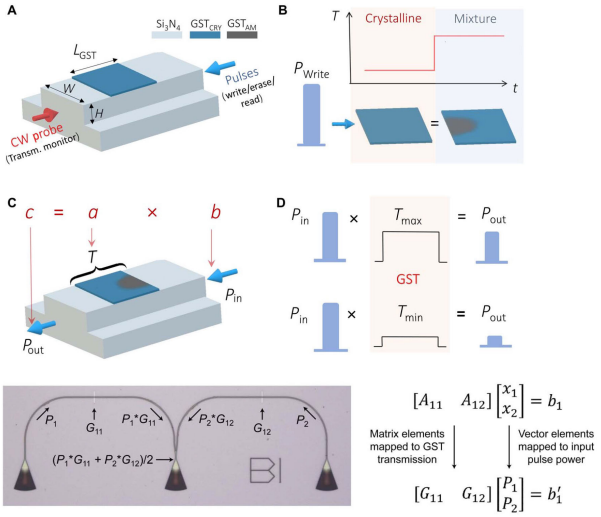

FIGURE 8. a) Scheme of reading and programming pulse of the GST as well as its geometry. b) Write pulse amorphousize some portion of the crystalline GST, leading to higher transmission levels. c) A simple scalar multiplication. d) Readout scheme with a P_{in} pulse which is unable to induce phase transition in GST because of its lower energy and duration compared to the write pulse. e) Sample of the fabricated device to perform a simple matrix-vector multiplication [100]. Permission: https://creativecommons.org/licenses/by/4.0/.

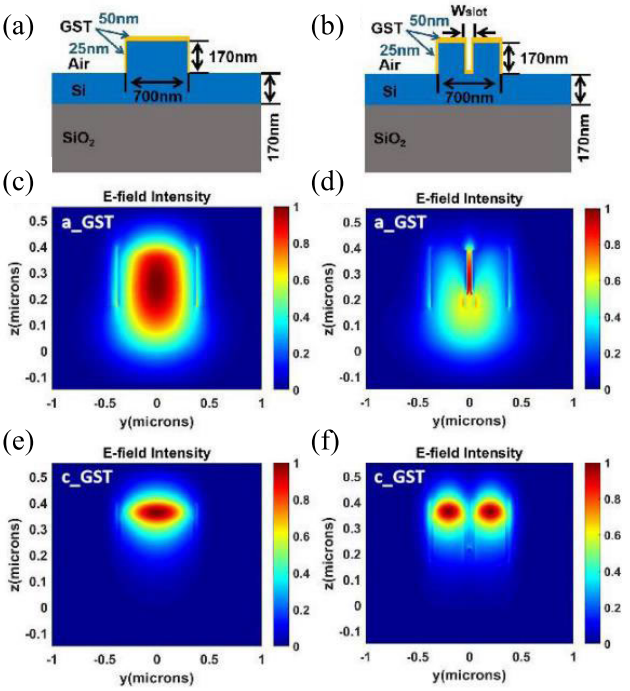

FIGURE 9. Design comparison of an in-memory photonic computing unit based on phase-change materials (GST): (a) The design presented in [100]. (b) The design presented in [102]. (c) Electric field profile for GST-ridge waveguide design when GST is in the amorphous state. (d) Electric field profile for GST-slot ridge waveguide design when GST is in the amorphous state. (e) Electric field profile for GST-ridge waveguide design when GST is in the crystalline state. (f) Electric field profile for GST-slot ridge waveguide design when GST is in the crystalline state. Permission: https://creativecommons.org/licenses/by/4.0/.

integrated with GST proposed in [100]. In addition, the optical transmission change in the slot-ridge design is increased significantly compared to the ridge design because of the enhanced interaction of the electric field and GST (see Figs. 9(a) and 9(b)). The change in the optical transmission level is an important parameter due to its crucial role in determining the MLC capacity of the OPCM cell. A higher dynamic range of the change in the optical transmission level of a single cell allows designers to store a higher number of bits per OPCM cell. The dynamic range of the optical transmission level in slot-ridge design can be even further enhanced by increasing the width of the slot. The designated design based on slot-ridge waveguides was tested by implementing a three-layer perceptron to perform a recognition task on MNIST handwritten digit dataset. An accuracy of 90.7% was achieved which was 2.6% higher than the conventional-ridge-waveguide design.

OPCM cells based on MRRs can also be used as a promising alternative for ridge-waveguide-based OPCM cells to implement photonic in-memory computing units. The work in [103] proposed a design in which GST was integrated into MRRs to implement an in-memory computing unit for spiking neural networks. By this design, the need for off-chip DRAM access to load the weights related to the implemented trained deep neural network using photonic tensor cores was eliminated. The configurability challenge for this design was also addressed by adding a bent waveguide to each synapse. The added bent waveguide can be used as the write port on the MRR-based phase-change memory cells for each synapse. In addition, the width of the write port was much smaller than the one related to MRRs. The reasoning behind such a design is to achieve an asymmetric design to have maximum light confinement in MRRs and less confinement in the write port to avoid any interference pattern. Using this writing scheme on the MRR-based OPCM cells made the design reconfigurable. This is becasue of the low error in the transmission in the presence of the write bent waveguide (i.e., ≈0.5% for a separation of 300 nm between the write bent waveguide and the ring), in addition to high coupling between the bent waveguide and the ring (i.e., ≈70% for the same separation). This made efficient writing on the MRR-based OPCM cell possible. The design in [103] was tested in the implementation of a PCM-based in-memory photonic computing unit trained on the MNIST dataset. The inferencing accuracy of 97.84% was achieved, which was really close to the inferencing accuracy of the ideal spiking neural networks at 98.34%.

Broadcast and weight is a protocol which was introduced initially in [77] to implement neuromorphic photonic processors. The broadcast-and-weight protocol uses wavelength-division multiplexing (WDM) to carry out computation in the photonic domain by using reconfigurable, continuous-valued filters called MRR banks to weigh the optical signals. Considering the design in [100], the work in [104] proposed Starlight, featuring a GST cell to exploit in-memory computing to enhance the parallelism in computation and using MRR-bank architectures in the

noncoherent photonic neural network that can be updated by using mode-wavelength division multiplexing. Starlight design showed lower power consumption and crosstalk noise compared to conventional broadcast-and-weight architectures [77], [82]. In particular, Starlight design showed an insertion loss of 0.05–0.1 dB and crosstalk noise of −50 to −30 dB for resonant and non-resonant state. The structure of a single dot-product engine that is used in Starlight is shown in Fig. 10. We can see that each kernel weight element can be translated into an optical transmission level of the GST using a write laser pulse to achieve a specific crystallization area. Programming the GST cells based on the kernel weights in Starlight was performed offline after the training of the network, as a one-time procedure. In addition, Starlight design showed that using hybrid mode-wavelength division multiplexing eliminates the need for high number of wavelengths to perform acceleration in addition to increased parallelism in the photonic in-memory computation using GST cells.

The Starlight architecture is illustrated in Fig. 11. We can see that by using multiple modes and GST-based in-memory computing units to perform matrix-vector multiplication, the number of wavelengths—and hence the number of the laser sources—can be decreased and this leads to enhanced parallelism in computation. In addition, this design strategy makes Starlight much more energy-efficient compared to conventional broadcast-and-weight architectures to carry out AI acceleration tasks [77]. In terms of power and area overhead of Starlight architecture, it was shown that using four TE modes and four wavelengths per mode ($4 \times 4 \times 4$ photonic acceleration unit) leads to a chip area of less than 0.4 mm^2 and consumes 0.078 W of power, which is lower than conventional noncoherent broadcast-and-weight architectures, such as DEAP [105] with a power consumption of 1.404 W. Eventually a $4 \times 4 \times 4$ Starlight design was tested on Iris classification dataset and it achieved the inferencing accuracy of 96%, which was consistent with the accuracy that was obtained during the training process.

Although embedding photonic tensor cores with PCM-based in-memory computing cells shows a promising prospect for photonic in-memory computing paradigm, two key bottlenecks of restricted bit-width and write endurance of the PCM-based photonic computing cells limit their performance. The size of the in-memory photonic computing units grows with the increase in the size of the designated data-driven applications. This necessitates numerous weight writes on cells inside the computing unit. Therefore, reduction of the lifetime and the MAC unit's accuracy is inevitable. Aging of the cells over the long run leads to the degradation of obtainable transmission ranges, and consequently, the accuracy can drop severely. The work in [54] showed that with only 30% aged cells in a photonic tensor core, the accuracy of the multiplication decreases by 35%. To alleviate this critical issue, an aging-aware optimization methodology for PCM-based in-memory photonic tensor cores, called "Elight," was presented in [54]. The work in [54] also described a write-aware training process for AI applications that reduces the number of write operations (by roughly 20 times), which is the primary cause of aging. In addition, a post-training optimization procedure is provided to further reduce the number of writing operations.

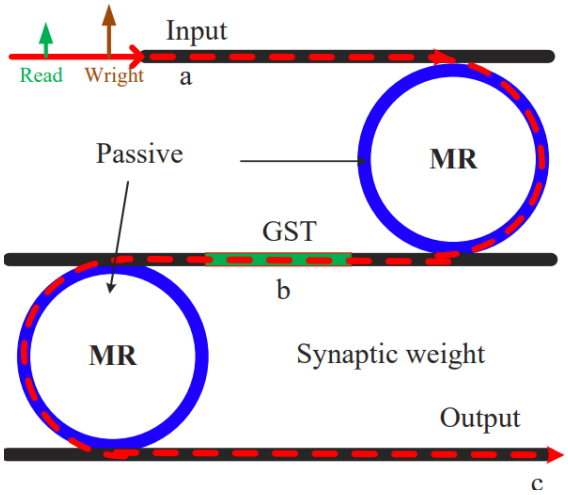

FIGURE 10. Starlight dot product engine using MRRs and integrated GST [104]. Permission: https://creativecommons.org/licenses/by/4.0/.

E. SIMULATION OF OPCMs

A simulation algorithm is of essence to start from the device and material level to system level to simulate the OPCM cells and optimize them according to the given design goals. In this part of our survey, we briefly discuss the simulation procedure of PCM-based photonic devices. The simulation of a PCM itself is nontrivial because of the need for multidomain simulations, including molecular, optical (electrical), and thermodynamic (heat) simulations. In addition, most of the research efforts that were presented so far are dealing with a single-cell analysis. As an example, the work in [22] indicated that for a top-illuminated sample of GST with the thickness of 80 nm and length of 20 μm, a laser pulse with a power of 3–5 mW and duration of 50–600 ns is required to obtain a fully crystalline state. The work in [56] also showed that to obtain 18% change in the transmission of a 10-nm-thick and 2-μm-long GST, about 650 pJ energy with a laser pulse with a power of 2.3 mW is needed. This implies that the laser pulse duration should be roughly 282.60 ns for a single write cycle. In the same work, it was shown that as the thickness of the GST cell increases, due to its higher optical absorption, lower energies will be needed at the input to trigger the same transition for a single write cycle. Suppose that we use 256 of such cells in an OPCM-based architecture to replace DRAMs [5]; this implies that significant optical power will be needed to address and control these cells. The required optical power can be decreased at a cost of increased write latency.

The work in [22] proposed such a platform and a simulation algorithm written in MATLAB, which is available publicly [106]. Nevertheless, the proposed simulation platform

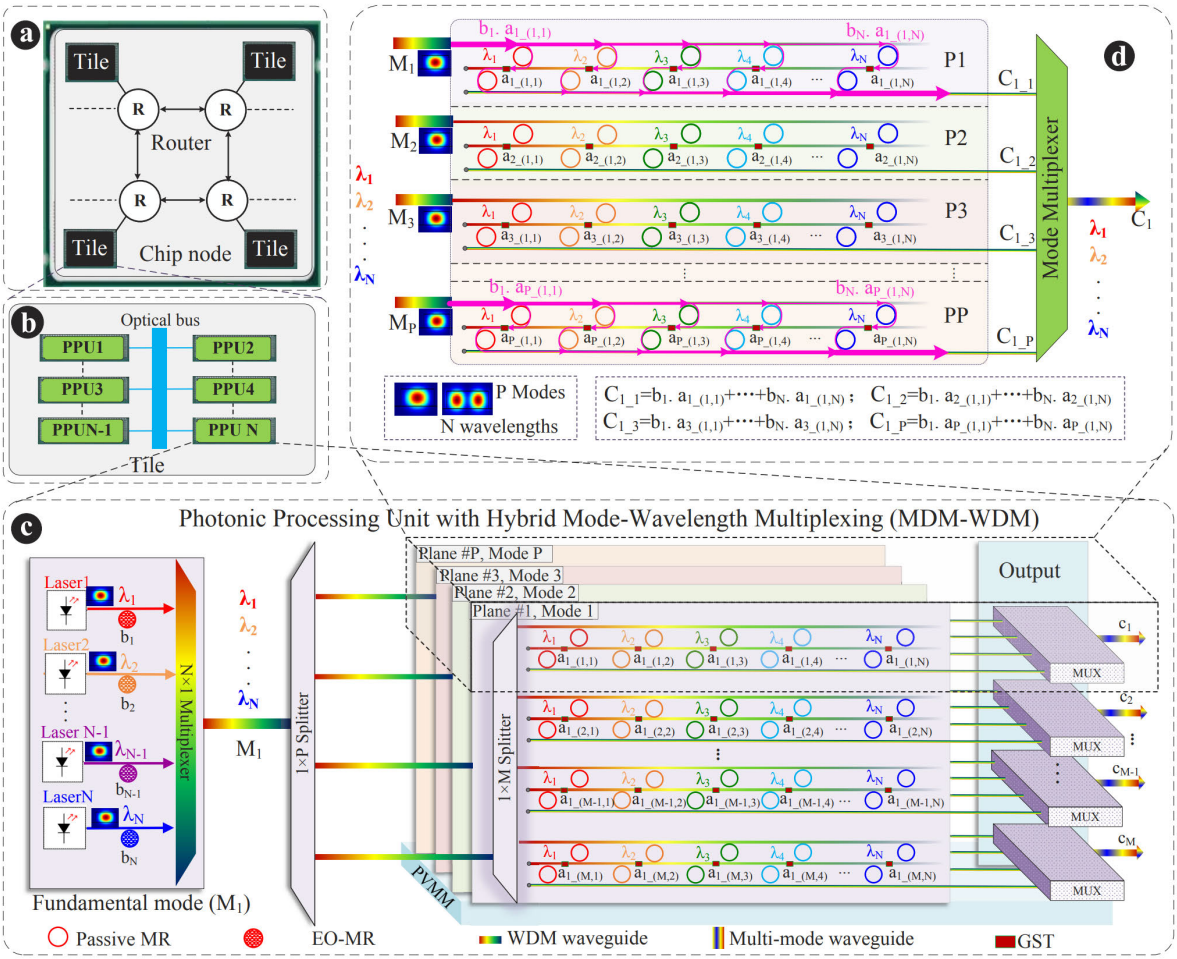

FIGURE 11. Starlight AI accelerator architecture. a) The architecture of the tiles in the processor. b) Architecture of each tile using multiple photonic accelerator units. c) Architecture of each photonic accelerator unit using hybrid mode- and wavelength-division multiplexing to perform acceleration in parallel. d) Architecture of each photonic acceleration unit using a single mode and multiple wavelengths to perform the matrix-vector multiplication [104]. Permission: https://creativecommons.org/licenses/by/4.0/.

has two major drawbacks: 1) it is 2D, and 2) the device is top illuminated instead of using a Si_3N_4-based ridge waveguide, similar to what is proposed in [11], [53], and [100]. The simulated results were verified using experimental results. The simulation steps performed in [22] are depicted in Fig. 12. As it can be seen from Fig. 12, the simulation starts with illuminating the GST sample with a laser pulse with specific duration and power. The input optical pulse will be partially absorbed by the sample and converted to heat, leading to temperature fluctuations in the sample. The heat transfer equation must be solved using numerical approaches, such as finite-element modeling (FEM), to obtain the temperature distribution at each time step. Based on the temperature distribution, nucleation and growth rates can be calculated. By using Cellular Automata–Nucleation and Growth model [22], the amorphous and crystalline regions can be modelled and their fractional distribution can be calculated. Eventually, from Lorenz and Fresnel equations, the transmission and reflection of the light can be calculated.

An overview of the results presented in [22] is shown in Fig. 13. Considering Fig. 13(b), the GST sample used in the simulations and experiments is top-illuminated via a laser pulse. For a constant laser duration, as the laser power increases, the diameter of the crystalline area increases. This causes an increase in the crystalline fraction of the sample, and hence a change in the optical reflectivity and transmissivity of the GST sample. As another experiment, the work in [22] suggested that the reflectivity and crystalline fraction of the GST sample increase with increasing the laser pulse duration and keeping its power constant (5.7 mW in [22]). The aforementioned trend was expected because for a constant laser pulse and increased duration, the amount of absorbed energy over time increases, leading to triggering phase transition from amorphous to crystalline state in the GST.

The simulation of GST-based photonic memory cells can also be done with computer-aided design (CAD) simulation tools, like COMSOL Multiphysics. The simulation should be performed for each time step. The phase transition model of GST can be modelled through a highly optimized Cellular Automata–Nucleation and Growth model, as it was noted in [107], [108], [109], and [110]. Unfortunately, there

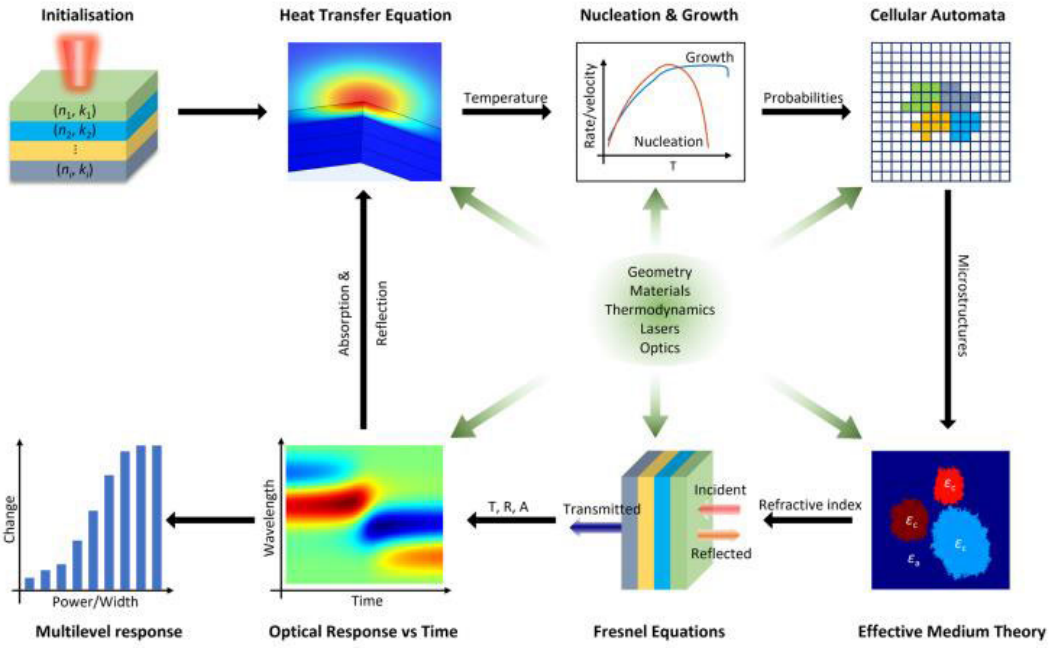

FIGURE 12. GST simulation steps demonstrated in [22]. Permission: https://creativecommons.org/licenses/by/4.0/.

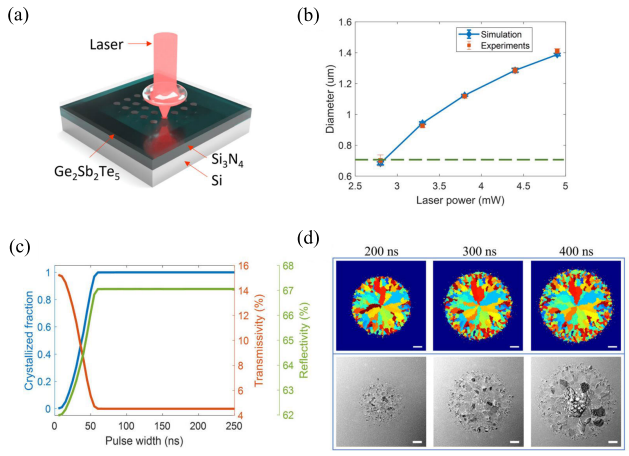

FIGURE 13. An overview of results presented in [22]. a) Schematic of the experimental testing unit used to verify the results. b) Verification of the simulation results by experimental results. Mean diameters of crystallised regions at different input laser powers. The dashed green line indicates the FWHM of the laser beam. c) Simulation results using a 5.4 mW laser pulse with different duration. d) Comparison of simulation and experimental results, The colorful grains are GST in crystalline state and the blue region is the GST in amorphous state. Permission: https://creativecommons.org/licenses/by/4.0/.

is no CAD simulation tool that can perform the Cellular Automata–Nucleation and Growth simulation due to its complexity and novel nature. Thus, it should be hard-coded and integrated into other multiphysics tools, such as COMSOL Multiphysics, similar to what was proposed in [56]. The work in [56] used the RF tool of COMSOL Multiphysics integrated to its HEAT TRANSFER tool to obtain the temperature distribution at each time step for a given geometry. Then, the output temperature distribution can be used by a hard-coded Cellular Automata–Nucleation and Growth code to obtain growth and nucleation rates precisely. This procedure can be repeated until the simulation time is finished. The simulation time to reach the convergence can vary from a couple of minutes to hours depending on the simulation parameters, such as the mesh accuracy, thickness, width, and length of the cell and duration of the laser pulse.

IV. OPEN CHALLENGES AND OPPORTUNITIES

In this section, we discuss some open device- and system-level challenges and requirements that should be considered when designing phase-change memories and PCM-based devices and architectures.

A. POWER-LATENCY TRADE-OFF

The energy that is needed for setting or resetting OPCM cells depends on the PCM's geometry and the pulse peak power and its duration. As a PCM sample becomes bulkier and thicker, the absorption enhances, thus phase change can be triggered faster. However, a PCM sample cannot be thinner than 2 nm, because for an extremely thin PCM, the PCM loses its dynamic phase-change properties [10]. The energy of an optical pulse can be approximated by multiplying the pulse duration with its peak power. As the peak power reduces, the pulse duration must increase to provide enough energy to trigger a single set or reset routine via phase transition of the PCM. Typically, using optical pulses with low peak power and low duration is desired for PCM-based memory architectures. With an increase in the pulse duration and the number of OPCM cells, the average latency of the entire system will increase, and this leads to the deterioration of the memory throughput.

Increasing the peak power will cause additional heating to the nearby devices, affecting the performance of nearby

TABLE 4. Different features of NVM technology [5], [12], [49], [53], [111], [112]. (F: feature size of the lithography).

Parameter	EPCM	ReRAM	OPCM
Cell size	$\approx$ 4–12 F^2	$\approx$ 4–12 F^2	$\approx 500\,nm \times 500$ nm
Write energy (J/bit)	$\approx$ 10 pJ	$\approx$ 0.1 pJ	60–130 pJ
Write latency (ns)	150–1000 ns	50 ns	25 ns
Read latency (ns)	50–80 ns	10 ns	25 ns
Write endurance	1e8	1e11	1e7
Retention	>10y	>10y	6–16y (depending on MLC capacity)
MLC	YES	NO	YES
3D integration	YES	YES	YES

photonic devices due to the thermo-optic effect and thermal crosstalk. Increasing the peak power also results in an increase in the total power consumption of the memory system, making the system power inefficient. Therefore, optimizing the geometry of a single cell as well as that of a memory array architecture is of great importance. In addition to the optimized geometry, using a hybrid OPCM cell can help reduce the programming energy. The work in [45] suggested that using a single layer graphene (SLG) heater in the structure of the OPCM can lead to a significant 20-fold reduction (8.7 ± 1.7 aJnm^3) in the OPCM cell programming energy density, compared to the state-of-the-art OPCM cell designs. The phase switching of the GST in the OPCM cell presented in [45] was triggered electrically by the application of a bias voltage using two gold contacts.

Because of the nonvolatile nature of PCMs, OPCM arrays offer zero static power to maintain the transmission level of the PCM cells when being used as a photonic main memory or in-memory photonic computing unit [104]. Nevertheless, to the best of our knowledge, the power-latency trade-off in OPCM-based memory systems has not been discussed in any prior work. Yet, the outlook of this paradigm can be predicted by comparing state-of-the-art NVMs (e.g., EPCMs) with DRAMs, as similar challenges may exist when using OPCMs as the main memory or in-memory computing unit. Using OPCMs for memory systems can increase the power overhead and latency of the system. The work in [5] suggested using SiPh links for communication between the memory controller and OPCM-based memory. However, using a SiPh link for such short-distance communication is energy inefficient, and requires multiple electro-optical and opto-electrical conversions per cycle [5]. This will lead to added latency and power consumption because of the limits of laser sources' wall-plug efficiency and the overhead of electro-optical/opto-electrical converters (see Fig. 7). Table 4 shows some of the key features related to the state-of-the-art NVMs. We can see from the table that in many aspects, like write energy and latency, write endurance and read latency, the performance of state-of-the-art EPCMs is even worse than ReRAMs and DRAMS. However, they offer better data retention, higher scalability, and MLC [12], [49], [111], [112]. The aforementioned limitations related to EPCMs are the main motivation for using OPCMs in future memory and computing systems. Based on the information in Table 4, any future OPCM-based memory architecture must have enhanced latency, endurance, and energy efficiency compared to those based on EPCMs.

B. ENDURANCE

The results presented in [5] show that as we increase the MLC capacity of a single OPCM cell, the average lifetime of the single OPCM cell, and hence the whole memory, decreases significantly. The writing procedure is the most critical procedure that affects the lifetime of OPCM cells. This is the main reason that in many implementations, a train of pulses is being used to write on a single OPCM cell. There is a trade-off between the average lifetime and MLC capacity of a cell. As we increase the MLC capacity, the OPCMs can be more scalable with a higher capacity, but this comes at a cost of reduced endurance. Optimization approaches were proposed to reduce the write procedures when a GST cell is being used as an in-memory computing unit. In particular, the work in [54] showed such optimization by performing a write-aware training to reduce the number of unnecessary writes when updating the weights during the training. The same work also showed a post-training optimization approach based on block-matching-based training and column-based reordering to reduce the number of redundant writes—with a negligible effect on the model's output accuracy—to increase the endurance of PCM-based photonic tensor cores [54].

C. AGING AND TRANSMISSION AND RESISTANCE DRIFT

Utilizing the MLC property of phase-change memories requires the different states in the PCMs to be well separated over time. Variation of the phase change material's state over time leads to instability in resistance and transmission. This phenomenon is called optical- and resistance-level drift and it is originated from thermal instability and optical band-gap widening of PCMs over time. The optical band-gap widening happens in PCMs in an amorphous state because of structural relaxation [113], [114] over time. This leads to a change in the optical transmission level in OPCM cells over time because of the physical nature of the drift in PCMs in the amorphous state. The instability in the state of the material level deteriorates even more over time because of aging of the cell. There are some work that tried to alleviate the resistance drift of the PCMs originating from the instability of the states. For example, the work in [115] proposed some physical-level strategies to decrease the resistance drift and increase the thermal stability of multilevel phase-change memory cells. The work in [115] related the resistance drift of the PCMs to the band-gap energy and sheet resistance of the material [116]. It was shown that this limitation can be alleviated via engineering the band gap, sheet resistance, and dielectric constant of the deposited phase change materials.

D. LOSS AND CROSSTALK NOISE

In some existing work for implementing OPCM cells, MRRs and waveguide crossings are exploited to construct, read, and write single photonic memory cell in a crossbar architecture [5], [53], [62]. Such devices suffer from coherent and noncoherent optical crosstalk noise, leading to misreading the memory in the read procedure, as well as changing

the transmission level when using higher MLC capacity for a single cell. Insertion loss can also lower a signal's amplitude used for reading multiple OPCM cells in an array of cells. These issues become even more critical when scaling memory arrays because of the accumulation in insertion loss and crosstalk noise power, leading to an increase in the number of misreads. Design optimization approaches must be used to deal with this issue to make OPCM-based memory architectures more scalable and resilient to optical loss and crosstalk noise [117], [118], [119], [120], [121].

Despite a wide range of applications of GST in constructing OPCM cells, this material shows a high insertion loss in photonic memory applications [61], especially when it is in the crystalline state due to its high extinction coefficient (see Fig. 2(c)). This limits the scalability of the architectures based on GST. One possible solution to address this issue is to use a new class of PCMs, called GSST. GSST, which has been studied for PCM-based photonic applications, shows superior performance in terms of thermal stability—through doping Se atoms and excess Ge atoms, which leads to an increase of the T_g [42], [122], [123]—and lower material loss contrast compared to GST (because of lower $\Delta\kappa$) [34], [122], [123]. The work in [21] suggested that different figures of merits (FOMs) of $\text{FOM}_1 = \Delta n/\Delta\kappa_a$ and $\text{FOM}_2 = \Delta n/\Delta\kappa_c$ can be used to quantify the performance of OPCMs. For memory purposes, a drastic change in the refractive index (Δn) upon the phase change in the OPCM cell is required. However, a large extinction coefficient change (κ) in the amorphous and crystalline state imposes excessive insertion loss to the OPCM cell due to material absorption (see II-D). The work in [21] showed that for GST, $\text{FOM}_1 = 109.72$, which is lower than that for GSST with $\text{FOM}_1 = 116.73$ at 1550 nm. This comparison can be interpreted as a higher refractive index and lower material loss that GSST in amorphous state offers compared to GST in the same state at 1550 nm. The same comparison can be made for crystalline state using FOM_2. We can see from [21] that for GSST, $\text{FOM}_2 = 4.17$, which again is higher than GST with $\text{FOM}_2 = 2.52$ at 1550 nm. Therefore, GSST applications to construct OPCMs can be expanded to obtain photonic memory arrays and computing units to alleviate the thermal instability and high material loss penalty in GST.

E. THERMAL SENSITIVITY

Thermal sensitivity is another major limitation to be considered, which can lead to transmission drift in a single cell. In [36], an analysis was carried out to model the thermo-optic coefficient in a PCM. An increase in the optical power dissipation in nearby optical components can be experienced by OPCM cells in the form of thermal variations (i.e., thermal crosstalk). Thermal variations may not trigger the phase transition but they can change the refractive index of the PCM in a particular state, leading to an increase in the number of misreads in OPCMs. The work in [36] presented analytical models for thermo-optic coefficient of GST. The presented models can be used to further optimize the performance of GST-based OPCM cells [34], [36]. In addition, the work in [124] presented an experimental study on the impact of temperature variation and transmission drift in OPCMs employed for in-memory computing units. The presented model in [124] can be used to optimize the performance of deep neural networks when they are being implemented using OPCM in-memory computing units.

F. FLICKER NOISE AND UNCERTAINTY OF THE INITIAL STATE

We learned that EPCMs can be good candidates to carry out analog in-memory computation for deep learning and AI applications. However, they suffer from flicker noise as random electron traps can be identified in the PCM's lattice. Flicker noise for EPCMs is even higher when the PCM used in the phase-change memory structure is in the amorphous state [125]. In addition to flicker noise, the PCMs used in the same phase-change memory cells respond differently to the same programming pulse. This issue will lead to inaccuracy and dispersion of OPCMs and EPCMs when being used as an in-memory computing unit. The work in [125] demonstrated that the aforementioned issues can be alleviated by using an optimized iterative programming approach. They showed that by using this programming technique, the conductance spread is under 14% and the relative drift is under 15%, with the relative noise being less than 9% for 90% of the cells.

G. COMPLEXITY AND FOOTPRINT OVERHEAD

We observed in [5] that we cannot simply replace the EPCMs with OPCMs in a memory architecture. Simply replacing the EPCMs with OPCMs will lead to thermal, read and write latency, and energy issues because of the incompatibility of OPCMs with integrated memory architectures. Consequently, additional photonic I/O and circuitry, such as E-O-E units, will be needed to convert the memory controller commands into optical signals. Moreover, a large number of silicon photonic links is required to replace the electrical links to convey the information from the memory controller to the OPCMs and vice versa. This requires using a vast number of active devices, such as electro-optical modulators, high-speed integrated photodetectors [126], and additional control units to optically address the OPCM cells. This makes the memory architecture more susceptible to optical loss and crosstalk noise, increases the power consumption and footprint, and diminishes the memory bandwidth [127]. In addition, the design of the E-O-E unit should be optimized to minimize the access time to the memory to read and write the cells. Furthermore, to deal with the device- and material-level limitations, the OPCM cells should be optimized to have minimal power consumption and latency.

H. FABRICATION-PROCESS VARIATIONS

Fabrication-process variations is a known issue in silicon photonic integrated circuits, which necessitate additional efforts

to design devices that are resilient to variations [97], [128], [129], [130], [131]. In the state-of-the-art designs for OPCM cells, the thickness of the PCM was considered extremely thin (i.e., ≈10 nm), and hence a slight variation in the thickness of the PCM sample leads to changes in the power absorption, transmission levels, and stored data. This limitation can increase the number of misreads and the bit-error rate (BER) in OPCM-based memory systems [5]. The effect on the latency and power consumption can be minor, but it will be accumulated as we scale the memory architecture. Therefore, OPCM cells should be designed and optimized to be resilient to fabrication imperfections. Mathematical models can be used to model the attenuation coefficient against the sample geometrical parameters and variations, like thickness and length of the OPCM cells, in which the GST is fabricated on top of a Si_3N_4 ridge waveguide [132]. The attenuation coefficient can be used as a figure of merit to design an OPCM cell for data storage and photonic computing which is resilient to fabrication-process variations.

I. SCALABILITY

Scalability is of importance when it comes to photonic data storage technologies. As the dimension of a single OPCM cell decreases, its properties also change according to its size reduction. Research shows that as the phase change material's film thickness decreases, T_g, optical band gap, incubation time, resistivity, refractive index, and extinction coefficient for most wavelengths increases [10], [133], [134], [135], [136], [137]. It was also shown that the crystallization speed would increase as the thickness of the PCM decreases. Overall, the thickness of a PCM in OPCMs cannot be smaller than 2 nm becasue the material will lose its dynamic properties stemming from phase transition.

J. SECURITY

Security is another challenge that stems from the aging issue in phase-change memories. Nonvolatile phase-change memory cells offer a limited capacity of write procedures. With an increase in the number of writes over time, the memory cell ages, and hence it is prone to write attacks [138]. The data which has been written on phase-change memory cells will remain even after power-off. The reason for this is because of using the physical state of the material to store the data. This will increase the threat of data accessibility by a malicious agent. In addition to the aforementioned threats, a bus snooping attack is another possible security threat in phase-change memories where a third agent can access the data which is being communicated over a chip. Different mapping and encryption approaches can be utilized to overcome this challenge in memory architectures based on phase-change memories.

K. PHASE CHANGE MATERIALS FOR PHOTONIC NETWORKS

In addition to the application of PCMs for implementing photonic memory architectures and photonic in-memory computing units, PCMs can also be integrated into conventional photonic devices to realize programmable photonic devices for photonic networks. For example, PCMs like Sb_2Se_3 can be integrated into passive SiPh directional couplers (DCs) to realize a tunable photonic switching cell [38], [60]. By controlling the phase state of Sb_2Se_3, the portion of an optical signal that can be coupled from one waveguide to another in the DC can be controlled. Lower loss and crosstalk can be offered by integrating Sb_2Se_3 into SiPh DCs compared to GST and Sb_2Se_3 [19]. This was the main motivation for using Sb_2Se_3 in [38].

MZIs are critical photonic devices that can be used in a variety of applications, such as silicon photonic switching networks [150], [151], [152] and electro-optic modulators [153] for optical communication platforms. A single MZI can be constructed by connecting two DCs and two straight waveguides. Therefore, to realize MZIs with low loss and crosstalk noise, DCs should have optimal design and performance. The work in [38] demonstrated that tunable DCs with a low insertion loss ($<$1.5 dB) and crosstalk noise (-20 to -40 dB) can be designed to construct MZIs using Sb_2Se_3. In addition, it was shown that such a design has a fast switching time (50 ns for GST and 78 ns for Sb_2Se_3) when using the DC as a photonic switching element.

The work in [141] and [142] proposed a design utilizing PCMs (Sb_2Se_3) to implement phase shifters to realize specific optical phase delays. PCMs can be also used to tune the performance of MRRs in optical switching networks based on MRRs [154]. The undesired resonance shift in MRRs (e.g., due to thermal or process variations [128]) is known as one of the main constraints in using MRRs for wavelength-selective photonic switching elements. The work in [154] showed that GST can be used to tune the resonant wavelength in race-track MRRs to eliminate the need for power-hungry frequency response adjustments, using, for example, thermal tuning. This makes the photonic switching elements much more power efficient and more resilient to thermal and fabrication-process variations. PCM-based switching elements can also be used to implement 2.5D SiPh interposer networks. For example, the work in [155] showed that 2.5D interposer-based photonic networks can utilize phase change materials to achieve reconfigurable bandwidth and power efficient communication in 2.5D chiplet systems. Although the application of PCMs in photonic devices is promising, more research is required to further enhance the performance of PCMs considering photonic network requirements.

L. PHASE CHANGE MATERIALS FOR PHOTONIC COMPUTING

PCMs can be also used to construct photonic computing units to accelerate the performance of AI accelerator platforms. An array of MZIs with integrated phase shifters can be used to perform matrix-vector multiplication at light speed using a single wavelength to implement coherent photonic neural networks for high-speed optical AI accelerators [139], [156]. The DCs designed in [38] can be also used to construct MZIs with low insertion loss and crosstalk noise

TABLE 5. Summery of different applications of PCMs in integrated photonics. (PIC: photonic integrated circuits).

Reference	Application	Material	Stimulation
[38], [60]	Tunable directional couplers	Sb_2S_3	Optical
[140]	Tunable MZIs	Sb_2S_3	Optical/Electrical
[141]	Tunable race-track MRR	GST	Optical
[142], [143]	Photonic phase shifters	Sb_2Se_3	Electrical
[144]	Application of silicon and silicon nitride in PCM-based PICs	–	–
[53], [62], [63]	Photonic data storage	GST	Optical
[6], [47], [48]	Data storage	GST	Electrical
[61]	Photonic data storage	GSST	Optical
[36]	Thermal-aware design optimization of photonic data storage cells	GST	Optical
[64]	Photonic switches	GSST	Optical
[57]	Photonic logic gates	GST	Optical
[65]	Photonic switches and data storage cells	GST	Optical
[11], [12]	Multilevel photonic data storage cell	GST	Optical
[67]	Photonic switches	GST	Electrical
[5]	OPCM-based memory architecture	GST	Optical
[67], [68], [145]	Plasmonically enhanced photonic data storage cells	GST	Optical
[146]	Electrically driven photonic computing units	GST	Electrical
[92], [93], [100], [101], [147]–[149]	Optically driven photonic computing units	GST	Optical
[54]	Performance optimization of photonic in-memory computing units	GST	Optical
[92]–[95], [99]–[104], [150]	Photonic in-memory computing units	GST	Optical/Electrical
[45]	Reducing the programming energy using a graphene layer	GST	Optical/Electrical

for coherent photonic neural networks [75]. In addition, considering the design in Fig. 8, the proposed PCM-based cell can be extended to perform matrix-vector multiplication in the optical domain. Compared to conventional photonic accelerators (e.g., those based on MZI arrays [75], [156] or MRR banks [77]), the benefits of this design are lower loss and accumulated crosstalk noise, elimination of bulky metallic contacts required for the phase shifters, and compact footprint.

Considering a single GST cell for photonic in-memory computing, photonic tensor cores can be designed based on wavelength-division multiplexing by using an array of MRRs integrated with phase-change memories to perform computationally expensive matrix-vector multiplication with zero static power and high speed [145], to outperform graphic processing units (GPUs). As another example, an architecture based on PCMs for photonic tensor cores was proposed in [146] and [147]. The difference of this design compared to [145] is that the PCM used in cells can be controlled via optical laser pulses. The design presented in [146] and [147] was able to operate at the speed of two tera-MAC operations per second, i.e., two trillion (10^{12}) MAC operations per second. Despite their novel approach to implement an integrated PCM-based photonic tensor core processing unit, the proposed design lacks a second unit for reference computation. The work in [148] addressed this problem by integrating a second GST cell on each photonic computing element to perform reference computation at the same time. Research in this area is still in progress to enhance the performance of the PCM-based photonic tensor cores to alleviate the scalability limitations originating from aging of the cells [157] and coherent crosstalk and insertion loss, and to store kernel weights and efficiently reconfigure noncoherent AI accelerators [84], [85], [86], [87].

V. CONCLUSION

Different from existing survey papers on photonic memories, this paper surveyed the fundamentals of PCMs from the material level to the system level for contemporary PCM-based photonic memories. A complete overview of the optical, thermal, and electrical properties of PCMs was presented. In addition, we reviewed the application of PCMs in the implementation of photonic memories and the benefits they bring to emerging many-core computing systems. Some applications of PCMs in-memory architectures and for in-memory computing units were presented as well as optimization approaches to alleviate the limitations related to the endurance caused by a high number of writes on photonic processing units, like PCM-based photonic tensor cores. Furthermore, we showed a simulation procedure for PCM-based photonic devices using commercial tools. Open challenges and opportunities in the design and fabrication of phase-change-material-based photonic devices were discussed, which can be used to further advance emerging photonic computing and communication system architectures. Table 5 summarizes the different applications discussed in this survey, from storage to non-storage photonic devices.

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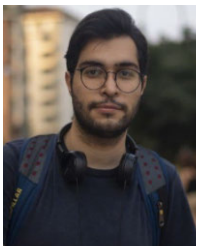

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