# INTEGRATED PHOTONIC AI ACCELERATORS UNDER HARDWARE SECURITY ATTACKS: IMPACTS AND COUNTERMEASURES \*

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#### ABSTRACT

Integrated photonics based on silicon photonics platform is driving several application domains, from enabling ultra-fast chip-scale communication in high-performance computing systems to energy-efficient optical computation in artificial intelligence (AI) hardware accelerators. Integrating silicon photonics into a system necessitates the adoption of interfaces between the photonic and the electronic subsystems, which are required for buffering data and optical-to-electrical and electrical-to-optical conversions. Consequently, this can lead to new and inevitable security breaches that cannot be fully addressed using hardware security solutions proposed for purely electronic systems. This paper explores different types of attacks profiting from such breaches in integrated photonic neural network accelerators. We show the impact of these attacks on the system performance (i.e., power and phase distributions, which impact accuracy) and possible solutions to counter such attacks.

Keywords Silicon Photonics · Security · Intrusion Detection System · AI Accelerator

#### **1** Introduction

Silicon photonic (SiPh) integrated circuits exploit the fast optical-domain data transmission to realize ultra-high bandwidth communication with low power consumption in high-performance computing systems [1]. SiPh has been deployed in many-core systems to improve their communication infrastructure [2], and most recently, in artificial intelligence (AI) hardware accelerators to boost both their communication and computation performance [3, 4].

Integrating photonic and electronic systems (i.e., optoelectronic systems) necessitates the use of opto-electrical interfaces to deal with signals from different domains. Such integration also necessitates SiPh node configuration (e.g., to adjust signal phase) for routing and computation [5]. For instance, the SiPh-based AI accelerator (SPAA) proposed in [3] develops a light-speed matrix-multiplication unit whose operation is based on a diagonal decomposition methodology. The matrix defined in the digital domain (i.e., application executing on a processor) needs to be properly mapped to the SPAA. This is done by defining the correct transformation signal phases in each SiPh node, where an electrical controller adjusts the tuning circuitry (e.g., by applying a bias voltage) on each SiPh node to realize the required optical phase. The controller has access to each SiPh node through an interface connection. The same is true for the

<sup>\*</sup> Citation: To appear on the procedings of IEEE MWSCAS 2023



(a) SiPh building blocks. MZI operation states: (i) Cross and (ii) Bar. MRR operation states: (iii) OFF resonance and (iv) ON resonance.



(b) Overview of a controller integration with a SPAA. The electrical controller interfaces with the SPAA to configure it (e.g., set optical phases).

Figure 1: (a) SiPh building blocks and (b) an overview of controller integration with a SPAA.

matrix inputs, mapped as the inputs of the SiPh circuit. Recovering the results in the digital domain is performed by optical-to-electrical conversions and photodetectors.

Systems integrating different technologies (e.g., an optoelectronic system) are more susceptible to malicious attacks [6]. In optoelectronic systems, attackers can profit from multiple signal conversions required to exchange data between the two domains and act on the integration interfaces. Furthermore, any photonic device operation is determined by the device's design parameters (e.g., waveguide width) and temperature, where minimal changes can change the device operation. For example, considering the thermal sensitivity of SiPh devices, in the SPAA proposed in [3], an attacker (e.g., an IP integrated in the system) can increase its own temperature (e.g., by performing heavy mathematical operations). Consequently, this can impose thermal crosstalk [7], creating signal noises by altering the adjusted signal phase shifts in the SiPh devices in proximity. Such phase noises will impact the inferencing accuracy in the SPAA (e.g., by up to 70% as reported in [8, 9]), degrading the overall system performance. The impact of different attacks can include data leakage and manipulation, service and sleep-denial, irreversible losses, systemic abnormal behaviour, and permanent breakdown [10].

Techniques to address electronic hardware Trojan (e-HT) attacks can be explored for optoelectronic systems. Still, most of such techniques are inefficient and will fail to address optoelectronic hardware security concerns [11]. This is due to the very nature of the breaches in such systems. While e-HTs target IPs and electrical paths, optical HTs (o-HTs) target the optoelectronic interfaces and introduce disturbances to the SPAA. Prior efforts [12, 6] presented solutions to enhance the security of optoelectronic systems by taking into account the characteristics of the optical path, adding an extra layer of security to the design. In this paper, we discuss attacks and their impacts targeting SPAAs and a defence mechanism to detect such attacks. As discussed, SPAAs are prone to interferences, which can hinder their employment. Hence, tackling security attacks is essential for further advancement and employment of such accelerators.

## 2 Photonic Devices and AI Accelerators

Mach–Zehnder interferometers (MZIs) and microring resonators (MRRs) are widely used as building blocks in different SiPh integrated circuits [13]. Fig. 1(a) illustrates conventional MZI and MRR designs. An MZI is an interferometric device that includes two 3-dB couplers and optical phase shifters on one or both arms. A phase shifter can be implemented using electro-optic or thermo-optic tuning mechanisms to introduce an optical phase shift on the electric field of optical signals traversing the MZI arms. As a result, the optical signals entering the output coupler can experience destructive or constructive interference (or somewhere in between). For example, in the 2×2 MZI shown in Fig. 1(a), the phase difference of  $\Delta \Phi = 0$  or  $\pi$  results in constructive or destructive interference. MZIs are often used in the design of optical switched networks and coherent SPAAs [14, 15].

An MRR is a resonating wavelength-selective device. Considering Fig. 1(a), an optical signal on the input port can be controlled using a biased arm on the ring. The resonant wavelength in an MRR can be adjusted by applying electro-optic or thermo-optic tuning to the MRR. The input signal propagates towards the through port when the ring is *OFF resonance*, and when the MRR is *ON resonance*, the input signal will couple into the ring and goes to the drop port. MRRs are often used in the design of photonic switched networks, modulators, filters, and noncoherent SPAAs [4]. For example, the work in [16] proposes to use MRRs to create non-linear functions defined by leveraging the impact of electro/thermo-optic effects in MRRs.



(a) Output readings with and without (b) Validation environment presenting the variations. (c) Unitary r

(c) Unitary matrix of a photonic complex-valued neural network (PCNN) [20].

Figure 2: (a) Optical linear multiplier example architecture and (b) validation environment (c) Output readings considering variations and not.

SiPh node configuration can be static (passive), defined during design time, or dynamically configured during execution time. Such dynamic reconfigurations can be achieved electronically following the application needs. Fig. 1(b) illustrates an example of an electronic controller integrated with a SPAA. In this example, each SiPh node in the SPAA is connected to the controller, which can configure the desired operation of the SiPh node. It can interact with the SPAA through electro-optic interfaces, and by using methods such as thermal tuning (e.g., using microheaters) or carrier injection (e.g., through PN junctions). Accordingly, an electronic controller can, for example, configure an MZI by applying a given voltage to increase the temperature in a microheater placed on top of an MZI arm, to change the optical signal phase in the MZI. Taking as an example a coherent SPAA [3], optical phases are adjusted in the underlying SiPh nodes (e.g., MZIs in [3]) by an electronic controller. Such adjusted phase values represent the weight parameters in the neural network, which can be obtained using software training and decomposition algorithms [3].

Using both MZIs and MRRs can help design powerful photonic computing architectures capable of performing complex operations. In general, SPAAs use a combination of power intensity and signal phases on the outputs to mimic different operations. For example, a photonic processor using both MZIs and MRRs can be used to perform Fourier transforms, which are essential for applications such as signal processing, image recognition, and data compression [17]. Coherent SPAAs based on MZIs, considered as an example in this paper, can be designed by performing coherent multiplication between an input vector  $I_n$  (i.e., input optical signals modulated with input features) and a weight matrix W (i.e., defined by adjusting phase settings on different MZIs), to obtain an output vector  $O_n$ . The linear multipliers can be represented using two unitary multipliers and a diagonal matrix, which are obtained using singular value decomposition (SVD) [3]. The multipliers and the diagonal matrix can be realized using a network of interconnected MZIs with different typologies. In [18, 19], an  $N \times N$  neural network is realized using a series of special unitary (SU) groups. Each SU is built using an MZI with two phase controllers, denoted SU(2). Based on SU(2), larger SU(N) groups are built and the entire configurable neural network can be created, in which N represents the number of inputs and outputs of the neural network (i.e.,  $\forall I_n \to I_n \times W = O_n$ ).

## 3 SPAAs under Hardware Security Attacks

Modern systems are prone to attacks due to a variety of vulnerabilities. These range from software bugs leading to undesired behaviour to maliciously inserted malware in a system. Pure electronic and optoelectronic systems share many of such vulnerabilities. One type of an attack that has the potential to severely affect a system and is hard to detect is the Hardware Trojan (HT). HTs act to steal information, degrade the performance, or even destroy the attacked system. Such type of an attack is hard to detect as it can remain in an "idle state" until some action triggers its execution [21]. Although sharing many vulnerabilities, optoelectronic systems have unique breaches and affected areas, needing special security treatment.

Denial-of-service (DoS) attacks can be injected by HTs. For instance, a sinkhole attack is a type of an attack in which one node actively collects data from a network path. This can be performed by an invaded node that redirects a transmission in the network to a different direction/destination. Another type of the same attack works by making false requests for neighbouring routers in order to receive transmissions addressed to other nodes. A flooding attack is a different type of DoS attack where an invaded IP/node affects the transmissions in the network by injecting noise/adversarial signals. This type of an attack aims at depriving the connected nodes from properly using the transmission path, as transmissions with too much noise are occurring. In a black-hole attack, one or more nodes are tweaked in such a way that the transmission(s) will target dead ends, leading to packet drops.

SiPh devices are sensitive to different variations, including fabrication-process (PV) and thermal variations. Prior studies showed that such variations will create optical phase noises in SPAAs, which can cause up to a 70% reduction in the inferencing accuracy of the network [8, 9]. SPAAs are vulnerable to attacks that may leverage from HTs to inject

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Figure 3: Output readings with and without perturbances, showing the impact on the outputs for each type of attack. The x-axis presents the outputs. On the y-axis, power is presented in dBm and phase is in radians.

noise into channels (e.g., cause changes in adjusted phases). Malicious IPs (e.g., with infected software components) can also increase the temperature of neighbouring nodes, which can result in variances in the physical characteristics of SiPh nodes, and ultimately, lead to incorrect operations. Another study observed a decrease in the accuracy of a SPAA by 5% when the temperature was increased from 25°C to 50°C. Moreover, it was demonstrated that the presence of optical phase noise can lead to a reduction in the network's accuracy, with an average error rate of 3.7% [8].

Although solutions are proposed for electronic HTs [22], not all of them are directly applicable to optoelectronic systems. For optoelectronic systems, efforts are made to ensure the security of designs by relying on the characteristics of the circuit [23]. Some solutions have been presented to enhance the security of optoelectronic systems, taking advantage of different aspects of SPAAs, such as PVs [24]. In [11], the focus is on tampering and snooping attacks during the thermal sensing in photonic networks-on-chip (PNoCs). A detection scheme was presented based on spiking neural networks (SNNs) trained to learn network patterns. By using thermal sensing and SNN feedback, the overall system security against tampering and snooping attacks is enhanced. The work in [25] presented a framework that utilizes PV-based authentication signatures. A new layer is proposed, integrated in the network gateway interface, which acts to encrypt transmitted data and detect attacks in runtime. In [6], a technique was proposed based on the integration of the network controller with the detection mechanism while focusing on tackling HT attacks. SecONet was presented in [12] aiming at securing a SiPh-based network against eavesdropping, spoofing, replay, and messageremoval attacks. This is achieved by using a combination of speculative and pre-computation, where a security layer and key-generating units are added to the network hardware stack. Nevertheless, the aforementioned efforts are all limited by different factors, such as strong dependence on the electronic controller, using pre-trained neural networks, or complex and error-prone off-line evaluations, such as experimentally measuring deviations. Also, no prior work has studied SPAAs and proposed countermeasures under security attacks.

In this paper, we explore a non-intrusive method relying on side-channel analysis. Side-channel analysis is a technique used to detect perturbations by measuring the output readings of the SPAA during operation. To do that, a hardware module is integrated with the electronic layer of the system and interacts with the SPAA to collect information of the transmitted signals. Attacks, such as black holes for instance, will interfere with the signal transmissions in the SPAA, which will lead to noise being inserted on the transmitted signals. The noise difference can be used though as a mechanism to detect perturbations (e.g., malicious interactions or attacks) in the SPAA.

## **4** Countermeasuring the Breaches

SPAAs are susceptible to various types of attacks that can impact their accuracy directly [8]. As demonstrated by [11, 6], perturbation detection in a SPAA is feasible by gathering underlying transmission information and analyzing transmission patterns. Computer-aided machine learning algorithms or modified network electronic controllers can perform this task. However, these methods necessitate either the transfer of data to perform off-line calculations or the modification of integrated modules, which is rarely feasible. In contrast, our approach here relies on side-channel analysis to detect variations in the transmitted signals. This approach enables real-time operational analysis while being agnostic to the SPAA architecture.

We introduce a two-step technique for attack detection in SPAAs. In the first step, during the initialization phase, baseline operation scenarios are established, including input laser(s) information and SiPh node configuration parameters. Reference output values are stored for later use. In the second step, during execution time, the same baseline scenarios are repeated, and the new output values are compared with the stored ones. If the difference between the readings exceeds a configured threshold, an alarm is triggered, and the system is flagged as suspicious. This paper focuses solely on the intrusion detection system (IDS) and does not address finding the point of breach. High-level entities in the system, such as the operating system or network controller, can handle the alarm. The motivation behind this technique stems from the low tolerance of SiPh nodes to variations. Fig. 2(a) illustrates the impact of variances

on an MZI node, similar to the one shown in Fig.1(a). As it can be seen, variations in the node cause deviations in the readings from their expected values. Such deviations impact the SPAA system performance, as shown by [8].

Our technique is designed to detect runtime perturbations and inform the system about the issue, allowing for any modifications to the SPAA to be detected by our module. More importantly, no changes to the internal hardware modules (such as the network controller) or the transfer of data to external computing hosts (such as for machine learning algorithms) are required. Instead, our module can be seamlessly integrated into the underlying system and act as an integrated module.

# 5 Results and Discussions

To validate our technique, we used Ansys Lumerical Interconnect to simulate dfferent SPAAs [3, 19, 18, 20]. The simulation environment is illustrated in Fig. 2(b), and all electrical modules were described using Python for seamless integration with SiPh models. We employed different SPAA architectures in our study [3, 19, 18], including the one presented in Fig. 2(c), which is used in [20] as part of a photonic complex-valued neural network (PCNN).

To provide insight into the impact of different types of attacks, such as black-hole, sinkhole, re-routing, IP highjacking, and flooding, we present the outputs under normal conditions and under attacks in Fig. 3, for the architecture presented in Fig. 2(c). The figures show the output power intensities and phases distributions. Under normal operation, all the readings should be identical or as close as possible to the designed ones. As it is possible to see, under different attacks, many variations on the readings occur, which lead to a decrease in the network accuracy, as previously reported in the literature[26]. By using these readings, our side-channel IDS can easily detect attacks and trigger an alarm. Despite its simplicity, our approach is effective because of the low variance required on the SiPh nodes to impact the outputs, as shown by our experimental results — see Fig. 3.

Our approach offers an efficient and non-intrusive technique for detecting perturbations in SPAAs. The proposed method only requires baseline operation scenarios to be established during the initialization phase, and during execution time, the system compares the new output values with the stored reference output values. If the difference between the readings is greater than a specified threshold, an alarm is triggered. Our approach does not require any modification on the internal hardware modules or the transfer of data to outside computing hosts. With this approach, we can successfully detect any perturbation on the SPAA without incurring additional overhead.

## 6 Conclusion

Silicon-photonic-based AI accelerators (SPAAs) require different opto-electrical interfaces for proper function (e.g., data storage). But using such interfaces make SPAAs vulnerable to various types of attacks. This paper presented a study of different attacks that exploit such vulnerabilities and shows their impact on the system performance. We also proposed possible countermeasures to mitigate these attacks. Our technique is validated using circuit models for SPAA simulation, and we demonstrated its ability to detect different attacks. We believe that this technique offers a valuable tool for ensuring the safety of emerging SPAAs.

## Acknowledgement

This work was supported in part by the National Science Foundation (NSF) under grant number CNS-2046226.

## References

- [1] S.Pasricha and M. Nikdast. A Survey of Silicon Photonics for Energy-Efficient Manycore Computing. *IEEE Design Test*, 2020.
- [2] W. J. Dally. Future Directions for On-Chip Interconnection Networks. http://www.ece.ucdavis.edu/ ocin06/talks/dally.pdf.
- [3] W. R. Clements et al. Optimal design for universal multiport interferometers. Optica, 2016.
- [4] F.P. Sunny et al. A survey on silicon photonics for deep learning. J. Emerg. Technol. Comput. Syst., 17, 2021.
- [5] Y. Xiong *et al.* Towards a Fast Centralized Controller for Integrated Silicon Photonic Multistage MZI-based Switches. OSA, 2016.
- [6] P. Guo *et al.* Potential threats and possible countermeasures for photonic network-on-chip. *IEEE Communications Magazine*, 2020.

- [7] S. Kyatam *et al.* Estimation of maximum temperature and thermal crosstalk between two active elements in a pic: development of a thermal equivalent circuit. *Appl. Opt.*, 2020.
- [8] S. Banerjee *et al.* Modeling silicon-photonic neural networks under uncertainties. In *IEEE DATE Conference*, 2021.
- [9] S. Banerjee et al. On the impact of uncertainties in silicon-photonic neural networks. IEEE Design & Test, 2023.
- [10] C. Moratelli *et al.* The Convergence of Technologies to Provide Security on IoT Edge Devices. *Convergence*, 2021.
- [11] J. Zhou *et al*. Attack mitigation of hardware trojans for thermal sensing via micro-ring resonator in optical nocs. *ACM JETC*, 2021.
- [12] J. Bashir *et al.* Seconet: A security framework for a photonic network-on-chip. In *14th IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, 2020.
- [13] L. Chrostowski and M. Hochberg. *Silicon Photonics Design: From Devices to Systems*. Cambridge University Press, 2015.
- [14] H. Zhou *et al.* Photonic matrix multiplication lights up photonic accelerator and beyond. *Light: Science & Applications*, 2022.
- [15] Md. S. Islam and M.J. Barsha. Mach zehnder interferometer (mzi) as a switch for all optical network. In *International Conference on Innovation in Engineering and Technology*, pages 1–5, 2018.
- [16] C. Huang et al. Programmable silicon photonic optical thresholder. IEEE Photonics Technology Letters, 2019.
- [17] S. S. Kou *et al.* On-chip photonic fourier transform with surface plasmon polaritons. *Light: Science & Applica-tions*, 2016.
- [18] F. Shokraneh *et al.* A single layer neural network implemented by a 4x4 mzi-based optical processor. *IEEE Photonics Journal*, 2019.
- [19] Y. Shen et al. Deep learning with coherent nanophotonic circuits. Nature Photon 11, 2017.
- [20] R. Wang et al. Multicore photonic complex-valued neural network with transformation layer. Photonics, 2022.
- [21] W. Hu et al. Detecting hardware trojans with gate-level information-flow tracking. Computer, 2016.
- [22] J. Frey and Q. Yu. A hardened network-on-chip design using runtime hardware trojan mitigation methods. *Integration*, 2017.
- [23] L. Zhang *et al.* Effectiveness of ht-assisted sinkhole and blackhole denial of service attacks targeting mesh networks-on-chip. *Journal of Systems Architecture*, 2018.
- [24] F. Pavanello *et al.* Recent advances in photonic physical unclonable functions. In 2021 IEEE European Test Symposium (ETS), 2021.
- [25] S.V.R. Chittamuru *et al.* Exploiting Process Variations to Secure Photonic NoC Architectures From Snooping Attacks. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2021.
- [26] S. Banerjee et al. Characterizing coherent integrated photonic neural networks under imperfections. J. of Lightwave Tech., 2023.