Fully CMOS-Compatible On-Chip Optical Clock Distribution and Recovery

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***Abstract*—Clock distribution in the multi-gigahertz range is getting increasingly difficult due to more stringent requirements for skew and jitter on one hand and the deteriorating supply voltage integrity and process variation on the other hand. Global clock network, especially in nanometer CMOS designs with ever increasing die sizes, has become a prominent performance limiter. A potential alternative to traditional interconnect technology for achieving clock distribution beyond 10 GHz while maintaining required skew and jitter budgets is using on-chip optical interconnects. A practical on-chip optical clocking system must be CMOS compatible in order to provide attractive cost effectiveness for system level integration and ease of manufacturing. This paper presents the design of a fully CMOS compatible optical clock distribution and recovery system in a 3.3 V, 0.35-μm CMOS process. Experimental results from the test chip prove the feasibility of providing optical-electrical interface in devices and circuits in a fully CMOS compatible manufacturing environment. Although the test chips were designed in a mature CMOS process technology and the measured performance is low, the test chips demonstrated the feasibility of on-chip optoelectronic integration with fully CMOS compatible process. On-chip optical clock distribution is one of the natural applications of fully CMOS compatible on-chip optical interconnect technology.**

***Index Terms*—Fully CMOS compatible on-chip optical interconnect, optical clock distribution, optical H-tree, transimpedance amplifiers (TIA).**

I. Introduction

CURRENT cutting edge VLSI designs have operating clock frequencies over 4–5 GHz built on 65-nm SOI process with 10 levels of low-k copper interconnect [1] and, over 2–2.4 GHz built on a 65-nm bulk CMOS process with 8 levels of low-k copper interconnect [2]. CMOS technologies will extend well into 22 nm within the next decade making process controllability difficult and resulting in increased processing variations [3]–[7]. CMOS scaling to the nanometer regime have caused long global wires to become an important design constraint and bottleneck. Ever increasing levels of integration further compounds this problem, necessitating a better interconnection technology. In a clock distribution network, process variations, and environmental variations introduce skew and jitter [8]. With increasing demand for higher performance and faster chips, increasing the operating clock frequency is an inevitable consequence. A faster clock frequency corresponds to a tighter clock period and requires strict limits on clock uncertainties. Optical signaling technology has immense potential to improve clock skew, jitter, and delay caused by back end of line (BEOL) deterioration in traditional interconnects [9].

The worst case global clock skew for an electrical clock tree implemented with unscaled interconnects, can consume up to 70% of the total clock period as technology scales from 180 to 22 nm [10]. Similarly, the worst case electrical global clock jitter can consume well over 20% of the total clock period as technology scales from 180 to 22 nm [10]. However complex and high performance VLSI systems such as microprocessors, implement a variety of techniques to reduce clock skew. These techniques include a variety of active clock deskewing systems [11], [12], in-path clock correction with clock retimers [13] and detailed design time clock buffer tuning to minimize worst case clock skew [14], [15]. Some microprocessor designs also use grids to distribute clock to reduce skew at the expense of clock power consumption, as illustrated in [14] and [15]. Consequently, the design complexity and cost (area and power) of using these techniques will increase. Optical clock distribution technique is considered to be a good alternative to conventional methods of balancing clock trees and clock buffers to reduce skew and jitter. Key advantages of optical clock distribution over electrical clock distribution are reduction in clock skew, delay, and clock network power as global clock buffers become unnecessary due to low optical transmission loss, reduced interference to and from neighboring electrical signals, high signal speed, independence of signal speed on waveguide variations thereby increasing robustness and low heat generation. These advantages make an optical clock distribution methodology very attractive. A comparative study in [10] shows that the global optical clock skew and jitter remain constant at under 10% and 6%, respectively, as technology scales from 180 to 22 nm node.

However, challenges in optical clocking are related to seamlessly integrating the optical components with bulk CMOS manufacturing to reduce integration cost and the additional need for optoelectronics to regenerate electrical clock signals. In a hierarchical electrical clock distribution system with multiple stages, replacing every stage with optical clocking leads to a power hungry solution. This is especially true with large die sizes such as modern multi-core processor chips. To alleviate this problem an optical-electrical hybrid approach to clock distribution was suggested in [10], where the first few stages of the clock tree is implemented optically followed by smaller local electrical

Manuscript received June 30, 2008; revised January 02, 2009.

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Digital Object Identifier 10.1109/TVLSI.2009.2024206

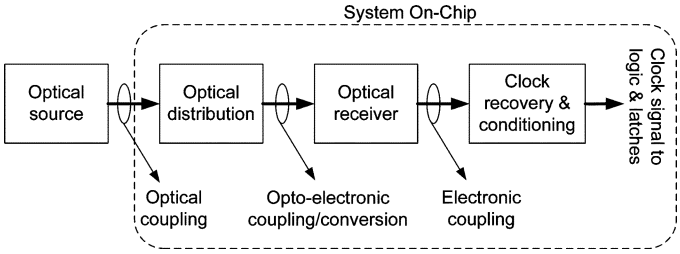

Fig. 1. Optical clock distribution system.

clock trees. This paper presents a set of components designed to illustrate the feasibility of a fully CMOS compatible on-chip optical interconnect system suitable for future on-chip optical clock distribution applications. Although the designs were implemented using a mature 0.35-μm CMOS process, the objective is to demonstrate the technological feasibility of such low-cost, integrated optoelectronic system for future high performance VLSI systems.

The remaining portions of this paper are organized as follows. The optical clocking system design is presented in Section II. The test circuits and architecture are presented in Section III. The test chip details and experimental results are discussed in Section IV and concluding remarks are presented in Section V.

II. Essential Components in on-Chip Optical Signalling System

Electrical clock distribution networks utilize geometrical or electrical matching or grid routing to minimize clock skew [16], [17]. To minimize clock delay, large, and power hungry clock buffers are inserted in the clock distribution network. These buffers can consume up to 30%–40% of the total chip power [18]. Most of the existing optical clocking solutions involve using non-CMOS compatible exotic materials or processing steps which are expensive to integrate into existing manufacturing flows, preventing their wide spread adoption [19]. A truly CMOS compatible solution will reduce manufacturing cost and facilitate easier integration into main stream manufacturing. Such an approach was introduced in [20]–[22]. Fig. 1 shows the various stages in an optical clocking system which is compatible with the proposed approach in [20] and [21]. The optical clock source is optically coupled to the distribution network, which is optoelectronically coupled to an optical detector that converts incident optical energy into current pulses. The recovery and signal condition stage then amplifies the current pulses to generate corresponding rail-to-rail electrical clock signal for local distribution. Clock signal is distributed to the entire chip by dividing the chip into clock domains and placing a clock recovery resource or transimpedance amplifier (TIA) station in each domain.

A. Optical Clock Source

The optical source providing the optical clock is a laser diode that is external to the chip. The laser diode is attached to a single mode optical fiber. The optical energy at the end of this fiber is the optical input to the clock distribution network. The optical coupling into the clock distribution network is achieved by positioning and gluing the fiber to the polished edge of the die. A 685 nm, 10 mW (Sharp-GH06510B2A) laser diode coupled with a 4-μm core and 125-μm cladding optic fiber, cleaved at one end is used as the optical clock source. The input laser wavelength (visible red 685 nm) was carefully chosen such that the optical energy is not absorbed by the silicon nitride waveguide core, but would be absorbed by the polysilicon detector. In addition, 685-nm laser sources are readily available and since 685-nm laser is visible to the human eye, it simplifies the verification of optical alignment and waveguide optical confinement. The laser diode used in this work was modulated using a square wave from a function generator, to simulate a clock signal.

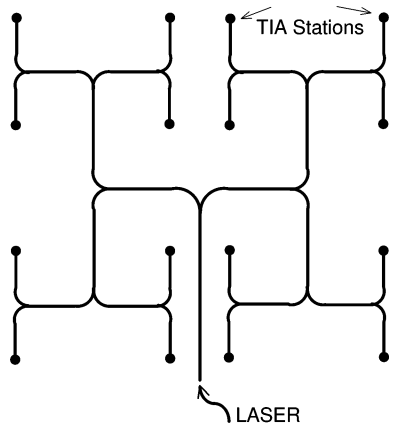

Fig. 2. Line diagram of the optical H-tree.

B. Optical Clock Distribution Tree

Extending the idea presented in [23] to the IC domain, on-chip waveguides can be used to construct a planar optical H-tree. A 16 leaf-node, balanced optical H-tree (as shown in Fig. 2) is used as the optical clock distribution network in the proposed on-chip optical clock distribution and recovery system. Seamless integration of the optical distribution network into standard CMOS processing is of paramount importance, especially since the distribution network is spatially the largest component of the system and where the advantages of optical signalling is most pronounced. The planar waveguide core is constructed from silicon nitride (SiN), which is normally used for copper encapsulation in a standard CMOS process. The cladding layers are made of silicon dioxide (SiO2) and low-k oxides such as phospho-silicate glass (PSG) and tetra ethyl ortho silane (TEOS), normally used as inter-metal dielectric material in standard CMOS processes. The silicon nitride is deposited using a plasma-enhanced chemical vapor deposition (PECVD) technique on to a PSG/TEOS/SiO2 sandwich, which serves as the bottom cladding. The top cladding is a TEOS/SiO2 layer. The high index difference between the waveguide core ($n = 1.8$) and cladding ($n = 1.45$) provides excellent optical confinement in the waveguide. To improve optical coupling between the H-tree and the external optical source, i.e., the optic fiber, the waveguide core is wider at the die edge and slowly tapered down to the detectors.

C. Optical Receiver: Photo Detector

Electrical clock is **recovered** from optical clock by using a photo detector which is placed at the end of each H-tree leaf-node. In addition to being truly CMOS compatible, the photo

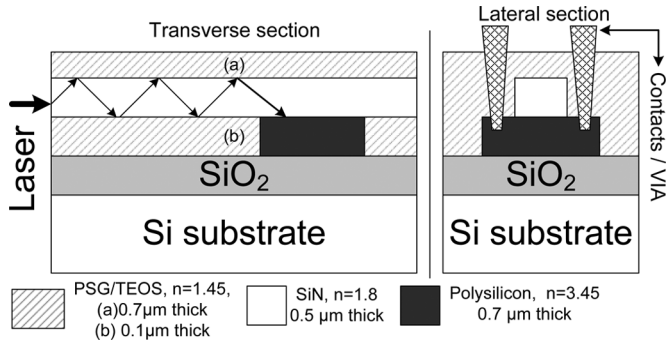

Fig. 3. Traveling wave photo detector.

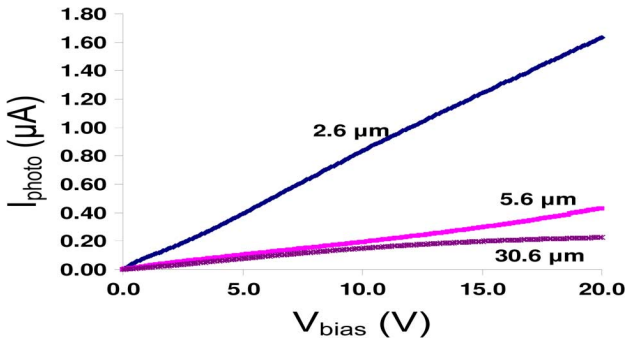

Fig. 4. I-V plot of a photo detector with various contact spacing in the first generation test chip with 5 μW of estimated input optical power.

detector must have high bandwidth and photo sensitivity. Conventional photo detectors such as P-I-N photodiodes have current "tails" (i.e., long temporal response) in their time domain impulse response, effectively limiting incident optical energy switching speed [24]. This behavior is attributed to the thickness of the photo detector and the greater distance between the electrodes and where the carriers are generated within the detector. Conventional photo detector designs therefore are insufficient for optical clock distribution purposes where clock frequencies are high and constantly increasing. A more suitable photo detector should have high speed and fast impulse responses with minimal photo current tail.

Thin polysilicon layer when used as the detector material generates carriers in the high field region with minimal photo current tail. However, a thin polysilicon layer results in low detector responsivity. Thus, a traveling wave or lateral incidence detector (as shown in Fig. 3 [22]) which greatly enhances photo detector responsivity without the need for thick polysilicon layer, is used. Thin polysilicon layer ensures that the carriers are generated close to the contacts (electrodes) greatly improving the response time of the photo detector. Furthermore, for a lateral incidence photo detector with a thin polysilicon layer, the photocurrent has lower dependence on the bias voltage as the carriers are generated close to the contacts and are less likely to undergo recombination. Measured I-V plots of the photo detectors on silicon as shown in Fig. 4 and reported in [21], exhibit quadratic photocurrent gain dependence on contact spacing and a linear dependence on applied bias voltage especially at lateral electric fields above 10 kV/cm.

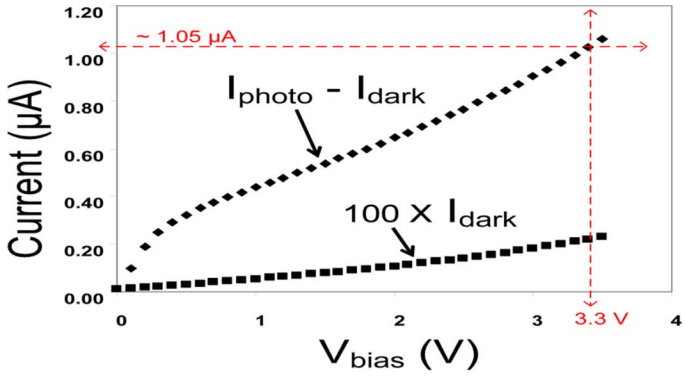

Fig. 5. I-V plot of a photo detector with 2.6 μm contact spacing in the second generation test chip with 5 μW of estimated input optical power.

Optoelectrical (ISE TCAD) simulations indicate that a 0.25 μm thick, 10 μm long polysilicon layer would be sufficient to absorb more than 80% of the laterally incident optical energy. Moreover the refractive index of polysilicon ($n = 3.85$) is higher than the refractive index of silicon nitride ($n = 1.8$), thus permitting leaky-mode coupling from the waveguide core to the polysilicon. The detector polysilicon is the same as the gate polysilicon, but it is masked from gate implantation and silicidation steps in order to provide the desired electrical and optical properties. The detector polysilicon is at the same level (height from bulk) as the gate polysilicon, it is entirely possible to place them at different levels. However, for manufacturing ease the two polysilicon layers are kept at the same level.

The lateral incident photo detector which is placed at the leaf-node of the optical H-tree, when properly biased generates a current pulse for every incident laser pulse. The photo detector initiates the clock recovery process by converting the incident optical clock to current pluses (photo current) which is then processed to generate electrical clock signals for local distribution. Due to the low magnitude of the photo current, it cannot be used directly to drive clock sink nodes. A TIA is used to convert, amplify and condition the photo current to generate rail-to-rail electrical clock signal. The photo detector used in the proposed on-chip optical clock distribution system was implemented on a first generation test chip, characterized and reported in [20] and [25] and the waveguide characterization was performed and reported in [22]. Subsequently, a second generation test chip was implemented integrating electronics into the first generation test chip. Integrating electronics into the test chip required two levels of metal interconnects, this increased the upper cladding thickness of the waveguides, thus, improving optical confinement and photo detector performance. Fig. 5 shows the I-V plot of a 2.6-μm detector in the second generation test chip with an optical input of 5 μW. $I_{\rm dark}$ is the dark current generated by the detector (noise) and the photo current is given by $I_{\rm photo}$ (signal). Note that the generated photo current $I_{\rm photo}$ for the same device and input optical power in the 1st generation test chip (Fig. 4 plot labeled 2.6 μm) is small at 3.3 V which is the supply voltage for the 0.35-μm process. In the 2nd generation test chip, the detector responsivity was improved and measured to be 1.3 A/W. A detailed discussion of the detectors is beyond the scope of this paper and will be presented in [26].

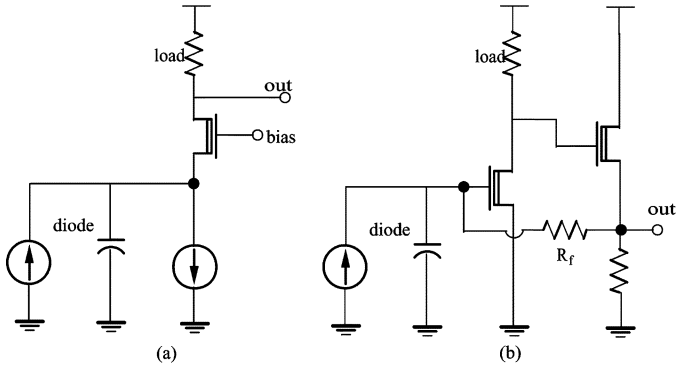

Fig. 6. Conventional TIA designs. (a) Common gate design. (b) Amplifier with feedback resistor.

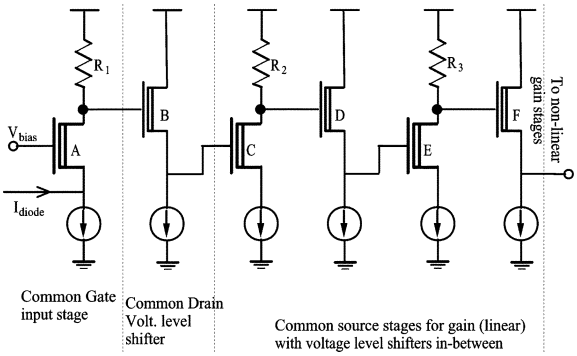

Fig. 7. TiA—Linear part.

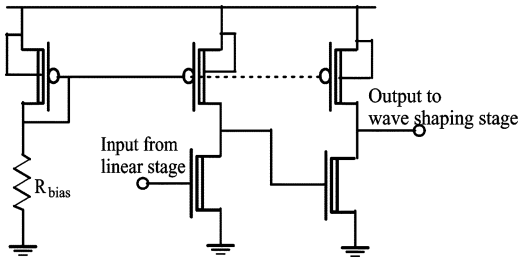

Fig. 8. TIA—BigL nonlinear part.

D. Optical Recovery and Conditioning

TIAs are characterized by their speed, noise sensitivity and responsivity. These characteristics are complementary to each other and are competing design goals often being traded-off during the design process. Conventional TIA circuit topologies, as shown in Fig. 6, comprises of either a common gate input state or a common source stage with feedback.

Common gate topology [see Fig. 6(a)] has high input noise sensitivity, low gain and are typically not used for high speed applications. Compared to GaAs or bipolar counterparts CMOS technology has lower transistor trans-conductance. The common source topology [see Fig. 6(b)], is perhaps the most widely used in GaAs and bipolar technologies. However, in CMOS this topology has large input capacitance (gate capacitance $C_{\rm ox}$) and the interaction between the input capacitor $C_{\rm ox}$ and the feedback resistor R_f increases the circuit's susceptibility to crosstalk noise. This interaction can also causes oscillatory time domain instability and can lower circuit bandwidth. Furthermore, the negative feedback provided by R_f lowers overall circuit gain. Hence for high speed optical clock recovery purposes in CMOS, the common source topology is not suitable. A desirable TIA topology should provide high speed, large bandwidth, low input noise sensitivity and high responsivity to photo current. To achieve all these characteristics in a TIA, a modular approach to the design of the TIA is considered. The proposed TIA topology comprises of a low gain linear analog module followed by a high gain low power nonlinear analog module and a load driving high power digital wave-shaping module. By physically decoupling and isolating the linear and the wave-shaping modules, feedback noise at the input is reduced. Gradual signal amplification improves overall time domain stability and provides for automatic gain control where variations in the input photo current has little impact on recovered output clock signal.

The linear module shown in Fig. 7 forms the front end of the TIA and interfaces the TIA to the photo detector. The linear module consists of a common gate input stage to minimize input resistance and capacitance to improve system bandwidth by shifting the dominant pole further to the higher frequencies. Two common source stages with source followers in-between them are used to boost signal gain. The linear module offers 20 KΩ impedance or 86 dBΩ transimpedance gain in a 0.35-μm CMOS design.

The nonlinear module provides most of the TIA's voltage gain. The robustness of the nonlinear module under process variation is essential to guarantee electrical clock recovery. The nonlinear module's robustness is improved by incorporating two different approaches in its design. The first approach is based on the observation that non-minimum length FETs are more resistant to process variation. Circuit topology based on this observation named "BigL" (shown in Fig. 8), consists of two high gain common source amplifiers in series. The second approach incorporates feedback and self correction elements in the circuit. The second topology named "replica" (shown in Fig. 9) incorporates feedback control and self correction by using replica biasing technique described in [27]. By actively monitoring the DC levels shifts at specific points in the circuit, deviations in circuit behavior due to process variation is identified and corrected [25].

The wave shaping module in Fig. 10, consists of cascaded inverters to drive the clock sink nodes. The input for the wave shaping module is the nonlinear module's output. Increasingly sized digital inverters will condition the nonlinear module's analog output to generate a full rail-to-rail clock signal and drive the clock sink nodes. In the experimental on-chip optical clock distribution system with the 16 leaf-node H-tree, one TIA is assigned to each of the 16 H-tree clock domains. The low pass filter elements in the replica TIA, i.e., the resistor and the capacitor were implemented using FETs. They were implemented as 0.4 μm $\times$ 1.1 μm and 5 μm $\times$ 5 μm FETs (effective W $\times$ effective L), respectively. The BigL and replica TIA area foot prints were 63.38 μm $\times$ 84.12 μm and 77.58 μm $\times$ 85.7 μm, respectively.

1) TIA Simulation Results: The photo detector is modeled as a 0–1 μA pulsed current source with parasitic resistor and capacitor as in Fig. 11. This served as the input to the TIA for simulation purposes.

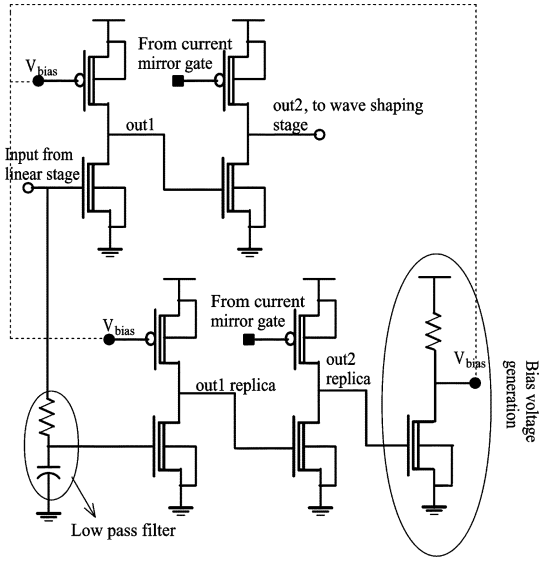

Fig. 9. TIA—Replica nonlinear part.

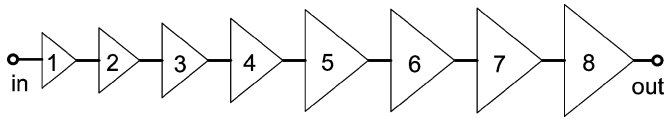

Fig. 10. TIA—Wave shaping part.

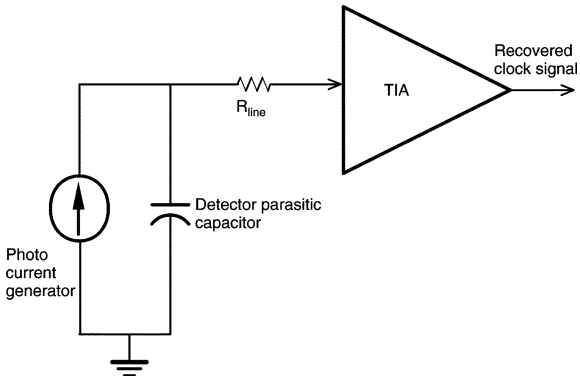

Fig. 11. Photo detector equivalent circuit and TIA.

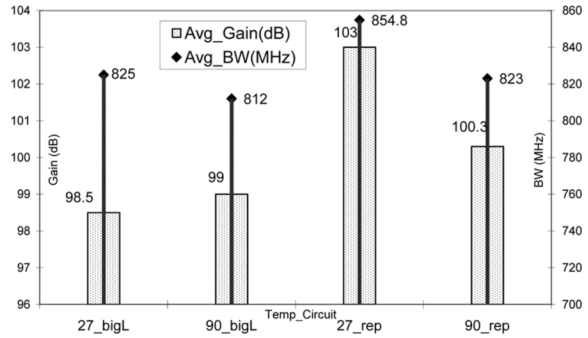

Fig. 12. Bandwidth and gain characteristics of BigL and replica TIAs.

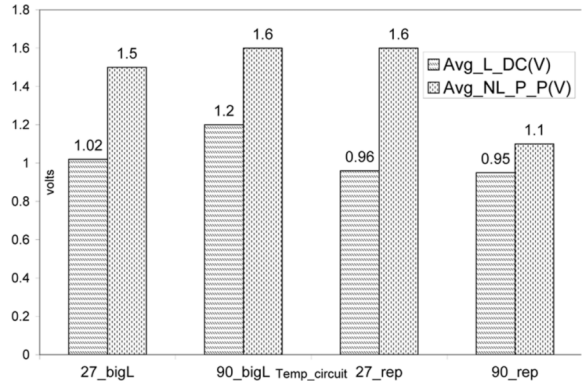

Fig. 13. Transient characteristics of BigL and replica TIAs.

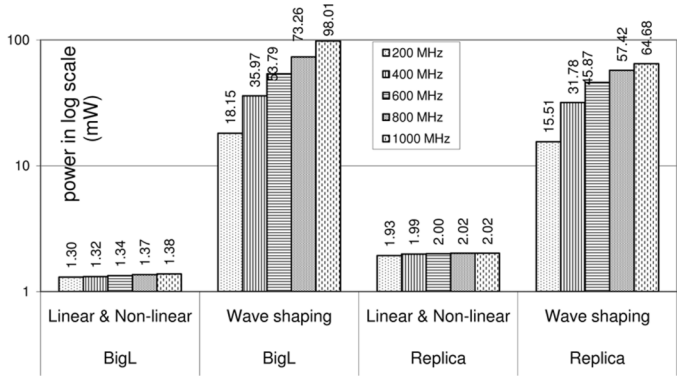

Fig. 14. TIA power consumption at different frequencies.

The two topologies were simulated at two temperature setting, i.e., at 27 °C and 90 °C. SPICE simulation results for average bandwidth and gain for the two topologies at 27 °C and 90 °C are shown in Fig. 12. Linear module's average output DC level (avg_L_DC) and nonlinear module's average output peak-to-peak voltage (avg_NL_PP) for the two circuits at 27 °C and 90 °C are shown in Fig. 13.

Nominal power consumption for the two topologies at five input photo-current frequencies from 200 to 1000 MHz in 200 MHz steps are shown in Fig. 14. Power consumption dependence on input frequency for the linear and nonlinear modules of the TIA is weak unlike the wave shaping module. The wave shaping module which decouples the analog parts of the TIA from the clock sink load downstream helps to improve TIA stability and scalability. Scalability of the TIA is important since the load size does not affect the linear and nonlinear modules of the TIA and ensures proper clock distribution when clock loads are not uniform. Scaling down the wave shaping module when the clock load is smaller will help reduce overall clock distribution power.

TABLE I
MONTE CARLO PROCESS VARIATION SIMULATION SETUP

	Variation range % of nominal value	
Parameter	Random	Systematic
Supply voltage	±3%	-
Photo current	±40%	-
FET width	±5%	±5%
FET length	±5%	±5%
Temperature	±10%	-

The two topologies were simulated for robustness under process variation by subjecting them to Monte Carlo simulations. Extreme conditions for process variation were used to ensure design robustness. For instance, typical variations for channel length and width in a 0.35-μm process were shown to

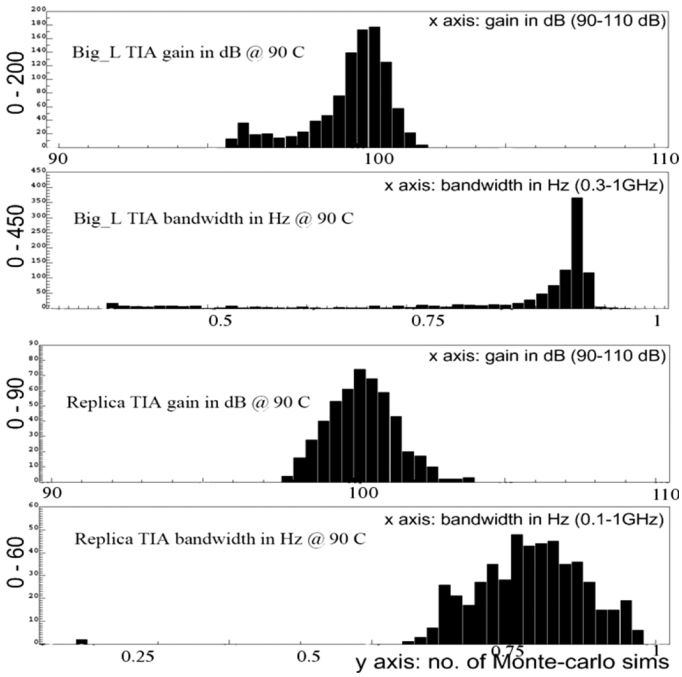

Fig. 15. Monte Carlo gain and bandwidth distributions.

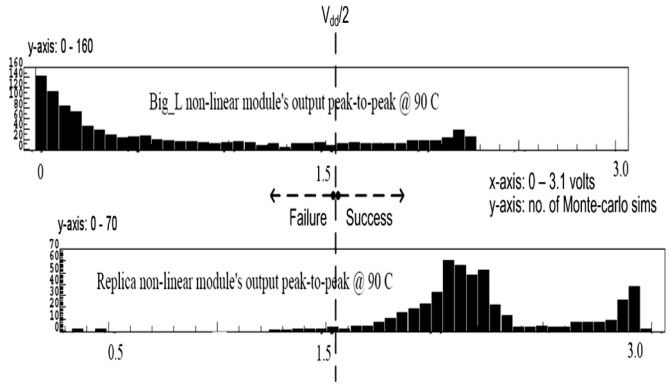

Fig. 16. Monte Carlo nonlinear output peak-to-peak distribution.

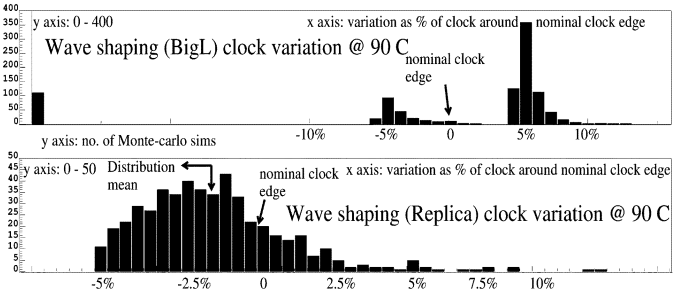

Fig. 17. Monte Carlo wave shaping output clock distribution at 1 GHz.

be between $\pm 4\%$ to $\pm 5.6\%$ [28]. Whereas in our simulations the FET length and width variation were kept at $\pm 10\%$ ($\pm 5\%$ random and $\pm 5\%$ systematic) which results in a more pessimistic performance (skew and jitter) variation. Due to limited silicon samples, such extreme conditions were used during circuit design to ensure sufficient working parts for post silicon test and validation. The operating environment with variations to design parameters is shown in Table I.

Under the conditions in Table I, the variations in AC characteristics including gain and bandwidth were measured. Gain and bandwidth distribution histogram for the two topologies are shown in Fig. 15. Y-axis is the number of Monte Carlo simulations and x-axis is gain in dB for gain histogram and frequency for the bandwidth histogram. Gain histogram is centered around 100 dB and the bandwidth ranges from 0.1 to 1 GHz. These distributions confirm the self correction action of replica TIA, which has fewer "tail" points compared to BigL TIA. Under the same process variation conditions as before, time domain characteristics including nonlinear module's output peak-to-peak were measured. The histogram for the nonlinear module's output peak-to-peak for the two topologies is shown in Fig. 16. X-axis is the voltage and Y-axis is the number of Monte Carlo simulations. Here the effect of self correction by the replica TIA is more evident with fewer failures (peak-to-peak $< (V_{\rm dd})/(2)$) compared to BigL TIA.

The clock variation (skew+jitter) introduce by the TIA in the recovered clock signal under the process variation conditions shown in Table I was estimated and is shown in Fig. 17. Fig. 17 shows the clock variation distribution at the output of the wave shaping stage for the two topologies as a percentage of the clock period. For the operating conditions in Table I, the replica bias TIA output exhibited tighter distribution around the nominal clock edge than that of the BigL TIA. The measured worst case 3σ cycle-to-cycle clock variation for the replica bias TIA was less than $\pm 5\%$ of clock period, i.e., ± 50 ps for 1 GHz clock rate.[1] This is smaller than the estimated worst case optical clock skew of 10% of clock period [10]. Assuming that the device delay is inversely proportional to the device drain current $(I_{\rm ds})$, and taking a more realistic gate length variation for a 0.35-μm process of $\pm 4 - 5.6\%$ [28], when gate length variation is reduced from $\pm 10\%$ to $\pm 5\%$, $I_{\rm ds}$ variation reduces from $\pm 30\%$ to $\pm 15\%$. Therefore under a more realistic process variation, the output variation of the replica bias TIA would scale to be less than 2.5% of clock period.[2] or less than 25 ps without requiring additional clock deskew techniques. While the channel length variations can be brought to a more realistic level for clock variation (skew and jitter) assessment, other parameters such as channel width variation is still beyond a realistic range based on experimental results [28]. Therefore the estimated worst case clock variation in the range of $\pm 2.5\%$ of clock period may still be pessimistic.

Active clock deskewing increases design complexity while using clock grids result in an increase in clock power consumption [29]. Without using active clock deskewing or using clock grids, the worst case clock variation was shown to be $\pm 2.5\%$ of the clock period (i.e., 25 ps in our case). Table II shows the clock skew values (jitter not included) reported for microprocessors. The worst case clock variation (skew+jitter) of the proposed clock network is consistent and comparable to the values

[1]In a typical electrical clock distribution network, an important contributor to skew is interconnect delay variations. However in an optical clock distribution network, the interconnect delay variation due to the optical interconnect is negligible. Therefore the variations of the optical-to-electrical converter/driver, i.e., TIA alone is included in the skew for the optical clock distribution portion of the entire clock distribution network. The clock variations of the downstream (local electrical) clock distribution network is also not included here.

[2]Considering the first-order effects of MOSFETs, i.e., $I_{\rm ds}$ is proportional to device (W/L) ratio and gate delay is proportional to charging/discharging current, $I_{\rm ds}$

TABLE II
CLOCK SKEW NUMBERS FROM MODERN MICROPROCESSORS INDICATING DESKEW TECHNIQUE USED [30], [15], [14], [31], [13]

Author	Source	Deskew	Skew before	Skew after
Gennopoulos	ISSCC 1998	Active	60 ps	15 ps
Rusu	ISSCC 2000	Active	110 ps	28 ps
Kurd	ISSCC 2001	Active	64 ps	16 ps
Stinson	ISSCC 2003	Active	60 ps	7 ps
Pham	ISSCC 2005	Grid	n/a	12 ps
Hart	ISSCC 2005	Grid	n/a	20 ps
Mahoney	ISSCC 2005	Active	n/a	10 ps
Golden	ISSCC 2006	Retiming	n/a	21 ps

in Table II. Although substantial effort has been made to make a fair and thorough assessment of clock performance of the proposed on-chip optical clock distribution network, a complete fair comparison to modern all-electric clock networks is extremely difficult due to the following reasons: 1) the usage of extreme conservative assumptions in the Monte Carlo simulations such as channel length, width and, photo current variations leading to a pessimistic clock variation estimate; 2) the non-availability of detailed design descriptions for large scale clock trees in complex VLSI systems; and 3) only the clock skew component of clock variation has been unambiguously reported in the literature.

E. Impact of Technology Scaling on Optical Clocking System Design

As the test chips were designed in a mature 0.35-μm CMOS process, a natural question is how the integrated on-chip optical interconnect system scale with technology scaling. We attempt to address this question on a component-by-component basis.

1) Optical Clock Source: Technology scaling results in higher clock rates and larger die sizes due to increased levels of monolithic integration. The expected impact of technology scaling on the optical clock source will require higher switching speeds and optical power output for larger dies. The design and monolithic integrating of truly CMOS compatible laser source continues to be a technical challenge. However, heterogeneous integration of III-IV semiconductor laser source remains the most widely used technique for on-chip optical signaling. Concurrently driven laser sources capable of delivering up to 40 mW of optical output power operating over 2.5 GHz have been demonstrated in [32]. As shown in [33] such laser sources can be successfully integrated with CMOS dies in a multi-chip module package. A 18 Gpbs optical interconnect technology was shown in [33]. Hence heterogeneous integration of high power and high speed laser sources for optical clock distribution at rates greater than 10 GHz is technically achievable.

2) Optical Clock Distribution Tree: Optoelectronic clock recovery is an essential part of optical clock distribution. Typically clock networks are hierarchical in nature with distinct global and local distribution sub-networks within the larger clock network. A hybrid approach to optical clock distribution in which the global clock network is optical and the local clock network being electrical was shown in [10]. This design is advantageous from a system power, skew, and jitter perspective due to the explosion in the number of clock recovery station as the optical tree depth is increased. The optoelectronic conversion circuitry is more complex than simple clock buffers and consume more power, therefore a careful tradeoff between global clock power and clock delay, skew, and jitter budgets are necessary; especially in nanometer CMOS technologies.

In nanometer CMOS, processing tolerances are typically well controlled. By constructing the optical components such as waveguides and detectors using standard CMOS materials that exist and are well controlled in nanometer technologies, no additional processing limitations are expected when using the described design in advanced technologies. With technology scaling, device source and drain diffusion sizes decrease. Smaller devices are more prone to optically-induced charges that are generated when these devices are placed within a critical distance from the waveguides. The optically-induced charges which cause circuit malfunction are generated due to evanescent power coupling from the waveguide to the bulk and optical energy scattering from the waveguide. A simple method to prevent this situation requires an "exclusion zone" around the waveguide where no devices are to be placed.

The induced currents from both evanescently coupled and scattered light may be related to the rates of power loss in the waveguide associated with each process. To calculate the exclusion zone width for scattered light, the relationship between the power carried by the waveguide (P_{WG}), the waveguide loss coefficient due to scatter (α_s), logic cell length parallel to the waveguide axis (L), cell width perpendicular to the axis (W), lateral offset of the cell center from the waveguide (X), vertical distance from the waveguide core down to the silicon (D), and the optically induced current in the logic cell I_{op} are considered. The configuration used to calculated the exclusion zone dimension is shown in Fig. 18. Although scattering at each point along the waveguide would be expected to be moderately isotropic in three dimensions, the approximate cumulative effect of a straight waveguide region with any reasonable value of $\alpha_s \ll 1/\mathrm{L}$ can be modeled by assuming scattering from each infinitesimal length of waveguide is 2-D into a plane perpendicular to the waveguide axis. The total power lost from the waveguide over the length of the cell is P and is given by (1) [34]. Equation (1) can be simplified as $P \simeq P_{\mathrm{WG}}\alpha_s L$

$$P = P_{\mathrm{WG}} \times (1 - e^{-\alpha_s L}). \tag{1}$$

Based on geometrical considerations, the fraction of this scattered power that is incident on the cell is $\eta = (\Phi 3)/(2\pi)$ which approaches its maximum possible value of 0.5 only when $X < W/2$ and $W \gg D$, i.e., a large cell is close enough to the waveguide to intercept almost all of the light that is scattered down. The resulting induced photocurrent due to scatter is $I_{\mathrm{ops}} = \mathrm{R}\eta\alpha_s \mathrm{L} P_{\mathrm{WG}}$; where R is the effective responsivity of the silicon cell junctions acting as photodiodes and in no case can exceed $R_{\max} = \lambda/(1.24\ \text{eV-}\mu\text{m})$ at any wavelength λ, or 0.55 A/W at the 685 nm wavelength used in this work. For a square die of edge length d, the first branch of the H-tree has length $d/2$, while the second and third branches have length $d/4$, the fourth and fifth branches have length $d/8$, and so on. Therefore, the upper bound for the total H-tree length will be $3d/2$. Given the power required at each H-tree leaf-node, i.e.,

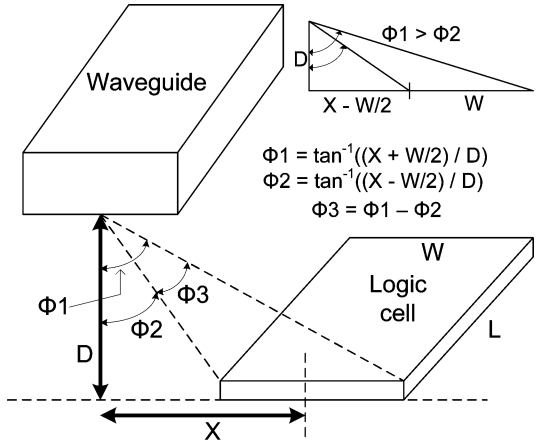

Fig. 18. Setup for exclusion zone calculations.

$P_{\rm node}$, the required input power $P_{\rm in}$ at the root of the H-tree can be calculated from (2)

$$P_{\rm in} = nP_{\rm node}\left[10^{(\frac{\alpha_s}{10})\frac{3d}{2}+(\frac{\chi}{10})log_2 n}\right] \quad (2)$$

where n is the number of H-tree leaf-nodes, α_s is the waveguide loss in dB/cm, d is the die edge in cm and χ is the excess loss at each split in dB, assuming each split divides the optical power equally.

Consider a 10 μm $\times$ 10 μm logic cell placed 0.655 μm (processing distance between SiN and polysilicon) below the waveguide (D) and offset from the center of the waveguide by 5 μm (X). Using 8 dB/cm waveguide loss and 2 dB/split splitter excess loss, the input optical power required for a 128 node 2.5 cm long H-tree is 250 mW. These loss numbers were experimentally ascertained from the test chip and are large (as explained in Section IV-B3) and result in large input optical power requirement and lends itself to performing worst case estimation. For the logic cell under consideration, based on the geometry $\eta = 0.24$. Thus, 24% of the power scattered out of the waveguide in the length of the cell is incident on the cell. For 250 mW input optical power with a loss of 8 dB/cm, the power incident on the cell is 111 μW. Using the cell's theoretical maximum responsivity of 0.55 A/W, this intercepted power will result in 61.2 μA of photo induced current $(I_{\rm ops})$, or 6.12 fC of unwanted photo generated charge for a 100 ps recovery time.

In the case of evanescent coupling of light from the waveguide to the silicon substrate, the same expressions used for scattered light apply except that the coupling efficiency is taken to be unity, $\eta = 1$, if only the substrate loss of the waveguide is considered. Based on commercial beam propagation method simulations, the imaginary part of the effective modal index of the waveguides described in this paper at a distance $D = 0.655$ μm above the silicon is found to be 9.45 $\times$ 10–7 which corresponds to an effective absorption coefficient of $\alpha_e = 0.173$ cm^{-1} at 685 nm wavelength. Thus, the maximum photo induced current due to evanescent field coupling $(I_{\rm ope})$ from the waveguide to a 10 μm long cell directly under the waveguide is given by $I_{\rm ope} = R_{\max}\alpha_e L P_{\rm WG}$ and evaluates to 24 μA. The photo induced current due to evanescent field coupling in a cell offset to the side would be less. Combining the photo induced current due to evanescent field coupling (24 μ) and photo induced current due to evanescent scatter (61.2 μA) gives a total photo induced current of 85 μA or 8.5 fC of photo generated charge for a 100 ps recovery time. Therefore if the $Q_{\rm crit}$[3] specification for a design is 10 fC/100 ps or less [36], [37] then an exclusion zone of 5 μm or less, respectively, around the waveguide will be necessary.

Using a more reasonable waveguide loss values of 1 dB/cm and 1 dB/split splitter loss, the input power for a 128 node 2.5 cm long H-tree is 1.1 mW [Section IV-B(6)] and the total photo induced current in the considered logic cell is 0.006 μA or 0.006 fC for a recovery period of 100 ps. Therefore for a $Q_{\rm crit}$ specification of 10 fC/100 ps there will be no need for any exclusion zones around the waveguides. Improvements in waveguide loss and excess splitter loss would reduce not only the required input power but also the size of the exclusion zone. The optical energy in the optical h-tree will vary from the root to the leaf-nodes due to splitting and waveguide loss. Therefore the exclusion zone dimension (if they are necessary) will be nonuniform and larger at the root where the optical energy is maximum and more likely unnecessary beyond the first or second split. Exclusion zones result in additional area overhead and layout constraints in the form of additional design rule checks for minimum clearance between the waveguide and diffusion layers. Additional custom design rules that are not part of standard design rules and custom GDSII layers will be needed in order to ensure manufacturability. Additional design rules and custom GDSII layers needed are likely to increase with scaling. Design of the two test chips with additional rules for manufacturability has shown that modern EDA tools are capable of handling the increased complexity.

3) Photo Detectors: For the photo detector design described in Section II-C, technology scaling would lead to a decrease in drawn polysilicon width (L) and contact spacing across it. Detector photo responsivity is inversely proportional to L, therefore for a given bias the detector responsivity should improve with scaling. Moreover the detector bandwidth and photoconductive gain product, which is inversely proportional to L is also expected to improve with scaling.

4) TIA Architecture: Output resistance of transistors in saturation will decrease with scaling into nanometer CMOS. As a result the TIA gain will decrease, however device transition frequency and hence TIA bandwidth will increase. TIA architectures in nanometer CMOS will be modular in nature and similar to the architecture described in Section II-D. With each technology node, suitable modification to the front end linear module will be necessary to maximize bandwidth. Additional gain stages, i.e., more than one nonlinear module may be needed, depending on gain-bandwidth-power-area tradeoffs. The design of the wave shaping module, i.e., the standard inverter chain should be straightforward depending on clock load. While the circuit designs in 90 and 65 nm have been demonstrated in [33] and [38]–[41], respectively, circuit topology will change in 45–22 nm range given the significant reduction in headroom and deteriorating transistor output characteristics. The basic modular nature of the TIA design is

[3] $Q_{\rm crit}$ is defined as the minimum amount of charge that must be collected by a circuit, due to an extraneous event causing charge generation at a sensitive node, in order to change the state of the circuit [35].

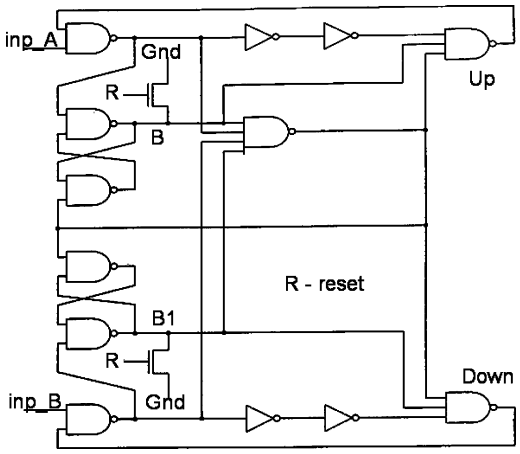

Fig. 19. Phase comparator circuit schematic.

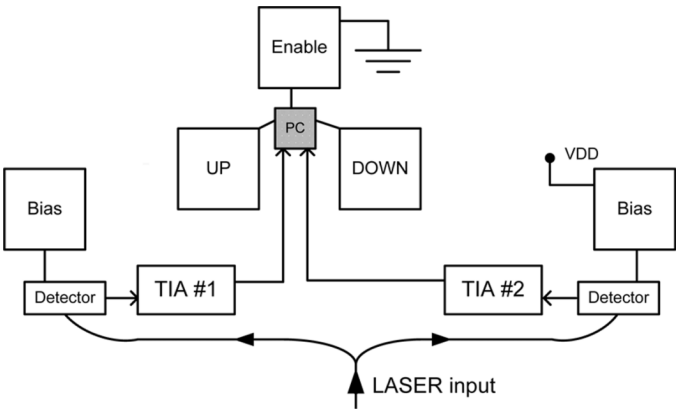

Fig. 20. Test setup for testing the clock recovery system.

more likely to be carried over to designs in advanced CMOS technologies and we foresee an increase in the number of TIA stages to compensate for the reduction in gain increasing power consumption of the optical-electrical design. However, the overall clock distribution power of an all electrical system also increases with scaling as more and more design opt to implement full-blown grid-style designs to reduce skew and jitter. Such a comparison is really out of the scope of this paper, due to lack of data.

III. Test Circuits and Test Architecture

There are several optical H-trees on the die, the main H-tree, which has 16 leaf-nodes is used for testing purposes. At all H-tree leaf-nodes a photo detector, its bias pad and a TIA are present to recover the electrical clock signal form the incident optical clock. A set of phase comparators (PC) are placed at appropriate locations along the chip to compare the phase of the recovered clock signals. The output of a TIA is shielded on either side by ground wires and routed to an appropriate PC. Fig. 19 shows the circuit schematic of the PC used to compare the phase of the recovered clock signals from two different leaf-nodes and the corresponding test setup is shown in Fig. 20.

In this setup, the TIA output cannot be directly probed. In order to test the TIA and probe its output, additional test structures were implemented. The TIA test structure shown in Fig. 22 consists of a ring oscillator (RO) circuit and a voltage-to-current

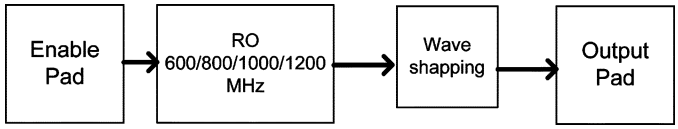

Fig. 21. Test setup for testing the RO.

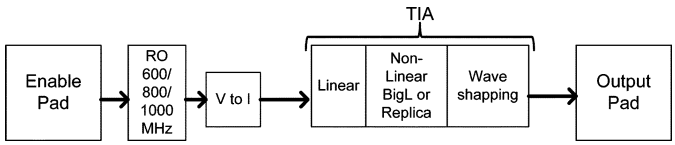

Fig. 22. Test setup for testing the TIA.

conversion circuit to trigger the TIA. "Enable" and "Output" pad pairs are used to enable the RO to initiate oscillations to trigger the TIA and to observe the TIA's output, respectively. A similar test structure with just the RO and wave shaping module is use to test the RO themselves, shown in Fig. 21. The ROs were designed for 600, 800, 1000, and 1200 MHz, only the former three are used to trigger a TIA in the test structure.

IV. Experimental Results

Fig. 23 is the die image of the second generation test chip fabricated in a 0.35-μm CMOS process utilizing two metal layers and a 3.3 V supply. The test chip is 9409 μm $\times$ 9029 μm in size. The edges of the chip was polished back to expose the edge of the waveguides to allow for optical edge coupling into the waveguides.

When designing an optoelectronic system, it is important to perform a link budget analysis, to determine if the desired goal can feasibly be obtained from the available inputs and components. For this system, the TIA design spec is 1 μA of photocurrent. With an estimated detector responsivity of 1 amp/watt, waveguide loss of 8.5 dB/cm and splitter loss of 2 dB/split, the detectors need to receive 1 μW, or -30 dBm, of optical power. From the die edge to each leaf node, the waveguide has four splits and is 0.8335 cm long resulting in 27 dB loss. Neglecting external fiber losses, the laser diode will inject -3 dBm, or approximately 500 μW into the die.

A. Experimental Results

Figs. 25 and 26 show the mean of the observed RO output peak-to-peak amplitude and frequency of oscillation of the RO test structures on the chosen wafer at different supply voltages. Clearly the observed performance was well below the design point, mainly due to a parasitic element value estimation error, which led to underestimation of the circuit parasitic elements, wire, and pad parasitic values. This resulted in the circuits being considerably undersized compared to the load size. Fortunately this error had no impact on the optical components and allowed the completion of design validation of the test circuits.

Fig. 27 shows the oscilloscope screen capture of the output of the 1200 MHz RO on a test die. When the enable signal is low the RO is enabled and the oscillations are observed. The zoomed in screen capture shown in Fig. 28 shows the peak-to-peak voltage measured to be 2.138 volts and the frequency to be 223.46 MHz.

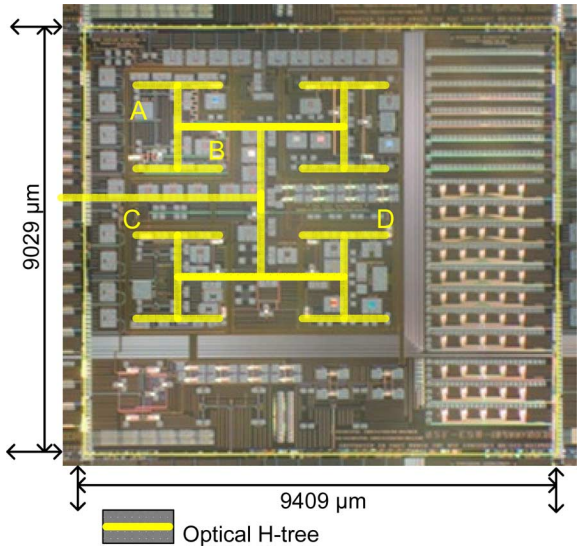

Fig. 23. Second generation test chip fabricated in a 0.35-μm process.

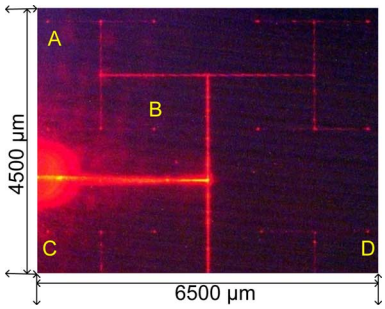

Fig. 24. Prolonged exposure image showing main H-tree lit up.

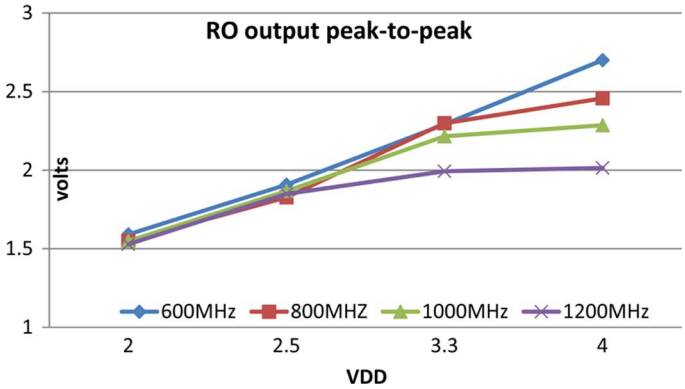

Fig. 25. Mean RO output peak-to-peak.

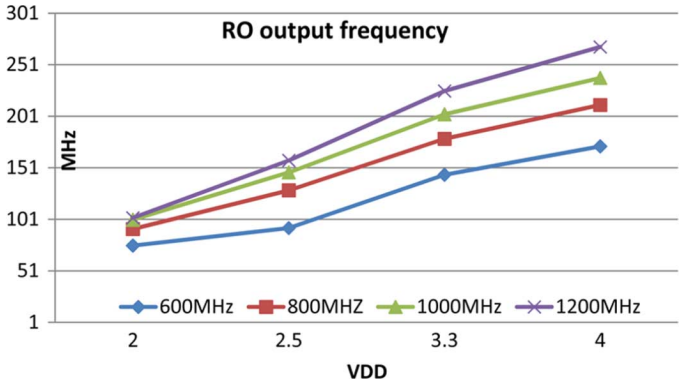

Fig. 26. Mean RO output frequency.

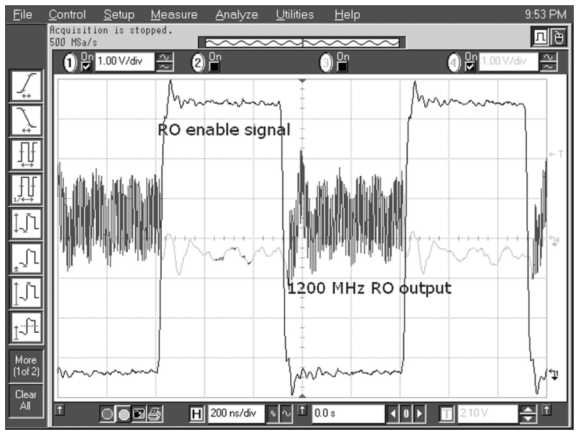

Fig. 27. 1200 MHz RO output capture showing enable signal and RO response.

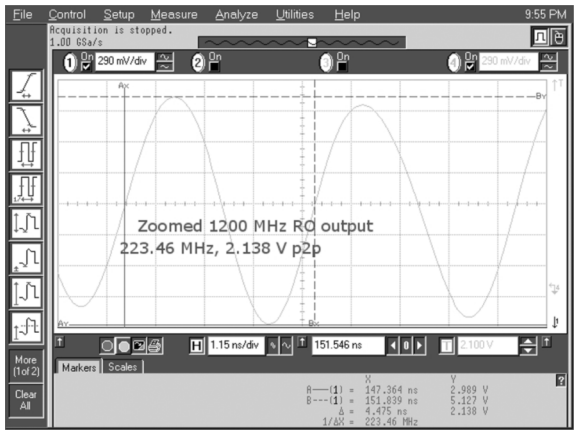

Fig. 28. Zoomed RO output, measurement details as labeled in figure.

Fig. 29 shows the oscilloscope screen capture of the output of a Replica TIA driven by a 1000 MHz RO. When the enable signal is low the RO is enabled, triggering the TIA and the oscillations of the TIA are observed. Fig. 30 shows the same signal but for a BigL TIA. The mean frequency and peak-to-peak for the Replica and BigL TIA measure are shown in Figs. 32 and 31, respectively.

Testing the clock recovery system involves the setup of the optical input as in Fig. 20. The output of the PC is probed at the "Down" pad. To test the clock recovery system a PC is chosen, then one of two inputs needed for the PC is set to be a recovered clock signal from a TIA at the end of the main H-tree with its detector bias pad tied to power supply (3.3 V). The second TIA station's detector bias is on-off (0–3.3 V) modulated. Applying a bias on the second detector produces a recovered clock with a phase difference compared to the constant clock. This should produce a sharp pulse at the PC output pad, in this case the "Down" pad. The circuit parasitic element estimation error and the underestimation of pad load, led to performance degradation of the PC; therefore the input laser's switching frequency was deliberately kept low.

Fig. 33 clearly shows no PC response when the laser is turned off. However when the laser is on, as shown in Figs. 34 and 35 the PC responds when the second detector is biased (the first

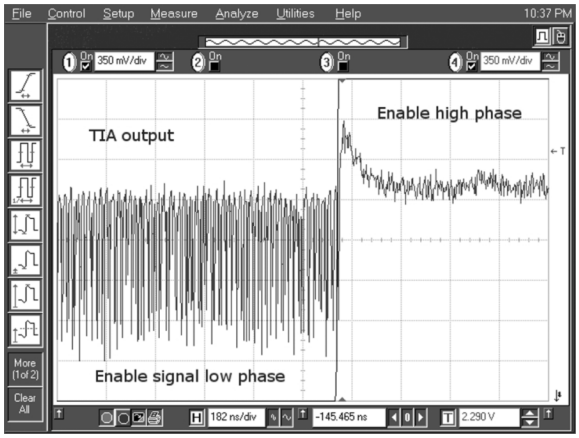

Fig. 29. 1000 MHz RO and Replica TIA output capture showing enable signal and TIA response.

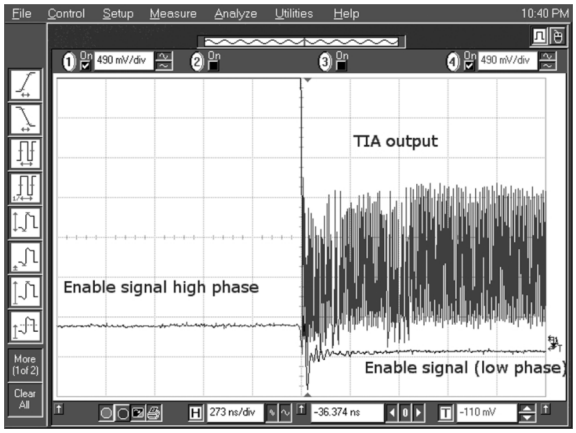

Fig. 30. 1000 MHz RO and BigL TIA output capture showing enable signal and TIA response.

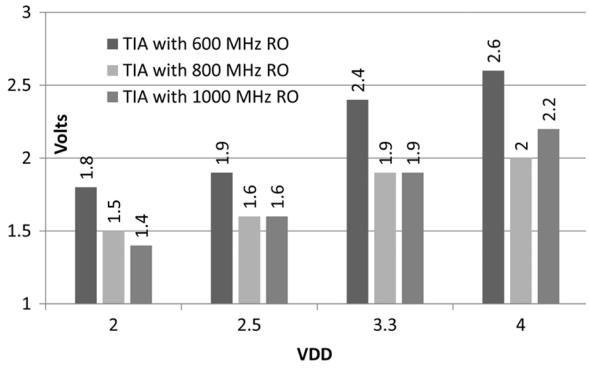

Fig. 31. Mean TIA output peak-to-peak.

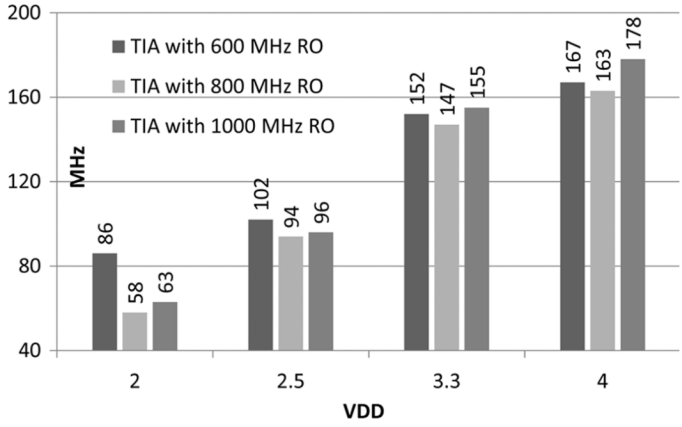

Fig. 32. Mean TIA output frequency.

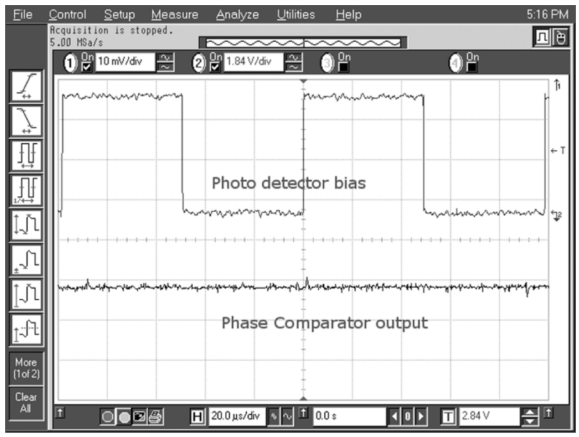

Fig. 33. PC output with no laser input.

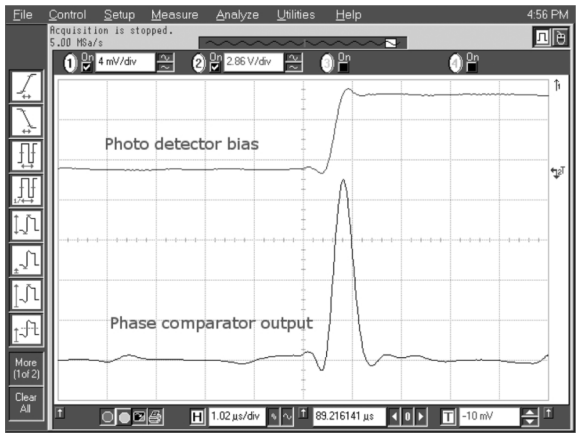

Fig. 34. PC output with 10 kHz laser input.

detector bias pad is tied to power supply, producing a constant recovered clock signal). The PC responds by producing a pulse corresponding to the phase difference and quickly settle down as expected.

B. Observations, Comments and Summary

1) The experimental results confirm the integrity of the optical clock distribution system, the desired functionality of the optoelectronic components and their interfaces. The entire on-chip system for optical signalling can therefore be made truly CMOS compatible and still deliver satisfactory optoelectronic performance.
2) Overall performance of the experimental system, in terms of speed, is marginal, however the functionality and feasibility of the system has been verified through the experiments performed on the system albeit at low frequencies.
3) Waveguide loss results were measured to be between 8 and 9 dB/cm. This was much higher than expected, and much higher than other values reported in the literature, which

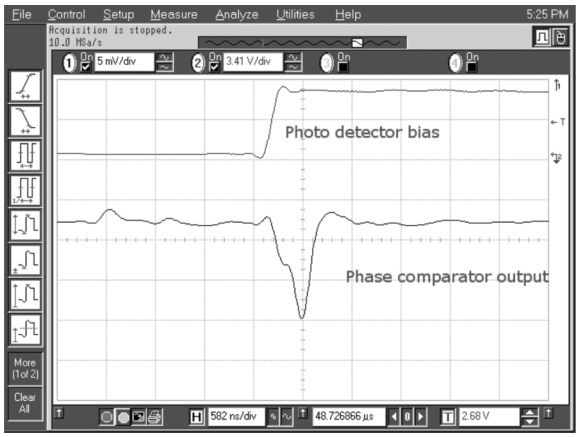

Fig. 35. PC output with 100 kHz laser input.

are typically below 1 dB/cm. Investigation revealed an unexpected loss mechanism caused by high absorption in the PSG layer which formed part of the lower cladding. As pointed out in Section II-C placing the detector polysilicon higher than the gate polysilicon will lead to moving the waveguide core (SiN and subsequent layers above) higher as well to ensure optical coupling and increasing the lower cladding thickness. However moving the detector polysilicon higher will result in two types of level-1 contacts, i.e., "taller" contacts to gate polysilicon, source and drain of devices, and a "shorter" contact to the detector polysilicon which is at a higher level. Lithographically additional masks to differentiate the two contacts are needed, consequently contact etch has to be performed in two stages. The two polysilicon layers are currently differentiated by the salicide block layer, therefore no new masks are needed. However polysilicon deposition will become a two stage process and a new field oxide layer has to grown and planarized that lies in between the two polysilicon layers. Furthermore the TIA's bandwidth will be reduced due to additional parasitic resistance and capacitance in the photo-current path between the detector and the input of the TIA. Therefore by moving the detector polysilicon higher and altering the thicker lower cladding composition can decrease the unexpected optical loss in the cladding. However there is a tradeoff between optical loss, manufacturing cost, variability, and TIA performance, this relationship has to be investigated further. Here both the polysilicon layers are assumed to be below the first metal layer. The detector polysilicon can also be place higher than the first metal layer. A complete discussion of this scenario is beyond the scope of this paper.

4) The optical splitters used in the H-tree were sources of additional loss and nonuniform energy split between the two branches. Analysis and design optimization of splitters will be addressed fully in more detail in [26].
5) Detector speed, as well as overall performance, was limited by the performance available from the 0.35-μm CMOS process. While producing test samples in the process was relatively inexpensive, the "trailing edge" nature of the process limited the overall performance available. Detector speed could be enhanced by implanting the polysilicon with electrically inactive species to damage the polysilicon and reduce the carrier lifetime [42]. As long carrier lifetime enhance the photoconductive gain mechanism mentioned earlier, a reduced lifetime would results in lower current response. Since the photoconductive gain mechanism is also inversely proportional to the square of the contact spacing, the effect of lower lifetimes could be alleviated by smaller contact spacing, or possibly by electrical circuitry which had lower drive current requirements. Lithographically, doping the detector polysilicon will result in modifications to the current process flow and introduce an additional implantation step.
6) In order to motivate the need for on-chip optical clocking system and provide a more meaningful comparison between an optical and an electrical clocking system, data from recently published examples are used. The power consumption measurement from the test chip could not be obtained due to the following two reasons. One, the performance of the test chip is well below the design point and the technology is outdated. Two, the power consumption of the main H-tree could not be measured individually. In order to minimize supply noise all analog devices on the chip were powered by a single analog power grid and all digital devices were connected to a digital power grid. Furthermore, to minimize the number of probes required to test the chip, most test structures were designed to be enabled by default.

The second generation test chip discussed in this paper was designed to verify the functionality of the entire optical clock distribution and recovery system, not per component power consumption. We believe that the lack of measured power consumption data on silicon does not diminish the novelty of demonstrating a fully CMOS compatible on-chip optical interconnect system using on-chip clock distribution as its main application.

However to better understand the impact of power consumption of future on-chip optical clock distribution system, let us analyze it by assuming that the hierarchical electrical clock network in [31] is to be hybridized, i.e., clock routes L0 and L1 are replaced with their optical equivalent. The equivalent optical H-tree for L0 and L1 routes will have seven levels of splits and will be 25 mm long from root to leaf nodes. Although the test chip exhibits high loss (8 dB/cm waveguide loss and 2 dB/split excess loss), better waveguide loss is obtainable based on other published results in the literature. The feasibility of less than 1 dB/cm waveguide loss and less than 1 dB/split excess loss has been demonstrated [43]. To perform a realistic comparison in power consumption, 1 dB/cm waveguide loss and 1 dB/split excess loss are used. In such a case, and with the required input photo-current of 1 μA at the leaf nodes and detector responsivity of 1 A/W; the required optical power into the H-tree is 1.1 mW. Assuming a laser and coupling efficiency of 10%, the total optical power is 11 mW. With seven levels of splits, there are 128 H-tree leaf nodes. However, the number of L0 and L1 route terminations are 85 $(14 + 71)$. Therefore placing TIAs at 85 leaf nodes for clock recovery is sufficient. To calculate the power consumed by the TIAs, measured power efficiency of 8.1 mW/(Gb/s) [38] and receiver power contribution of 45% [38]

are used. The design in [38] is in a 90-nm CMOS technology similar to [31]. The rated clock in [31] is 2.5 GHz, therefore the power consumption for one TIA at 2.5 GHz will be 9.1125 mW, i.e., 8.1 * 2.5 * 0.45 (receiver contribution from [38]). Therefore the total power for 85 TIAs will be 775 mW. The total power for the optical equivalent clock network will be $775+11=786$ mW.

Taking an all-electric clocking system in 90-nm design [31] as an example, the total power consumption for L0 and L1 routes is 1300 mW. The equivalent optical clock network with waveguide loss of 1 dB/cm and 1 dB/split consumes approx 40% less power than its electrical (L0 and L1) counterpart. For the same optical clock network if the waveguide losses were worsened and were around 2.5 dB/cm and 2 dB/split, the power consumption of the optical clock network still has a 30% advantage over the all-electric counterpart. Moreover in the electrical clock network due to interconnect limitations, two phase differential half frequency clocks are necessary to regenerate a full swing clock signal which is then multiplied to generate a full rate full swing clock signal for further distribution [31]. Differential two phase clock distribution is not necessary in case of the optical equivalent clock network. Compared to the electrical L0 and L1 clock network, there are fewer differential amplifiers and repeaters in the optical equivalent which reduces the potential sources for clock skew, jitter and delay. Therefore, replacing the first two stages of the clock distribution network in [31] with their optical equivalent results in lowering global clock power and reduces design complexity while still delivering same or better downstream clock performance. A generic optical clock distribution system with optimal optical tree depth will have fewer electronic components (sources of jitter, skew and delay) in the clock signal path, compared to an all electrical clock distribution system, thus, minimizing absolute clock jitter, skew and delay, and potentially obviating the need for the expensive and complex active clock de-skew system while retaining comparable performance.

V. Conclusion

Nanometer CMOS technologies have necessitated a better interconnection technology, as long global interconnects have been shown to be a design bottleneck. Optical interconnect technology is a potential alternate to traditional interconnects and has immense potential to improve interconnect delay, clock skew, jitter and have better signal integrity. The keys to successful adaptation of on-chip optical interconnects are ease of integrating optical components into standard CMOS manufacturing and manufacturing cost. The work presented in this paper attempts to integrate individual components to demonstrate a truly CMOS compatible optical clock distribution system and enable successful adoption of on-chip optical interconnects. The proposed optical clock distribution system and clock recovery components were implemented on silicon as a test vehicle in a mature 0.35-μm CMOS process for feasibility analysis. Although many aspects of the test circuit designs can be further improved, experiments on the test chip has established the feasibility of the proposed approach and the overall system functionality. Encouraged by ongoing work on individual components both here and elsewhere, despite steep design improvements needed, we see no fundamental challenges in successfully implementing the design presented here in advanced nanometer CMOS technologies that require greater that 10 GHz clock rates.

Acknowledgment

The prototype chip presented in this paper was manufactured by Avago Technologies. The authors would like to express their gratitude for their generous support for this project.

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