

Waveguide Coupled CMOS Photodetector for On-Chip Optical Interconnects

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Abstract – A novel, truly CMOS compatible, waveguide coupled, high-speed photodiode for on-chip optical clock distribution is designed using analytical calculations, electro-optical simulations, and experimental analysis. Experiment and simulation results from test devices are presented and analyzed. Results from test devices and waveguides currently under fabrication in the Agilent 0.35 μm CMOS process will be reported.

I. INTRODUCTION

On-chip electrical interconnects for global signals will increasingly become a bottleneck as CMOS scaling continues. Optical interconnects can present an attractive alternative if they can be made CMOS compatible, including being planar (monolithic) and using materials already present in the CMOS process. Free space optical interconnects have been demonstrated for inter-chip communication [1] but they would require expensive processing and careful alignment for intra-chip communications. CMOS compatible waveguides and photodiodes have been demonstrated for on-chip signal routing [2], although a high speed, high responsivity CMOS compatible photodiode has not yet been realized.

II. WAVEGUIDE in CMOS

The waveguide is formed with a core of silicon nitride, which is normally used for copper encapsulation, and a cladding is formed from dielectric layers used between metal layers in a CMOS integrated circuit. Light is routed using typical waveguide components like bends and splitters. The light is then coupled into a photodiode.

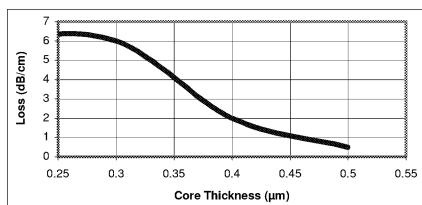


Fig. 1 Waveguide loss Vs. Core thickness for a Silicon Nitride core with low-k dielectric as cladding

Optical simulations were performed using beam propagation and FDTD methods; in order to determine the thickness of the

core and cladding required to sustain a single optical mode in the waveguide. Mode number calculations indicate that a core thickness of 0.5 μm is sufficient to sustain a single optical mode in the waveguide Fig. 1 shows that there would be a 0.5 dB/cm loss for a 0.5 μm core thickness, which is tolerable in this case as the entire link is a few centimeter long.

III. DETECTOR in CMOS

One of the most important requirements of the photodiode, in addition to being CMOS compatible is high bandwidth. The carriers generated away from the electrodes give rise to the increased current tail in the impulse response of the planar P-I-N photodiode in [2], thereby limiting its speed. In order to achieve high speed the use of a thin silicon layer as detector is essential to ensure that only carriers generated in the high field region contribute to the photocurrent. However, a thin silicon layer results in low responsivity for normal incidence devices. Thus there is a trade off, and a device that meets both the photoresponse and high speed requirements needs to be designed. Normal incidence Metal-Semiconductor-Metal (MSM) photodiodes made in polysilicon have been found to have good responsivity at 860 nm [3] with a 2 μm layer of polysilicon. The use of a thinner ($<0.5 \mu\text{m}$) polysilicon layer was found to greatly reduce the photoresponse but resulted in a much higher operating bandwidth [4]. The use of waveguide coupling would offer greater light confinement and lateral light incidence would result in more absorption, which would enhance the photoresponse, as the light would encounter more detector area along its direction of propagation.

A. Traveling Wave Detector

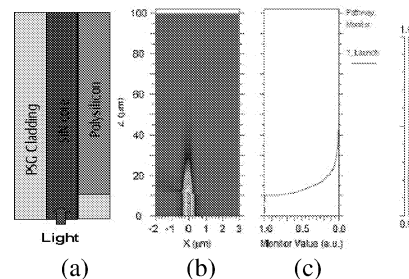


Fig. 2. Optical Simulation of the waveguide coupled photodiode. (a) Device structure used for simulation (b) Color contour for the light intensity. (c) Normalized plot of the light intensity in the waveguide as a function distance traveled over the polysilicon

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Traveling wave detection or lateral incidence would greatly enhance the photoresponse without the need for a thick layer of polysilicon. Simulations indicate that a 0.25 μm thick and 10 μm long polysilicon layer would be sufficient to absorb more than 80% of the incident light, as shown in Fig. 2. The 0.25 μm thick polysilicon ensures that the carriers are generated close to the contacts thus greatly improving the time response of the photodiode. Electro-Optical (ISE TCAD) device simulations indicate that the responsivity increases by a factor of 100 with lateral light incidence as seen in Fig. 3. The photocurrent for lateral light incidence shows less dependence on the bias voltage, this is due to the fact that most of the carriers are generated close to the contacts where they are less likely to undergo recombination. Preliminary impulse response simulations indicate a 3-dB bandwidth of about 10 GHz. Measurement results from devices currently under fabrication in the Agilent 0.35 μm process will be presented.

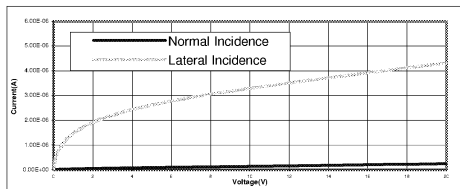


Fig. 3. Simulated response at lateral and normal light incidence of a 10 μm contact spacing photodiode, at 200 μW of 780nm incident light

Polysilicon photodiodes were fabricated and tested in order to understand the electrical properties of polysilicon, and the effect of polysilicon thickness on the photoresponse.

B. Polysilicon Metal-Semiconductor-Metal Photodiodes

MSM photodiodes with 100 μm X 100 μm active area and 5 μm finger spacing were fabricated on 0.25 μm and 1.6 μm thick polysilicon, and Ti (25 nm)/Au (150 nm) was deposited to form the contacts. Table 1 shows the measured responsivity of these devices along with the calculated values of responsivity. It can be seen that the measured responsivity increased by a factor of 10 when the thickness changed from 0.25 μm to 1.6 μm as expected.

TABLE I
Measured and calculated responsivity for MSM photodiodes for a wavelength of 780 nm and normal light incidence

Thickness of polysilicon	0.25 μm	1.6 μm
Measured Responsivity	2.74E-04A/W	3.62E-03A/W
Calculated Responsivity	12E-03A/W	80E-3A/W

The measured responsivity of these devices was less than the calculated responsivity and was bias voltage dependent. This is due to recombination in the defect states at the grain boundaries in polysilicon [5]. Annealing in hydrogen plasma at high temperatures significantly reduces the density of defect states and the grain boundary potential barrier [6]. All CMOS circuits undergo a similar type of annealing process and in

order to test the effect of annealing some of the test devices (currently under fabrication) will be annealed and others that are not annealed will also be tested and results will be presented.

C. Polysilicon Schottky Barrier Photodiodes

Schottky barrier photodiodes similar to the CMOS photodiodes currently under fabrication were fabricated on 1.6 μm thick Polysilicon. The devices had two 100 μm X 100 μm contacts of Ti (25 nm)/Au (150 nm) 10 μm apart on the polysilicon. Titanium was used as the contact metal because it has a work function similar to that of tungsten. Tungsten, which is used as a contact via in the CMOS process, is the contact metal in the test chip currently under fabrication. The simulations were performed using a similar device structure and geometry.

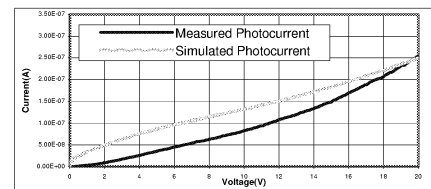


Fig. 4. Measured and Simulated photoresponse of a 10 μm contact spacing Photodiode, at 200 μW of 780nm incident light.

There is a good agreement between the measured data and simulations as seen in Fig. 4, indicating an accurate simulation model.

IV SUMMARY

We have designed a CMOS compatible waveguide optical interconnect system, with waveguides and photodetectors on a single chip. TCAD simulations indicate a responsivity of 0.053 A/W and a 3-dB bandwidth of approximately 10 GHz. We will report results from waveguide coupled photodetectors, and waveguides currently under fabrication.

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