signal 2 before switching, now after rearranging the correlators the data bearing signal 3 will be fed to the demodulator (signal D). The corresponding dashed S curve is shown in Fig. 2b where the old equilibrium point R has moved to the right

By using the ACTL with three correlator arms shifted relative to each other it is possible to track a PN code subject to Doppler effects. Owing to the periodic discriminator characteristic these effects are taken care of by an adaptation of the arms whereas the channel noise can be suppressed by a narrower loop compared to the classical DLL. Of course, the ACTL can also lose lock because of some improper switching behaviour due to high channel noise. This can be improved by employing switching criteria resulting in a periodic discriminator characteristic with hysteresis. Also, because the three arms are identical, they can all be used in the code acquisition phase in order to speed up this process by a factor of three.

Acknowledgment: We would like to thank P. E. Leuthold, Director of the Communication Technology Laboratory, ETH, Zurich, for his support of this research.

References


LOW THRESHOLD VOLTAGE VERTICAL CAVITY SURFACE-EMITTING LASER

K. L. Lear, S. A. Chalmers and K. P. Killeen

Indexing terms: Lasers, Semiconductor lasers

Vertical-cavity surface emitting laser diodes with threshold voltages as low as 1.48 V are demonstrated. The devices have low-resistance epitaxial mirrors, and current passes through the entire mirror stack. The low threshold voltage results from both low threshold current densities and mirrors with low resistivities even at low current densities. The laser fabrication sequence is relatively quick and simple and allows for the rapid characterization of vertical-cavity surface-emitting laser material.

Vertical cavity surface emitting lasers (VCSELs) have developed rapidly during the past few years, but their performance is still hampered by high mirror resistances due to large potential barriers at each heterojunction in the mirror stacks. Previously, high threshold voltages, typically 3 V or more, were symptomatic of these high parasitic series resistances which also caused poor efficiencies and other problems associated with excessive heating [1]. Recently, alternative laser structures have been developed in which the current flow bypasses the top mirror giving threshold voltages as low as 1.7 V [2]. We report a VCSEL threshold voltage of 1.48 V in an all-epitaxial semiconductor structure in which current flows through the entire mirror stack. The reduction in threshold voltage results from greatly reduced mirror voltage drops due to low resistivity mirrors with completely linear current-voltage characteristics [3] and low threshold current densities due to an efficient cavity design and high reflectivity mirrors. Highly conducting VCSEL mirrors are necessary for the planar, implant isolated fabrication approach [4], but also could be used to advantage even in lateral injection approaches.

ELECTRONICS LETTERS 1st April 1993 Vol. 29 No. 7
Our all-epitaxial structure was grown by molecular-beam epitaxy and included low resistivity Be-doped and Si-doped AlGaAs mirrors. The mirror interfaces are continuously graded from 10 to 50% AlGaAs mole fraction by varying both the aluminium and gallium effusion cell temperatures using a method similar to that reported previously [5]. We adjusted the temperature profiles to give an eight-segment piecewise linear approximation to a sinusoid, and obtained linear current-voltage characteristics with resistivities as low as $1.8 \times 10^{-2} \Omega \text{cm}^2$ for 20 period mirror stacks with Be doping concentrations of $5 \times 10^{10} \text{cm}^{-2}$ [6]. The importance of current-voltage linearity is manifest in the characteristics of a typical superlattice graded mirror and the continuously graded mirror shown in Fig. 1. Although these two alternate grading schemes can produce roughly similar differential resistivities at high current densities, the voltage drop of the 8 segment mirror is much smaller at low current densities (<500 A/cm$^2$). Threshold current densities in this range are achieved in this work and have been reported by other groups [6, 7]; they are expected to become typical for high performance VCSELs.

The voltage drop is that measured for the mirror stack alone; contact and substrate voltage drops have been subtraced

![Fig. 1 Voltage against current density for 20 period mirror stacks with 8 segment period compared with superlattice graded mirror.](image)

We have combined our mirrors with a triple InGaAs quantum well cavity to produce a very low threshold voltage VCSEL structure. The growth begins with 35 periods of an Si doped mirror on an n-type substrate following which the majority of the cavity is grown. The growth is then interrupted to measure the reflectivity spectrum. Based on the measured wavelength of the cavity mode and mirror stop band, the layer thicknesses for the remainder of the cavity and the 22 period Be-doped mirrors are adjusted to correct the cavity and mirror centre wavelengths [8]. This single measurement ensures a highly accurate cavity wavelength that typically falls within 0.25% of the desired value.

To assess the VCSEL design and material quality, bottom-emitting devices of various sizes were fabricated from this epitaxial structure. Devices were made with a single photolithographic step which defined an evaporated pure gold circular or square contact by liftoff. In addition to functioning as electrical contacts, the gold features enhance the reflectivity of the top mirror and serve as masks for a phosphoric wet etch used to isolate devices. The etch went part way into the lower mirror stack as well as undercutting the gold contact by ~3 µm at the junction plane. A blanket Ge/Au/Ni/Au n-type contact was then evaporated on the sample. The overhanging perimiter of the gold contact formed by the wet etch undercut prevented the n-type contact metal from landing on the sloped mesa side and shorting out the junction.

The devices were driven CW, and the power emitted through the polished but uncoated substrate was measured with a calibrated silicon photodiode. All current–voltage measurements were verified to within 1 mV using multiple instruments. The light-current and voltage-current characteristics of a diode with a 25 µm diameter junction are presented in Fig. 2. The device exhibits a 2.9 µA, 1.48 V lasing threshold which is only 0.23 V in excess of the photon energy corresponding to the lasing wavelength of 990 nm. Neighbouring devices had similar characteristics. The ripple in the output power curve is a result of the coupling with the cavity formed by the bottom mirror and the uncoated substrate. Despite the high bottom reflectivity and the substrate reflection, the output power peaked at 96 mW. Measurements on larger devices with a 42 x 42 µm$^2$ square junction gave CW threshold currents as low as 81 mA or threshold current densities of 460 A/cm$^2$. These large devices produced 2.5 mW of output power at 60 mA and lased to currents greater than 100 mA.

![Fig. 2 Light and voltage against current characteristics for 25 µm diameter mesa etched VCSEL.](image)

The measured power output is consistent with that expected from a simple calculation of external slope efficiency using estimates for mirror reflectivities, internal quantum efficiency, and free carrier absorption, but neglecting other losses such as scattering and diffraction. The bottom mirror of the VCSEL structure has 35 periods with a calculated reflectivity of 99.86%. The top mirror is 21 periods ending in a 1/4 layer that in combination with the semiconductor-air interface gives a reflectivity of 99.27%. This design is ultimately intended to be used for top emitting devices with the top output coupler transmissivity being much greater than that of the bottom high reflector. However, the addition of gold on the top mirror boosts the calculated reflectivity of the top mirror to 99.87%. Note that the reflectivity is increased by the gold even in the absence of an additional 1/6 phase matching layer that would have maximised the reflectivity [9]. The estimated round trip free-carrier absorption is 1% which, being much larger than the mirror losses, dominates the total losses and leads to poor slope efficiencies. By dividing the bottom mirror transmissivity by the total losses and assuming an 80% internal quantum efficiency and further accounting for the 30% reflection at the uncoated substrate to air interface, we estimate an external slope efficiency of 6%. This calculated value agrees well with the measured value for the large devices.

The fabrication sequence described here offers a convenient means for the rapid fabrication of VCSELs to evaluate epitaxial structure design and quality. It is not, however, intended to give optimum laser performance. The high mirror reflectivities lower the threshold but greatly diminish the power output. The low mirror loss emphasizes the effect of other loss mechanisms such as free-carrier absorption, diffraction, and scattering. The conical shape of the lasers not only contributes to diffraction losses but accentuates the contact and upper mirror resistance because their areas are smaller than the junction area. The importance of reducing the contact and other parasitic resistances along with that of the p-type mirror is evident from examining the total series resistance of our lasers. The slope of the current–voltage curve in Fig. 2 gives a differential resistance of 45 Ω above 15 mA. This is 10 times higher than the resistance expected due to the approximately $2 \times 10^{-2} \Omega \text{cm}^2$ p-mirror contribution. Hence, the other parasitic resistances are now dominant and must be reduced for further device improvement.

In summary, we believe we have demonstrated a record low CW threshold voltage for VCSELs. This low voltage results from a low threshold current density of 460 A/cm$^2$ in combination with a mirror having low resistance at these current densities. The devices have been fabricated by a method which allows for quick evaluation of InGaAs quantum well VCSEL material including that designed for top emitting structures.
More optimum fabrication approaches using this epitaxial structure and attention to other parasitic resistances should result in yet better performance.

Acknowledgments: The authors would like to thank S. Samora, S. Kileyone, and J. Nevers for technical assistance, R. Geels for the use of his mirror simulation program, "Multi-layer", and K. Choquette, A. Owyoung, and J. Tsao for a careful review of the manuscript. This work was performed at Sandia National Laboratories, supported by the US Department of Energy under contract No. DE-AC04-76DP00789.

References


Fig 1 Gate capacitance measurements on SOI n-MOSFETs with different lengths for near-zero and very positive back-gate voltages

W = 50 μm, \( \mathrm{TO}_{1} \approx 52 \, \mathrm{nm} \), \( \mathrm{TO}_{2} = 90 \, \mathrm{nm} \)
-- near zero back-gate voltage
-- very positive back-gate voltage

On one hand, appropriate shielding and a careful calibration procedure are used to eliminate the stray capacitance due to the connection leads to the device under test. An incomplete elimination however does not affect our calculations, because the stray component can be assumed constant throughout the measurements and all the extraction formulas are based on differences of capacitance values.

On the other hand, fringing capacitance effects may not be totally neglected. \( C_{b} \) indeed incorporates inner \( (C_{ib}) \) and outer fringing \( (C_{of}) \) capacitances, related to the existence of electric field line between gate and source/drain either inside or outside the device active area. Whereas the outer fringing is almost bias-independent and is hence removed by capacitance subtraction, the inner fringing value strongly depends on the applied biases [7]. It is maximum for \( C_{ib} \), but completely vanishes for conditions corresponding to the measurement of \( C_{of} \) due to the shielding effect of the front inversion layer. Regarding \( C_{ib} \) because there is no front inversion, we will assume this

EXTRACTION OF PHYSICAL DEVICE DIMENSIONS OF SOI MOSFETS FROM GATE CAPACITANCE MEASUREMENTS

D. Flandre and B. Gentinne

Index terms: MOSFETs, Capacitance measurement, Silicon-on-insulator structures and devices

A new technique unique to SOI MOSFETs is presented for extracting the physical device dimensions (effective gate length and gate oxide and film thicknesses) from a set of gate capacitance measurements on transistors with various lengths.

Introduction: Gate capacitance measurement of MOS transistors is widely used for the characterisation of bulk Si devices [1]. In SOI technology, such measurements have seldom been used for fabrication [2-6] and we assume that the method has so far been restricted to the extraction of the SOI film thickness from measurements on very large devices [4-6].

In this Letter, the technique is extended to the simultaneous extraction of the effective gate length and of the gate oxide and film thicknesses from a set of gate capacitance measurements on transistors with various lengths. Subsequently, the technique is also validated for the extraction of the film thickness on devices with short dimensions.

Limitations of previous technique: The technique presented in Reference 4 to extract the film thickness \( \mathrm{TO}_{1} \) of an SOI MOSFET was based on the variation of the capacitance measured between gate and source/drain with front-gate \( (\mathrm{V}_{g}) \) and back-gate voltages \( (\mathrm{V}_{b}) \) [2, 3]. At low \( \mathrm{V}_{g} \), the capacitance curve of an SOI MOSFET is quite similar to that of a conventional bulk MOSFET (Fig. 1): in the cutoff regime, a minimum value \( C_{o} \) corresponding to the parasitic and gate-overlap capacitances is observed, whereas in the turn-on regime, a maximum value \( C_{a} \) close to the total oxide capacitance \( C_{ox} \) is obtained. At high positive \( \mathrm{V}_{b} \), the cutoff curve changes dramatically: a value \( C_{o} \) is observed which is much larger than \( C_{a} \). This has been related to the formation of an inversion layer at the film/buried oxide interface, so that \( C_{o} \) can be associated with the series combination of the fully-depleted film capacitance \( (C_{fd} = W \times L \times \varepsilon_{o} \varepsilon_{r} \mathrm{TO}_{1}) \) and of the total oxide capacitance. From this intuitive interpretation, the following formula was derived in Reference 4:

\[
\mathrm{TO}_{1} = \frac{C_{a} - C_{o}}{C_{r} - C_{o}} \times \frac{C_{o}}{C_{o} - 1}
\]

This formula was initially developed for very large devices \( (W \times L > 50 \, \mu m) \). To extend its validity to devices with more practical dimensions, it is not sufficient to account for the effective gate length \( L_{e} \) and width \( W_{eff} \). Inaccuracies in the measurement of the capacitance values should be adequately assessed.

ELECTRONICS LETTERS 1st April 1993 Vol. 29 No. 7