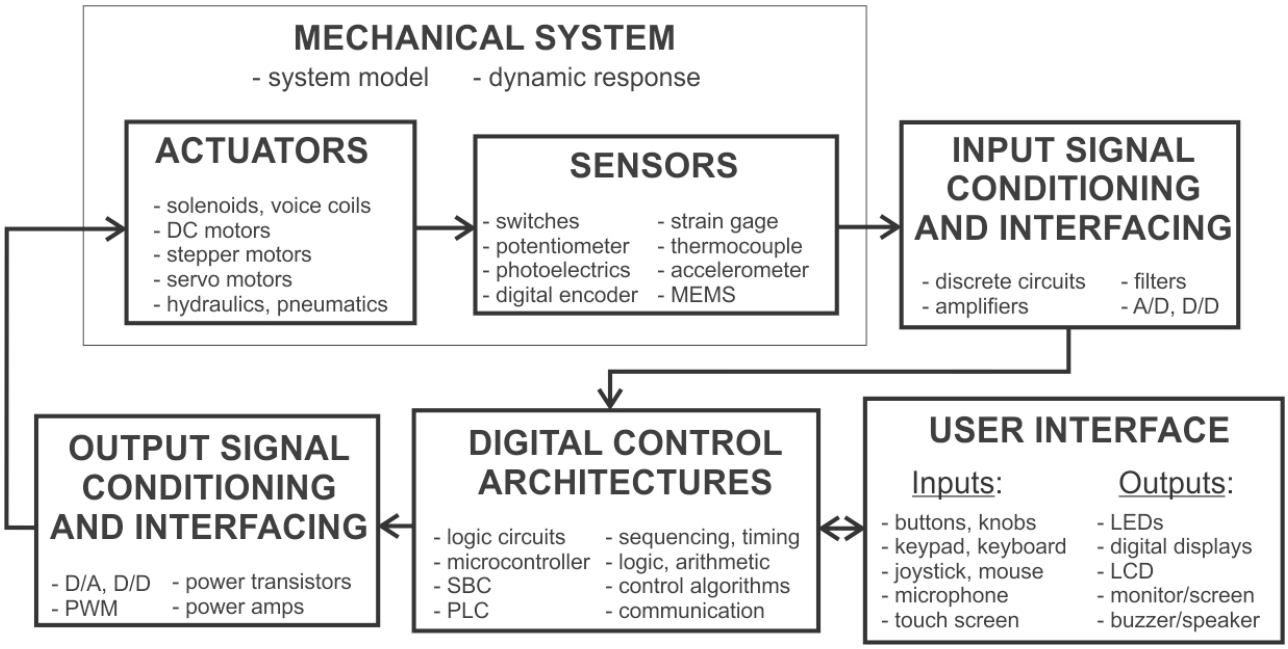
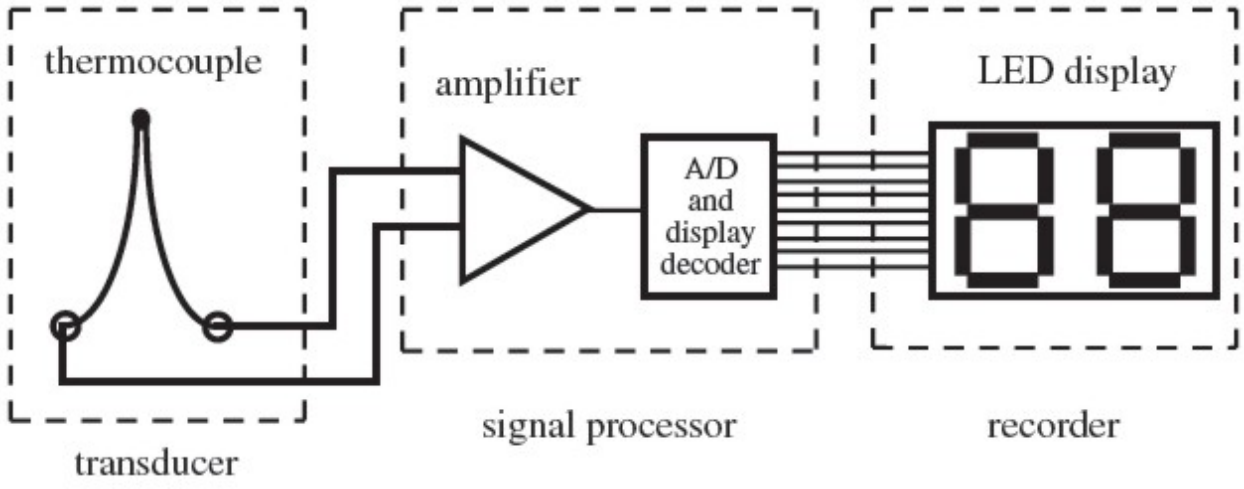
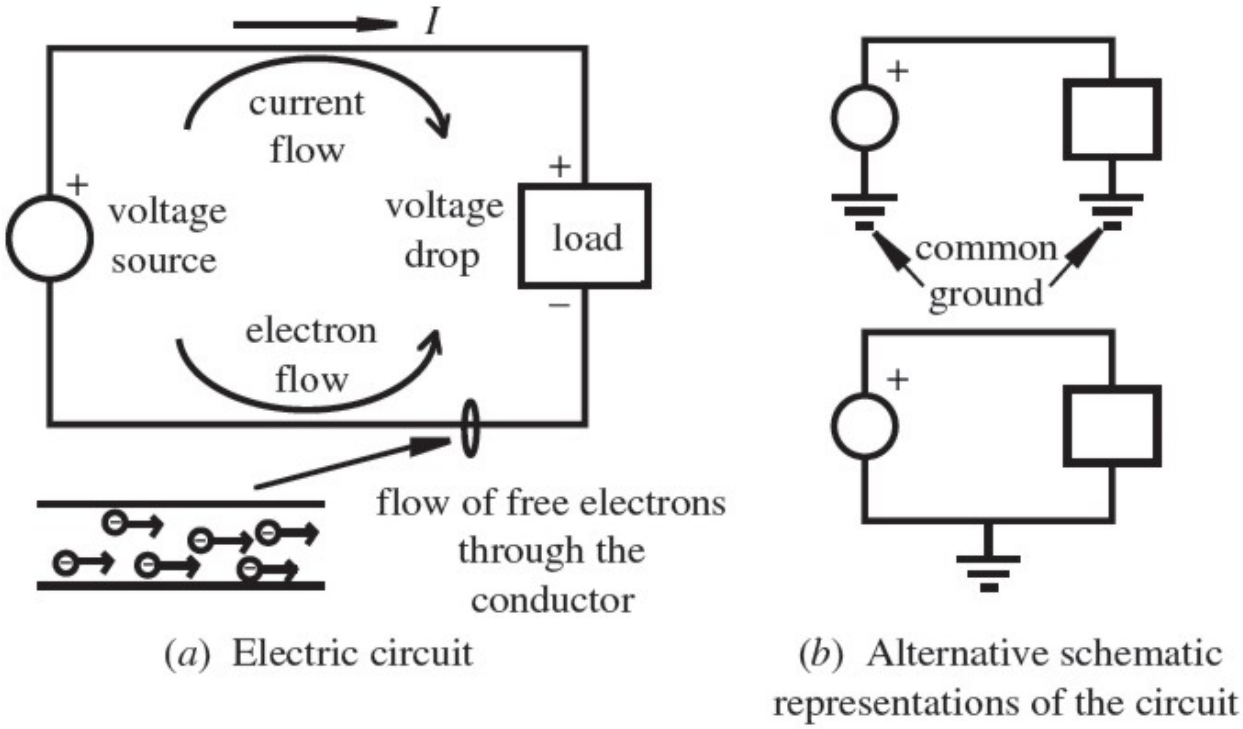


Figure 1.1 Mechatronic system components (p. 3)



Example 1.2 Measurement System—Digital Thermometer (p. 5)



(*a*) Electric circuit

(*b*) Alternative schematic representations of the circuit

Figure 2.2 Electric circuit terminology (p. 13)

Table 2.2 Resistor color band codes

a, *b*, and *c* Bands		*tol* Band	
Color	**Value**	**Color**	**Value**
Black	0	Gold	±5%
Brown	1	Silver	±10%
Red	2	Nothing	±20%
Orange	3		
Yellow	4		
Green	5		
Blue	6		
Violet	7		
Gray	8		
White	9		

Table 2.2 Resistor color band codes (p. 18)

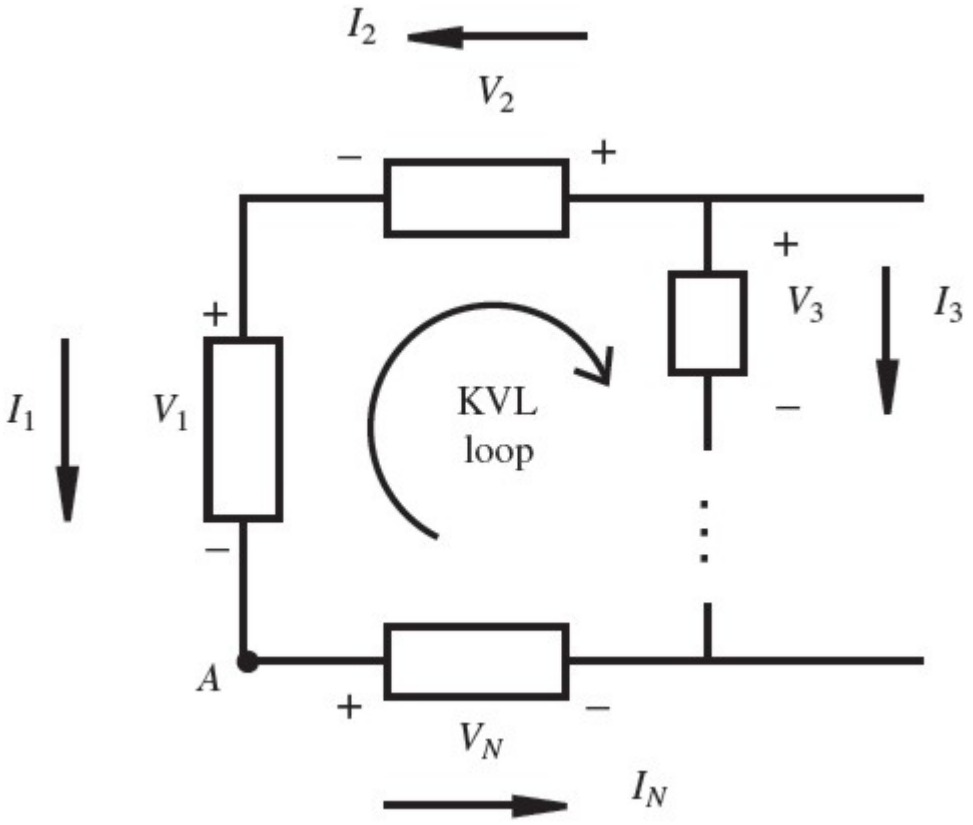
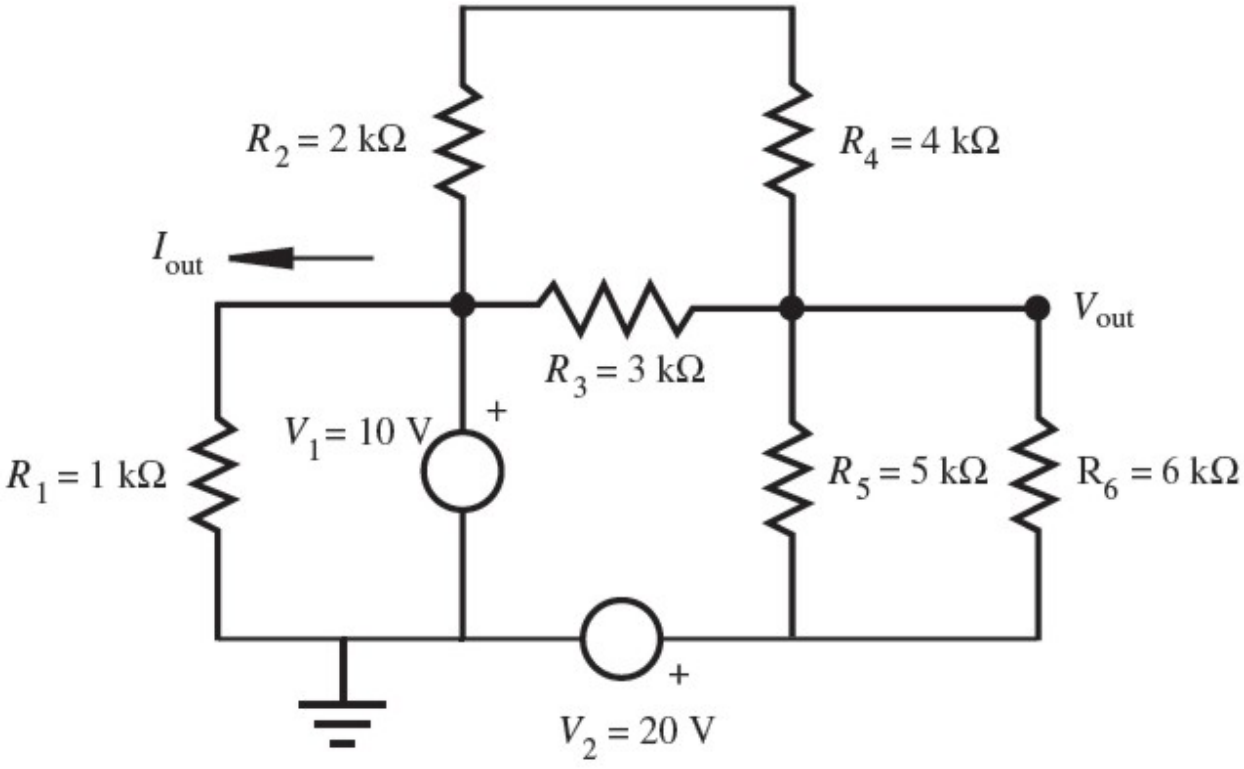
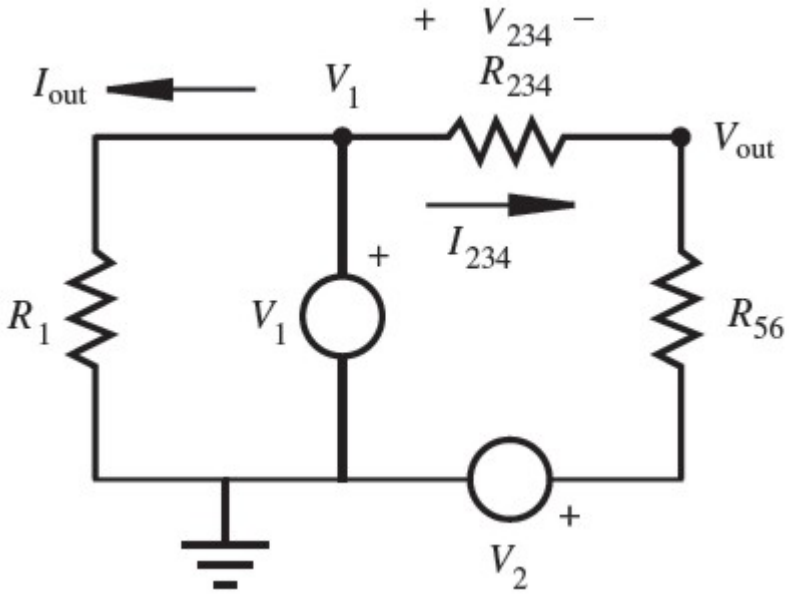


Figure 2.13 Kirchhoff's voltage law (p. 22)





Example 2.4 Circuit Analysis (p. 29)

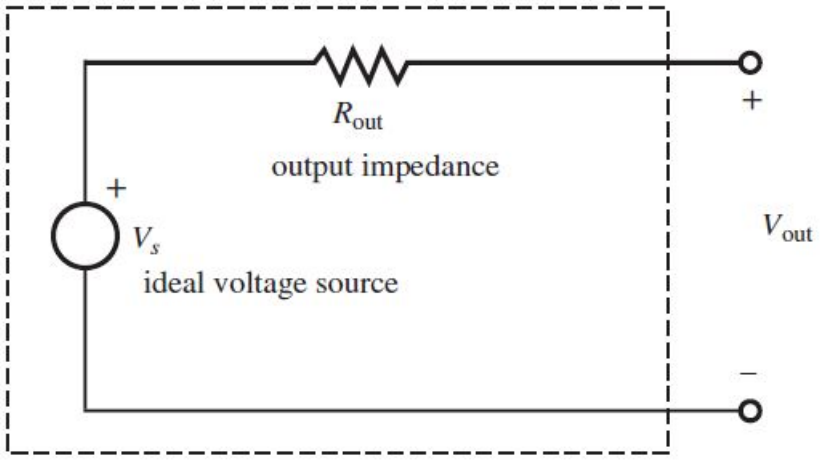


Figure 2.18 Real voltage source with output impedance (p. 31)

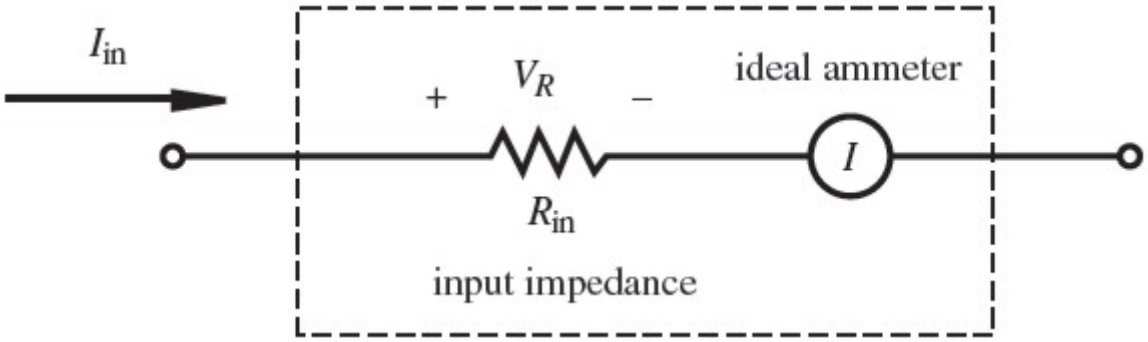


Figure 2.21 Real ammeter with input impedance (p. 32)

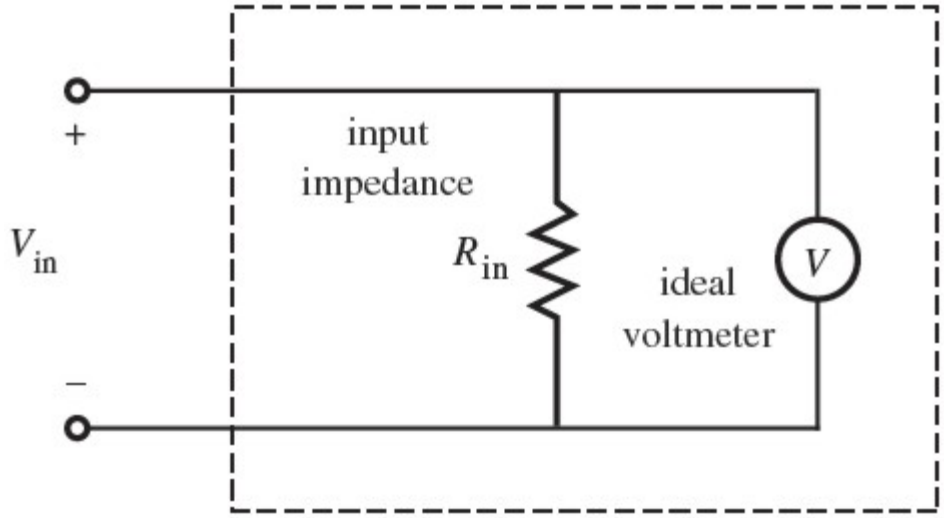


Figure 2.22 Real voltmeter with input impedance (p. 32)

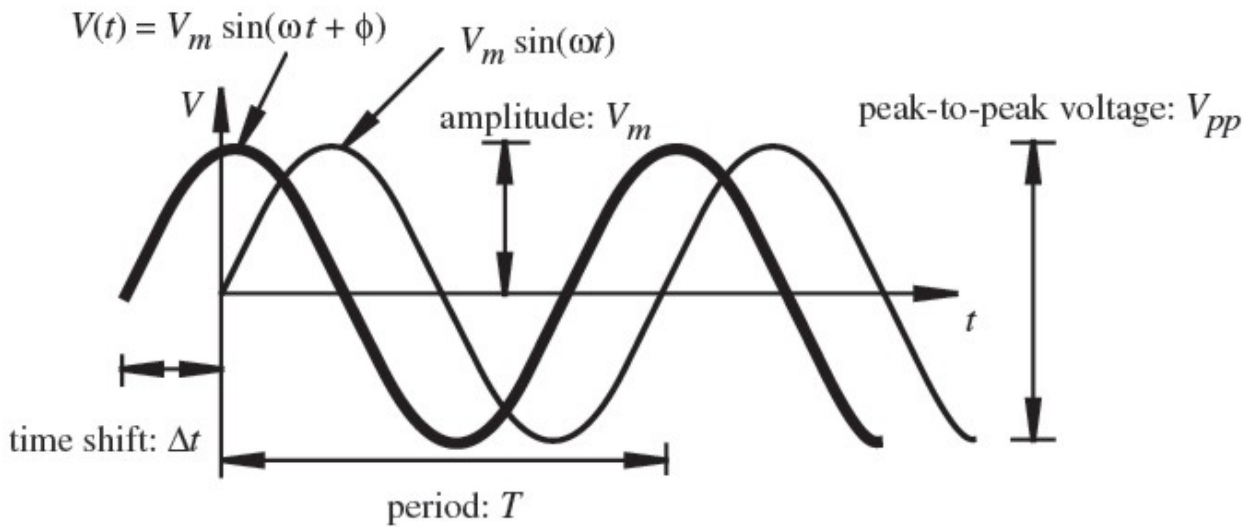


Figure 2.28 Sinusoidal waveform (p. 37)

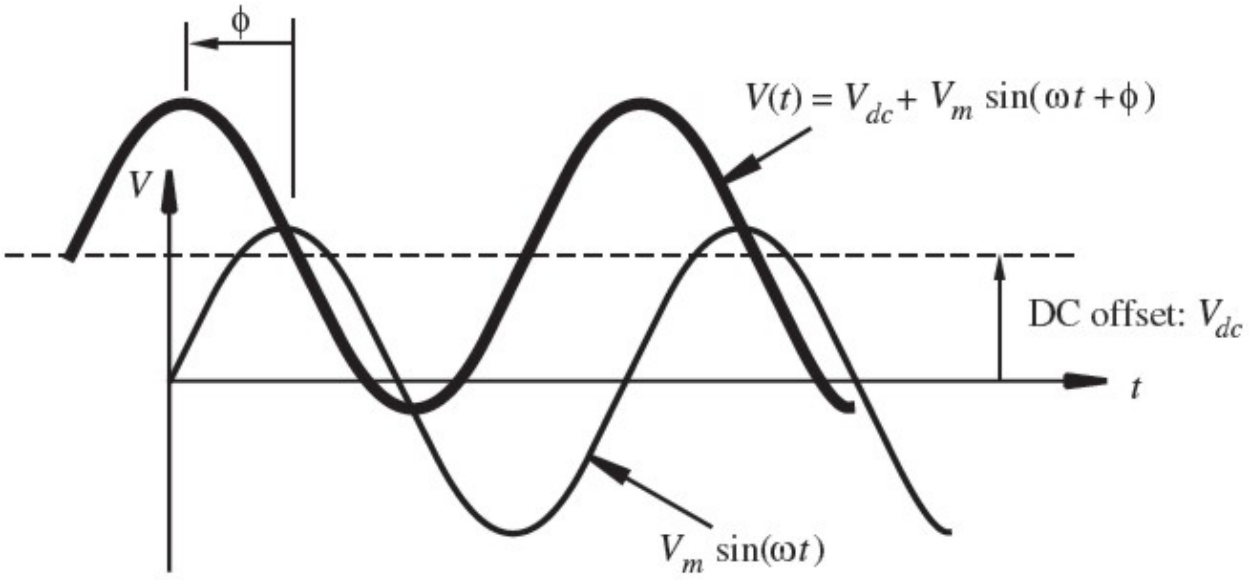


Figure 2.29 Sinusoidal signal DC offset (p. 38)

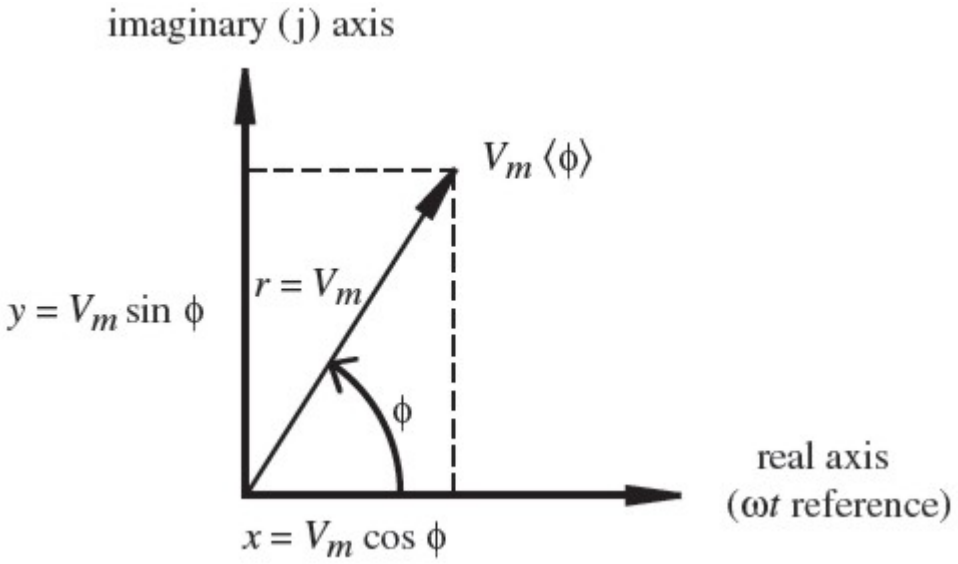
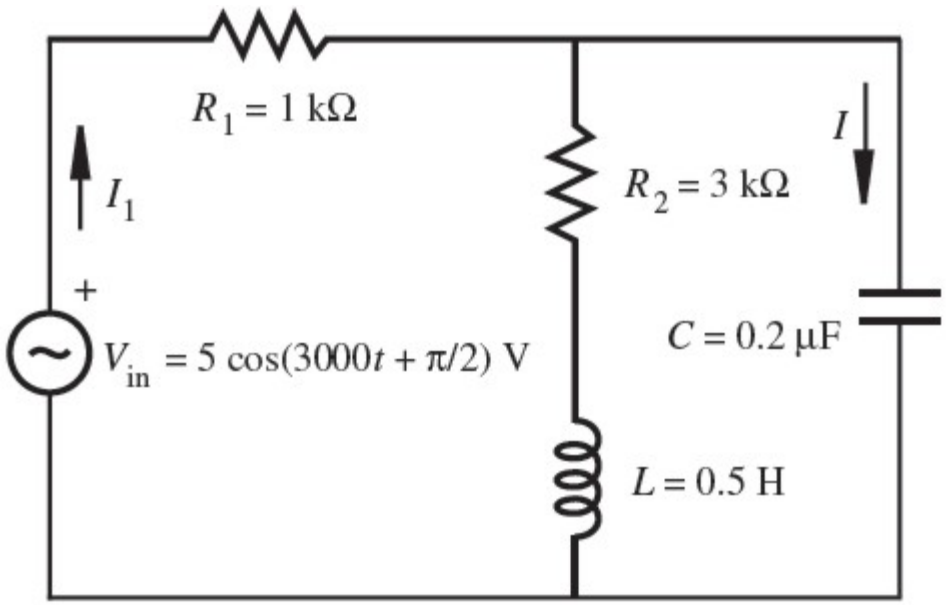


Figure 2.30 Phasor representation of a sinusoidal signal (p. 40)



Example 2.7 AC Circuit Analysis (p. 42)

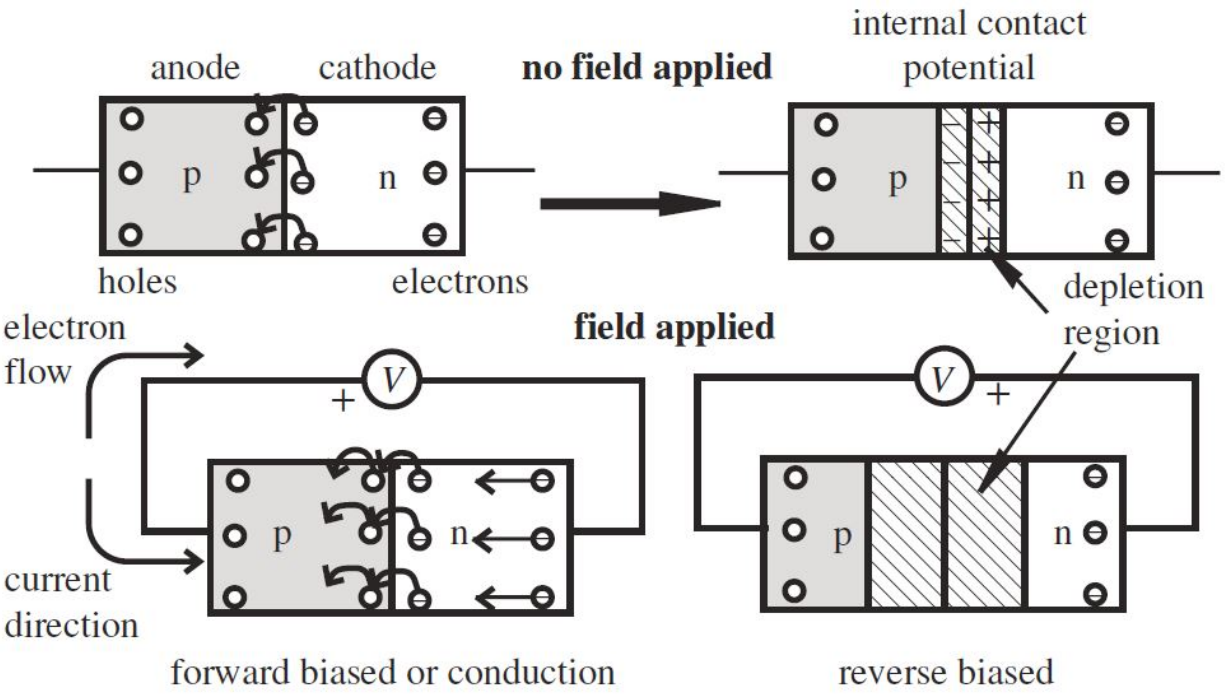


Figure 3.2 pn Junction characteristics (p. 78)

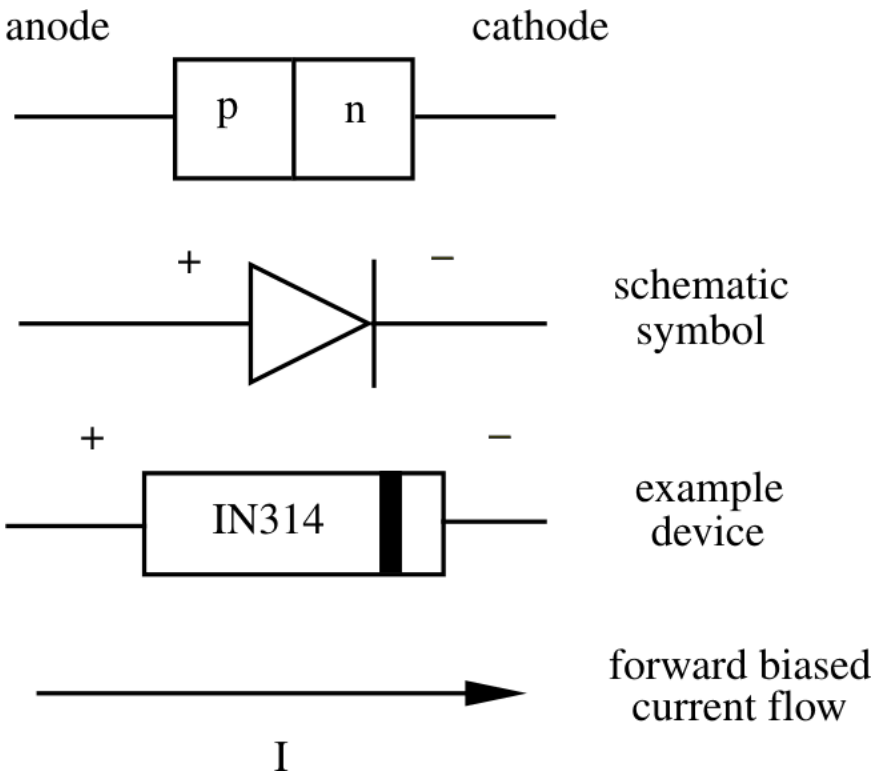


Figure 3.3 Silicon diode (p. 79)

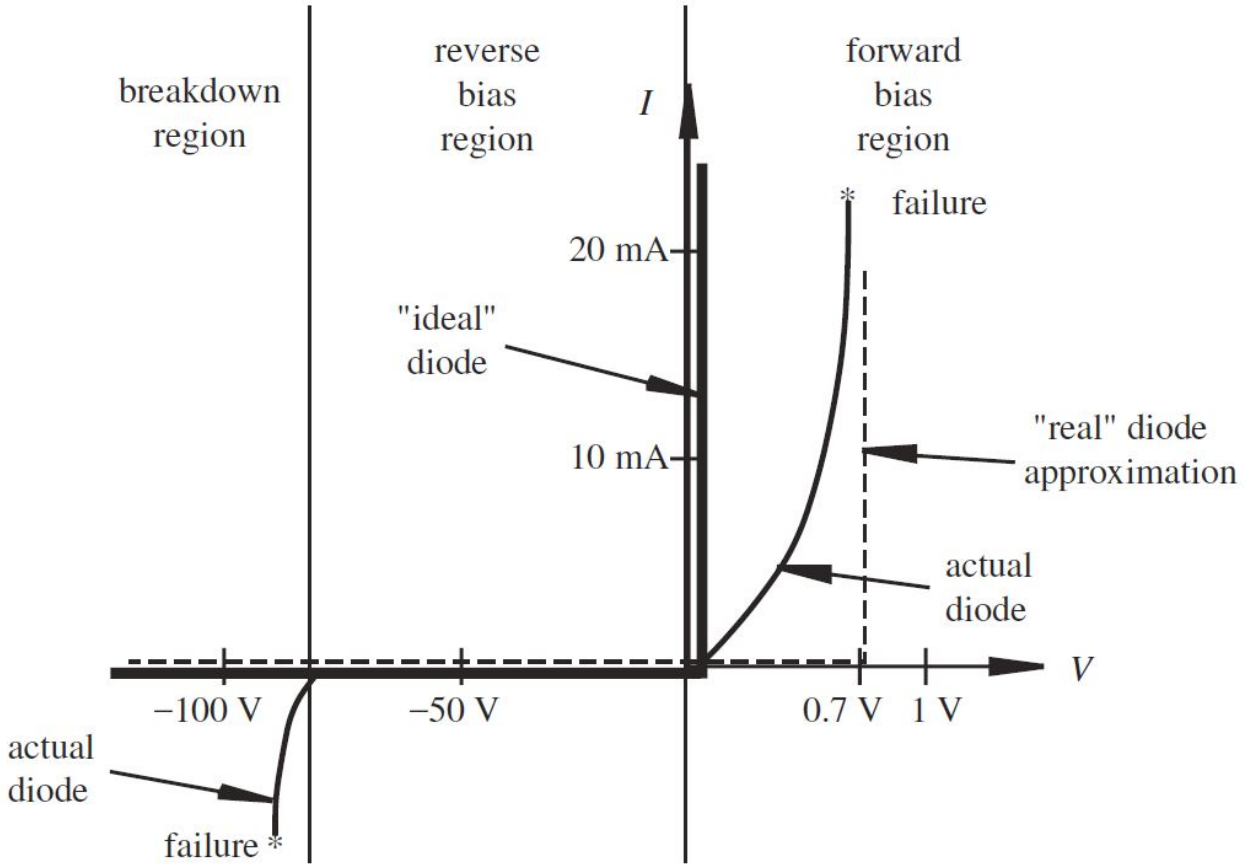


Figure 3.6 Ideal, actual, and approximate diode curves (p. 80)

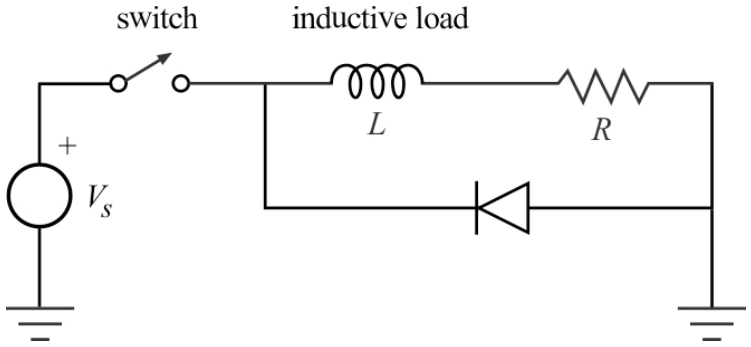
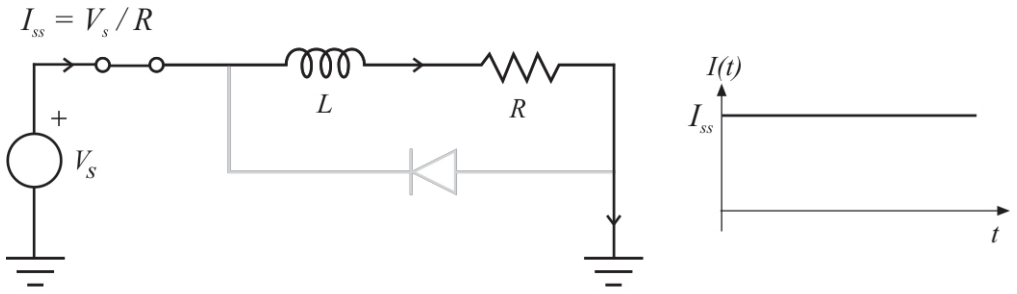
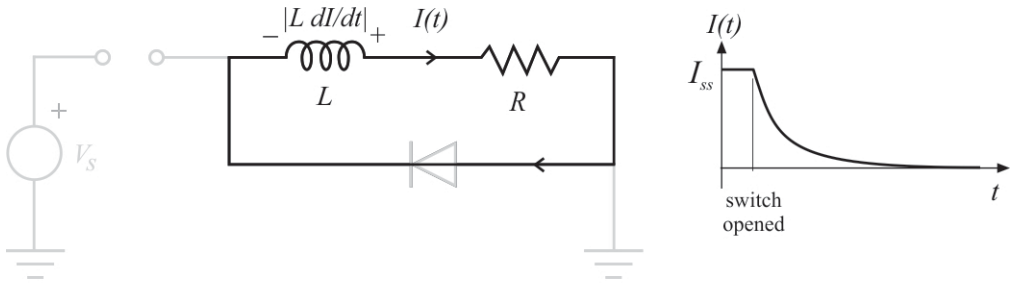


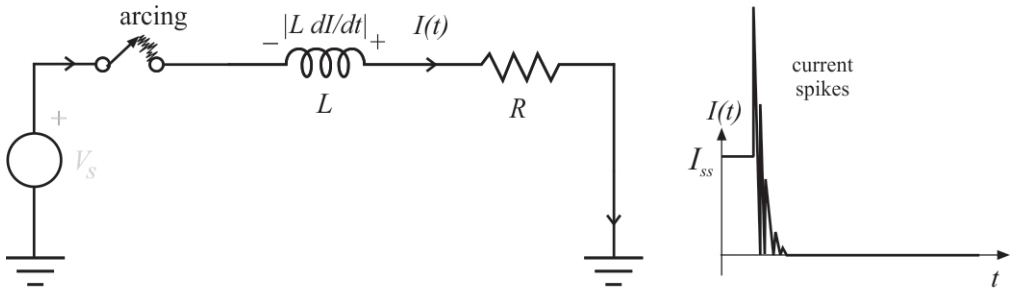
Figure 3.9 Inductive load flyback protection (p. 83)



(a) switch closed, in steady state



(b) immediately after switch opened



(c) immediately after switch opened, without flyback diode

Figure 3.10 Flyback action (p. 84)

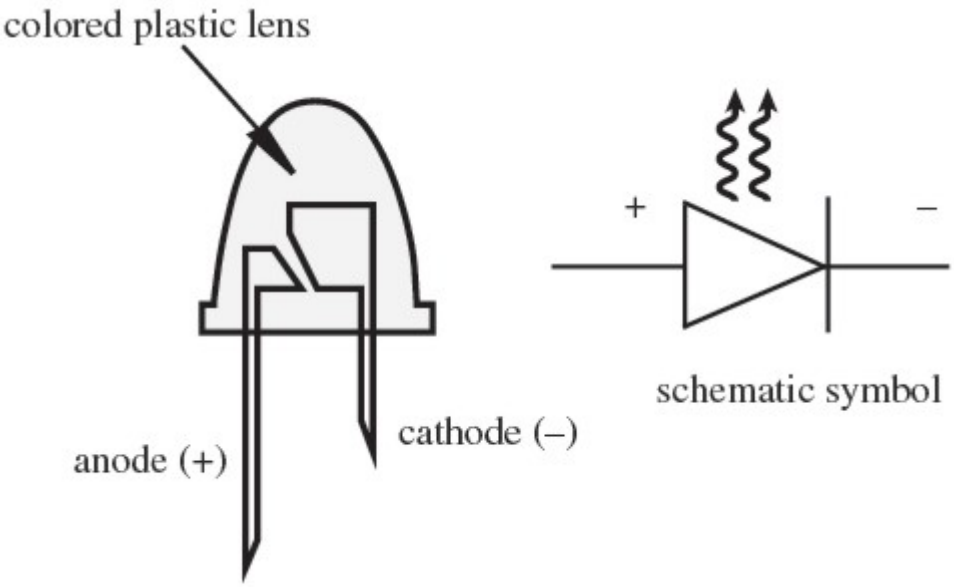


Figure 3.11 Light-emitting diode (p. 86)

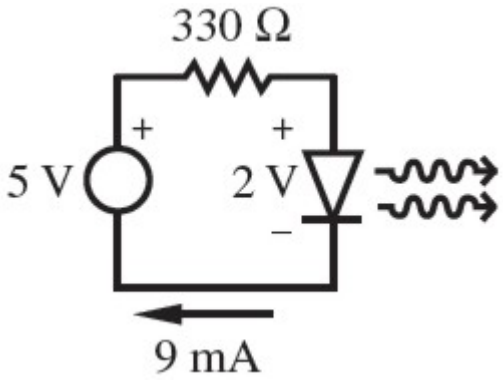


Figure 3.13 Typical LED circuit in digital systems (p. 86)

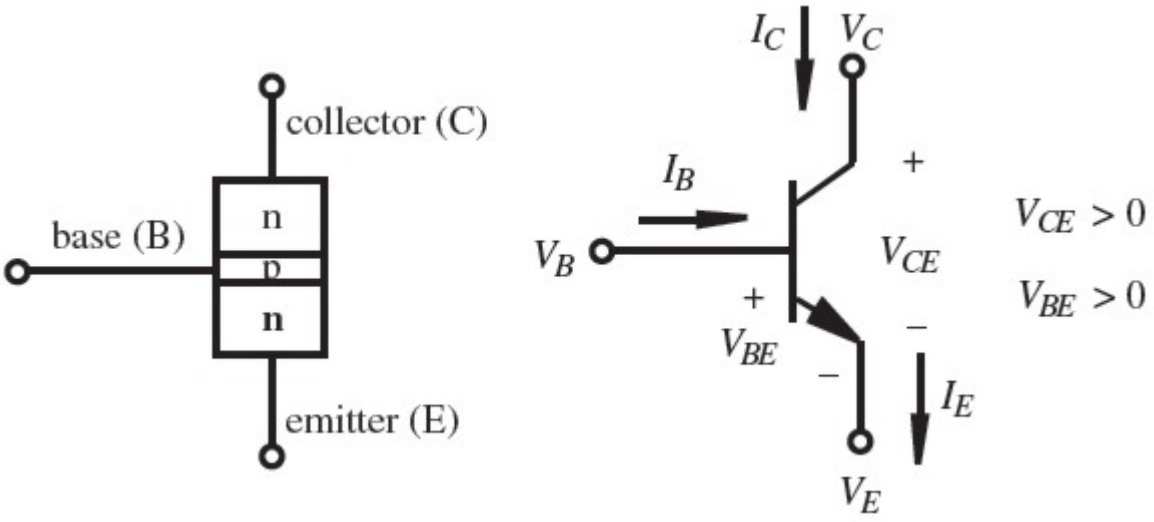
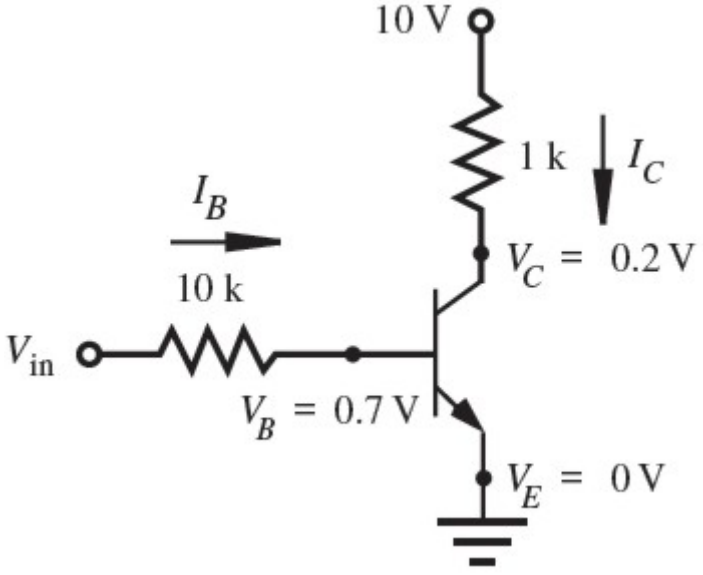


Figure 3.19 npn Bipolar junction transistor (p. 96)



Example 3.4 Guaranteeing a Transistor Is in Saturation (p. 99)

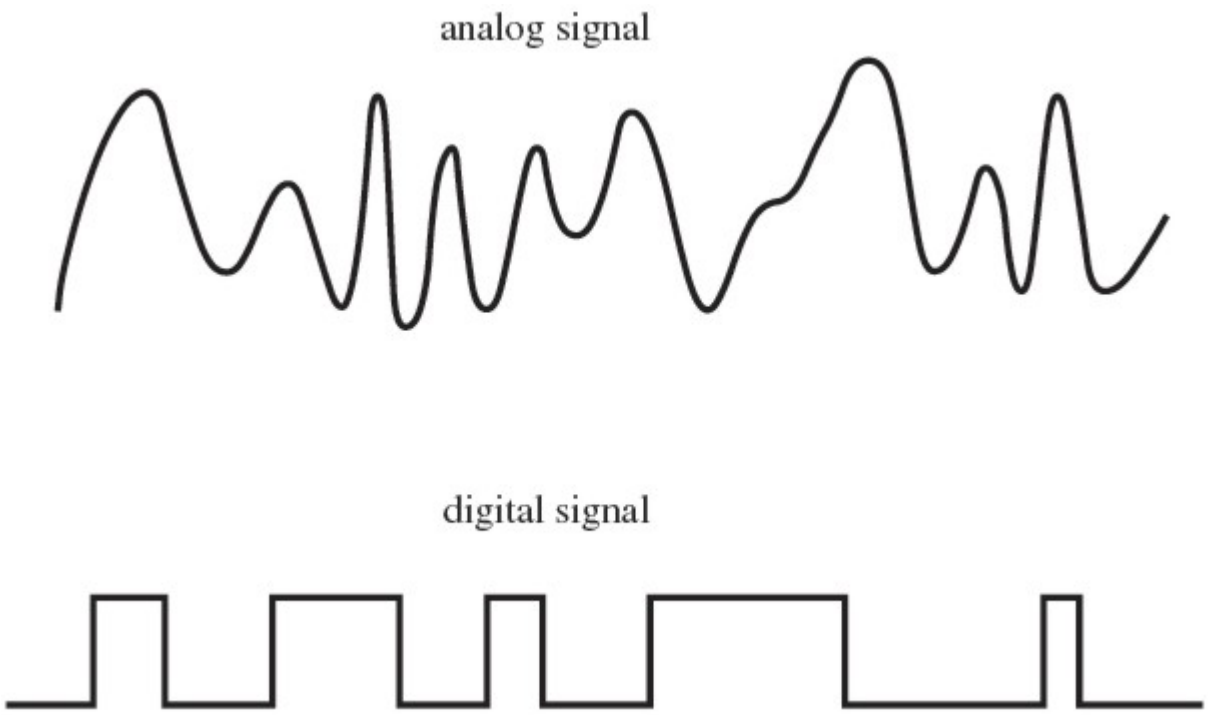


Figure 6.1 Analog and digital signals (p. 206)

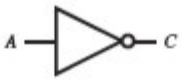
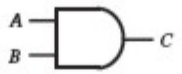
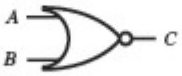
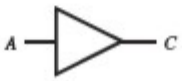
Gate	Operation	Symbol	Expression	Truth Table
Inverter (INV, NOT)	Invert signal (complement)		$C = \overline{A}$	A C 0 1 1 0
AND gate	AND logic		$C = A \cdot B$	A B C 0 0 0 0 1 0 1 0 0 1 1 1
NAND gate	Inverted AND logic		$C = \overline{A \cdot B}$	A B C 0 0 1 0 1 1 1 0 1 1 1 0
OR gate	OR logic		$C = A + B$	A B C 0 0 0 0 1 1 1 0 1 1 1 1
NOR gate	Inverted OR logic		$C = \overline{A + B}$	A B C 0 0 1 0 1 0 1 0 0 1 1 0
XOR gate	Exclusive OR logic		$C = A \oplus B$ $= A \cdot \overline{B} + \overline{A} \cdot B$	A B C 0 0 0 0 1 1 1 0 1 1 1 0
Buffer	Increase output signal current		$C = A$	A C 0 0 1 1

Table 6.3 Combinational logic operations (p. 211)

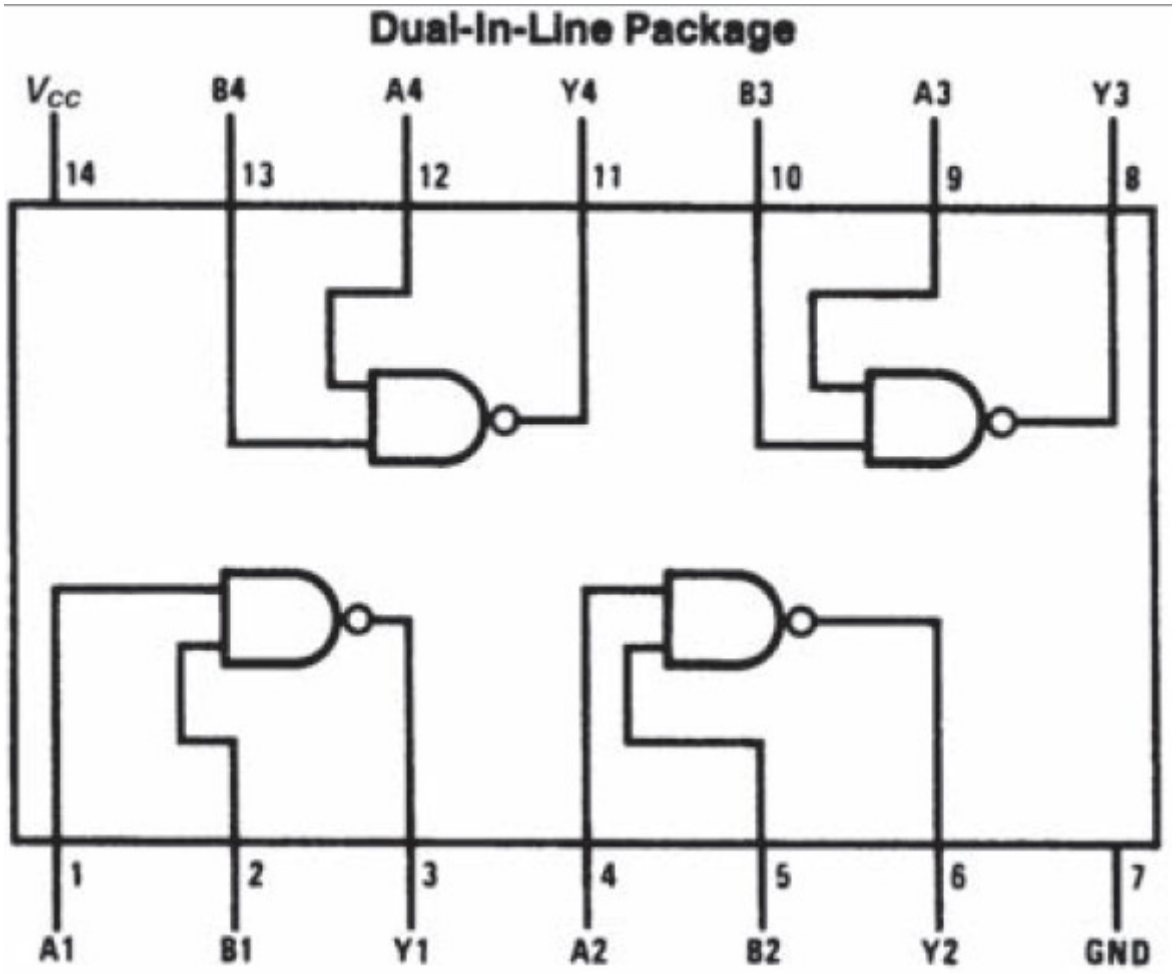


Figure 6.25 QUAD NAND gate IC pin-out (p. 238)

6.6.1 Define the Problem in Words

1. An active state where the alarm will sound only if the windows or doors are disturbed. This state is useful when the occupants are sleeping.
2. An active state where the alarm will sound if the windows or doors are disturbed or if there is motion in the house. This state is useful when the occupants are away.
3. A disabled state where the alarm will not sound. This state is useful during normal household activity.

- *A:* state of the door and window sensors
- *B:* state of the motion detector
- *Y:* output used to sound the alarm
- *C D:* 2-bit code set by the user to select the operating state defined by

$$C\,D = \begin{cases} 0\ 1 & \text{operating state 1} \\ 1\ 0 & \text{operating state 2} \\ 0\ 0 & \text{operating state 3} \end{cases}$$

6.6.2 Write Quasi-Logic Statements

Activate the alarm ($Y = 1$) if A is high *and* the code $C\,D$ is 0 1 *or* activate the alarm if A *or* B is high *and* the code is 1 0.

6.6.3 Write the Boolean Expression

$$Y = A \cdot (\overline{C} \cdot D) + (A + B) \cdot (C \cdot \overline{D}) \tag{6.29}$$

C	D	$(\overline{C} \cdot D)$	$(C \cdot \overline{D})$
0	0	0	0
1	0	0	1
0	1	1	0

6.6.4 AND Realization

$$Y = \overline{\overline{A \cdot D} \cdot \overline{(\overline{A} \cdot \overline{B}) \cdot C}} \tag{6.33}$$

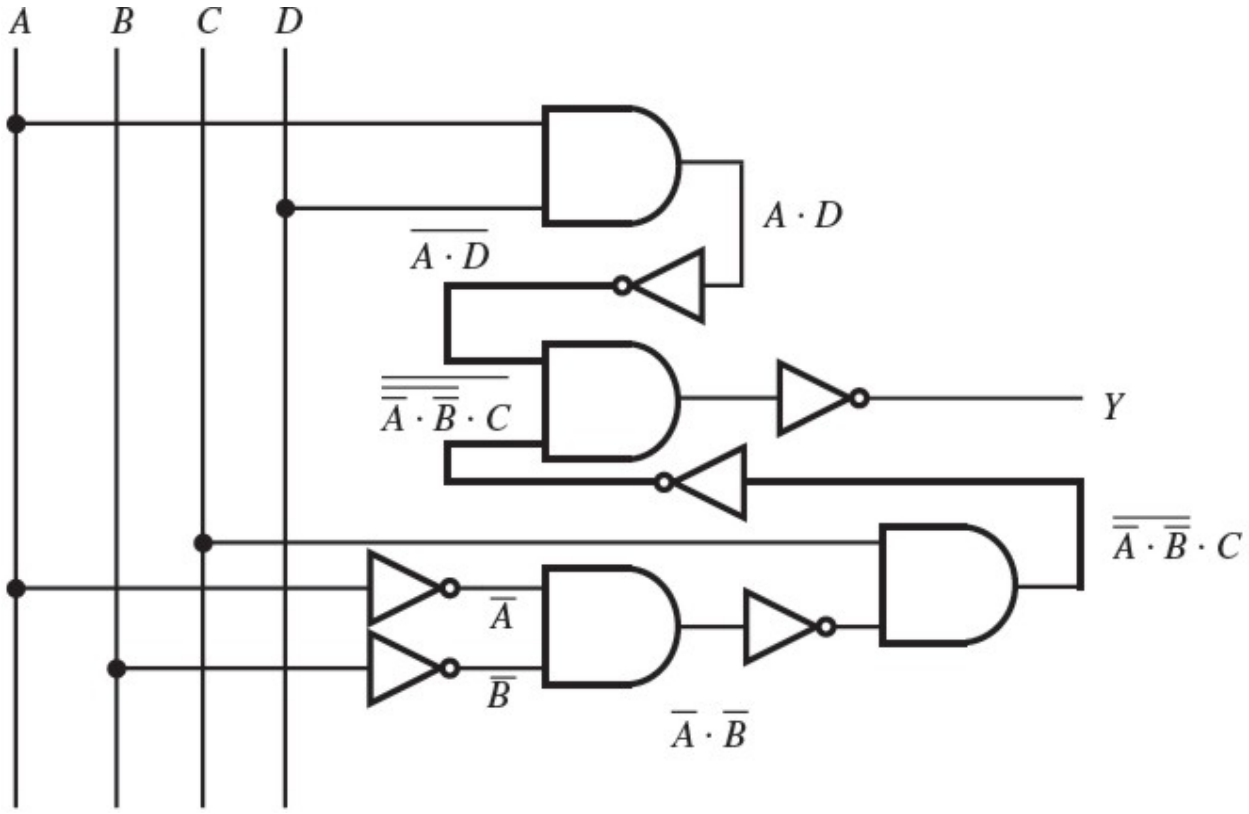


Figure 6.4 AND realization schematic of the security system. (p. 219)

EXAMPLE 6.4 Sum of Products and Product of Sums

$$\begin{array}{ccccc} & & & 1 & C \\ 0 & 0 & 1 & 1 & A \\ +0 & +1 & +0 & +1 & +B \\ \hline 0 & 1 & 1 & 0 & S \end{array}$$

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Sum Of Products (SOP)

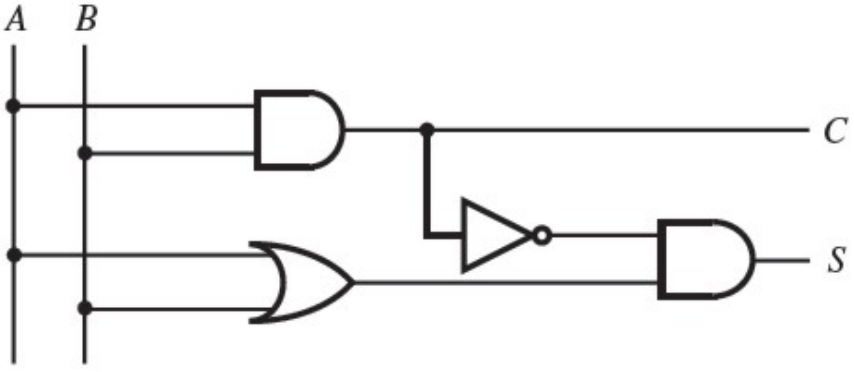
$$S = (\overline{A} \cdot B) + (A \cdot \overline{B})$$

$$C = (A \cdot B)$$

Product of Sums (POS)

$$C = (A + B) \cdot (A + \overline{B}) \cdot (\overline{A} + B)$$

$$S = (A + B) \cdot (\overline{A} + \overline{B})$$



Example 6.4 Sum of Products and Product of Sums (p. 220)

Figure 6.5 Clock pulse edges (p. 222)

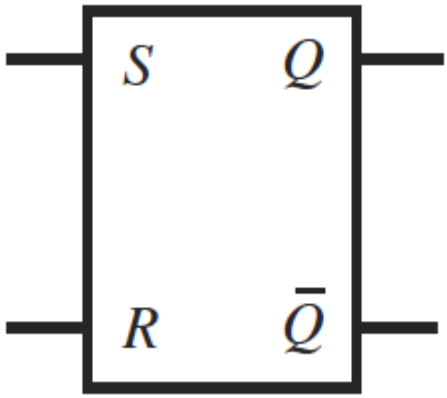


Figure 6.6 RS flip-flop (p. 223)

Inputs		Outputs	
S	R	Q	$\bar{Q}$
0	0	Q_0	$\bar{Q}_0$
1	0	1	0
0	1	0	1
1	1	NA	

Table 6.4 Truth table for the RS flip-flop (p. 223)

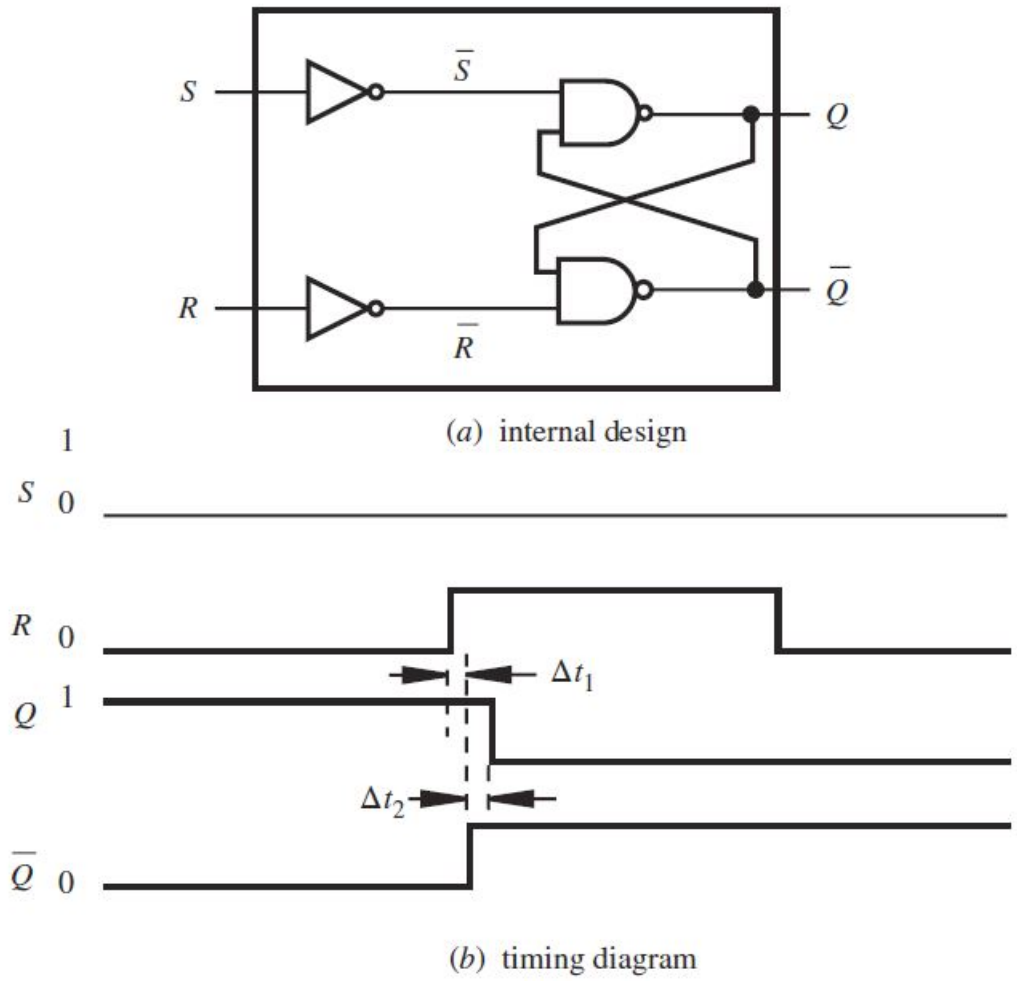


Figure 6.7 RS flip-flop internal design and timing (p. 224)

S	R	CK	Q	$\overline{Q}$
0	0	↑	Q_0	$\overline{Q}_0$
1	0	↑	1	0
0	1	↑	0	1
1	1	↑	NA	
X	X	0,1,↓	Q_0	$\overline{Q}_0$

Table 6.5 Positive-edge-triggered RS flip-flop truth table (p. 225)

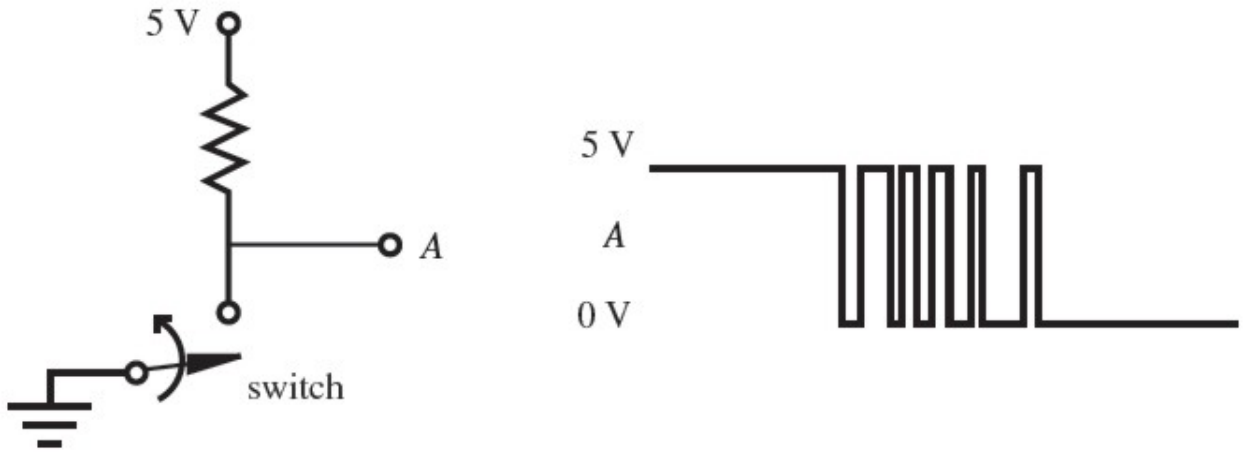


Figure 6.16 Switch bounce (p. 230)

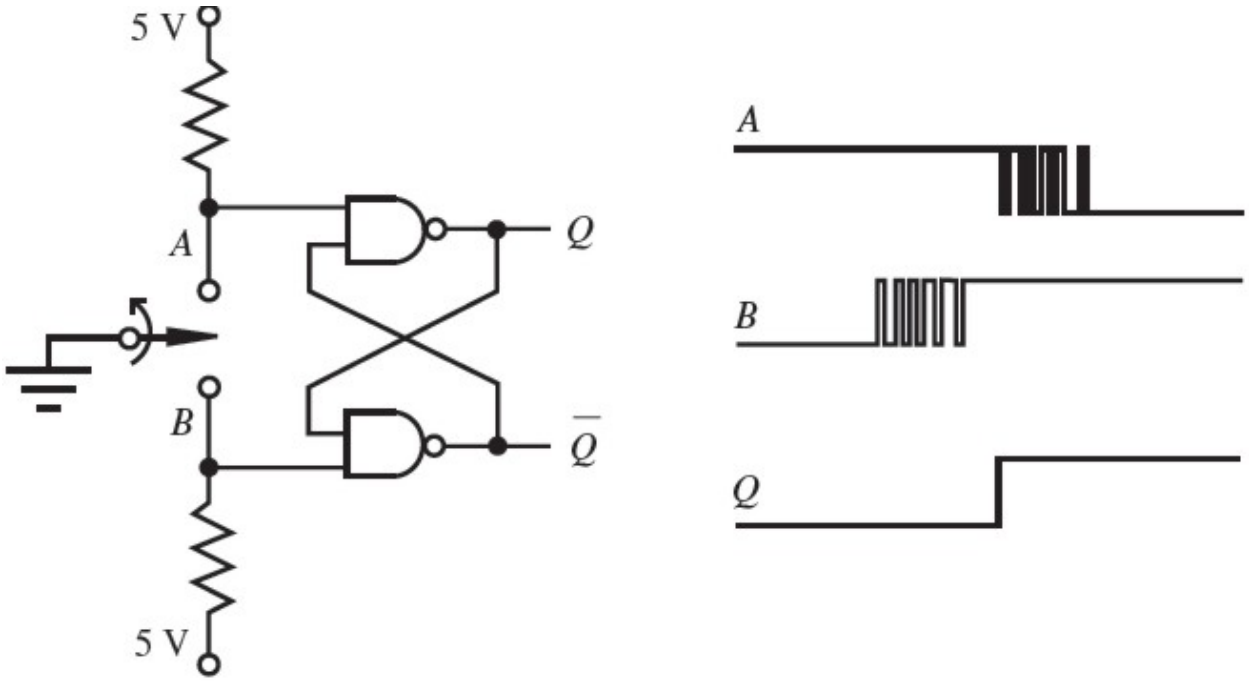


Figure 6.17 Switch debouncer circuit (p. 223)

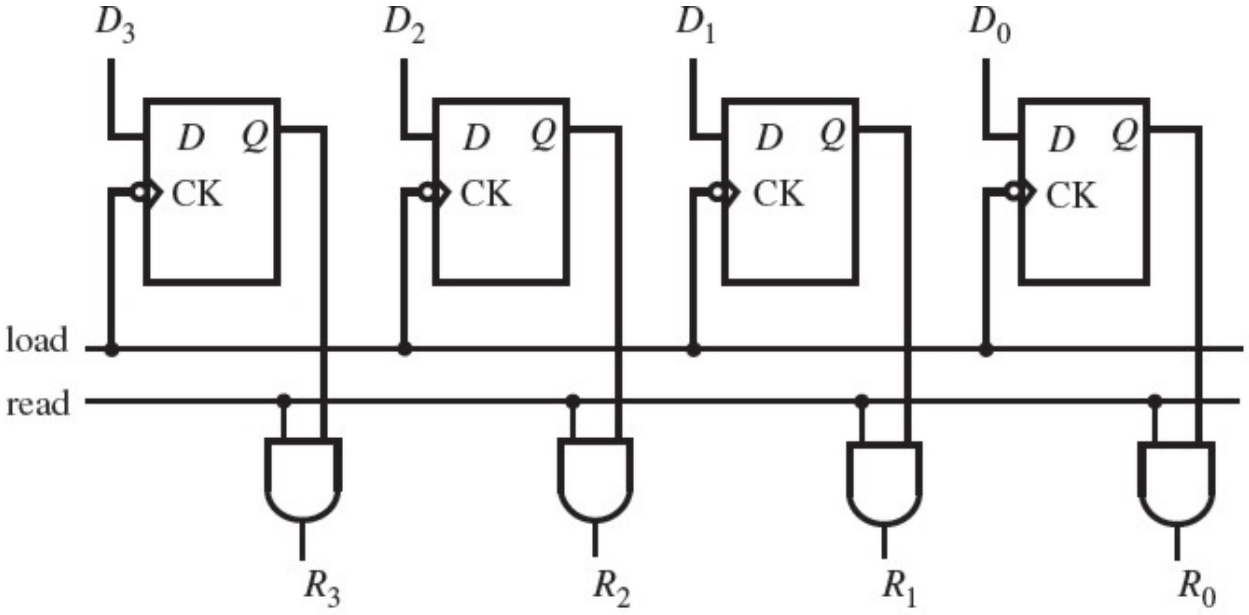


Figure 6.18 4-bit data register (p. 232)

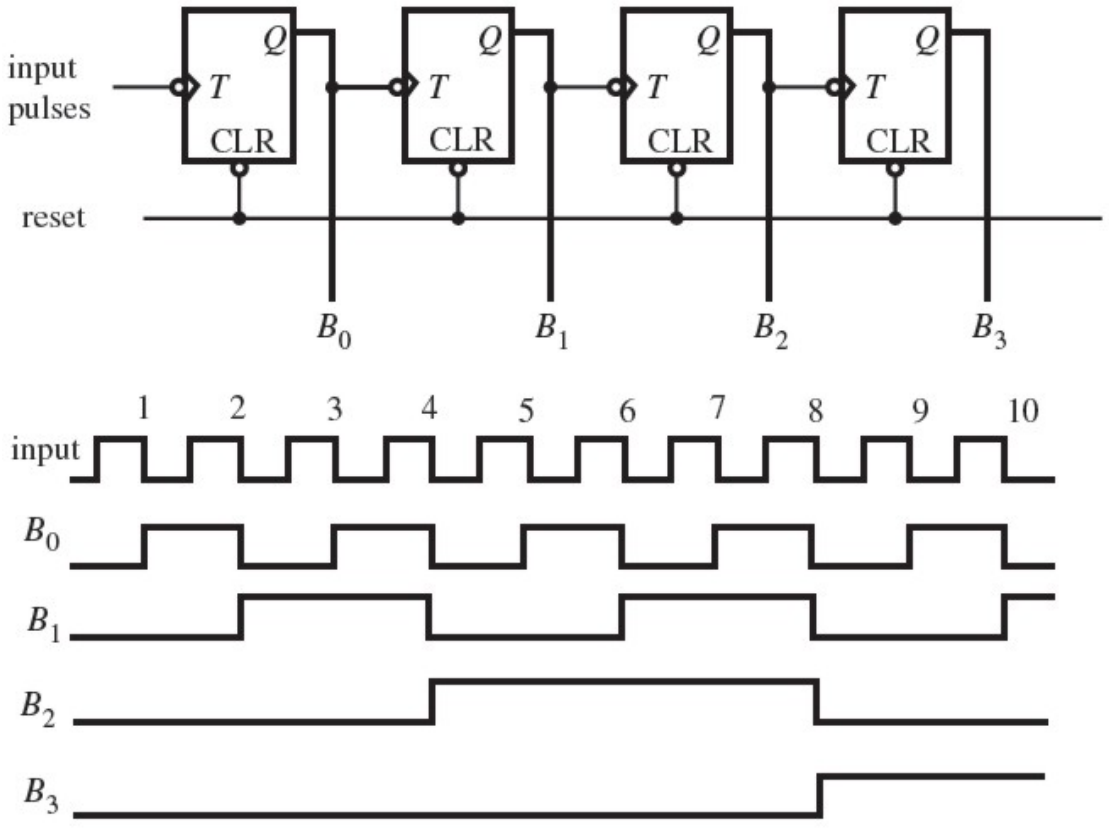


Figure 6.19 4-bit binary counter (p. 232)

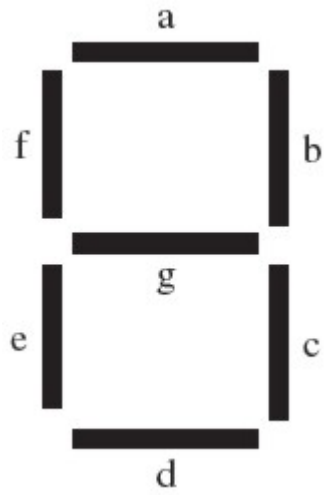


Figure 6.34 Seven-segment LED display (p. 245)

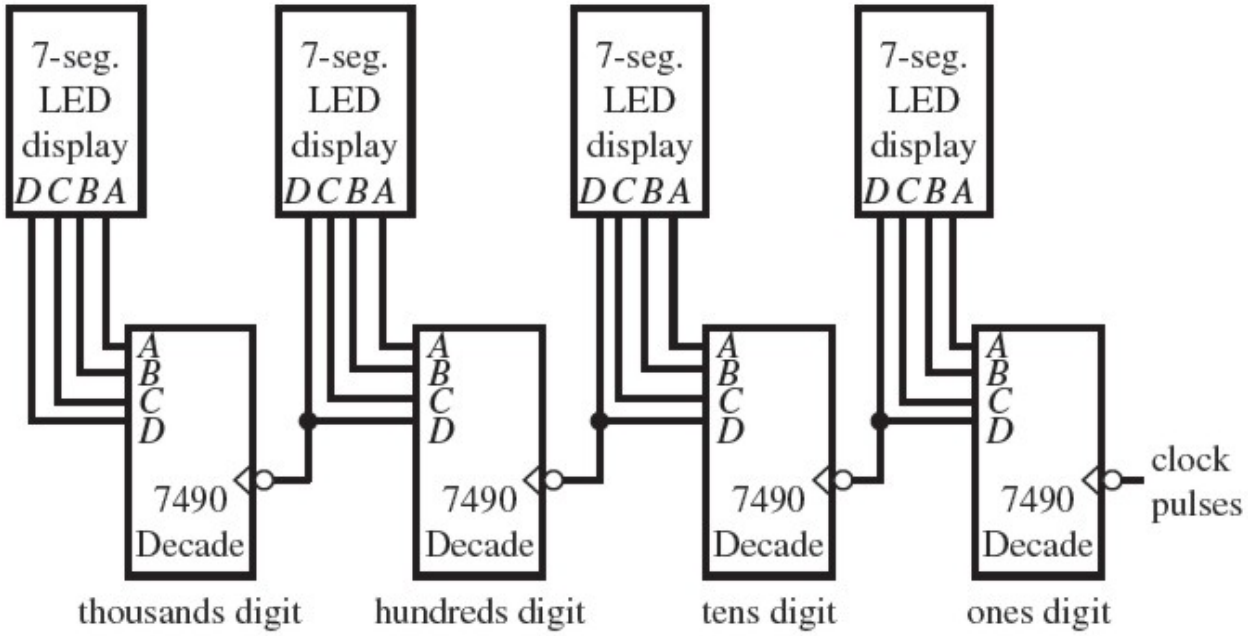


Figure 6.33 Cascaded decade counters (p. 244)

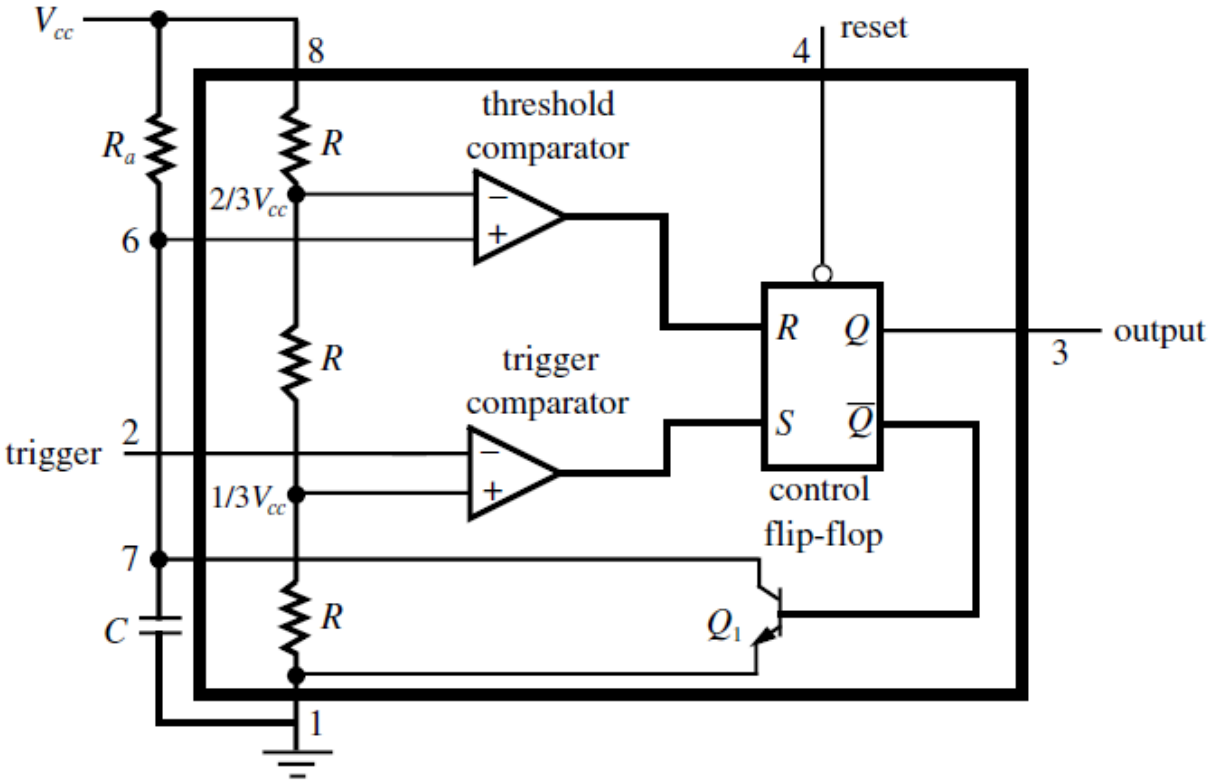


Figure 6.42 Block diagram of the 555 IC (p. 248)

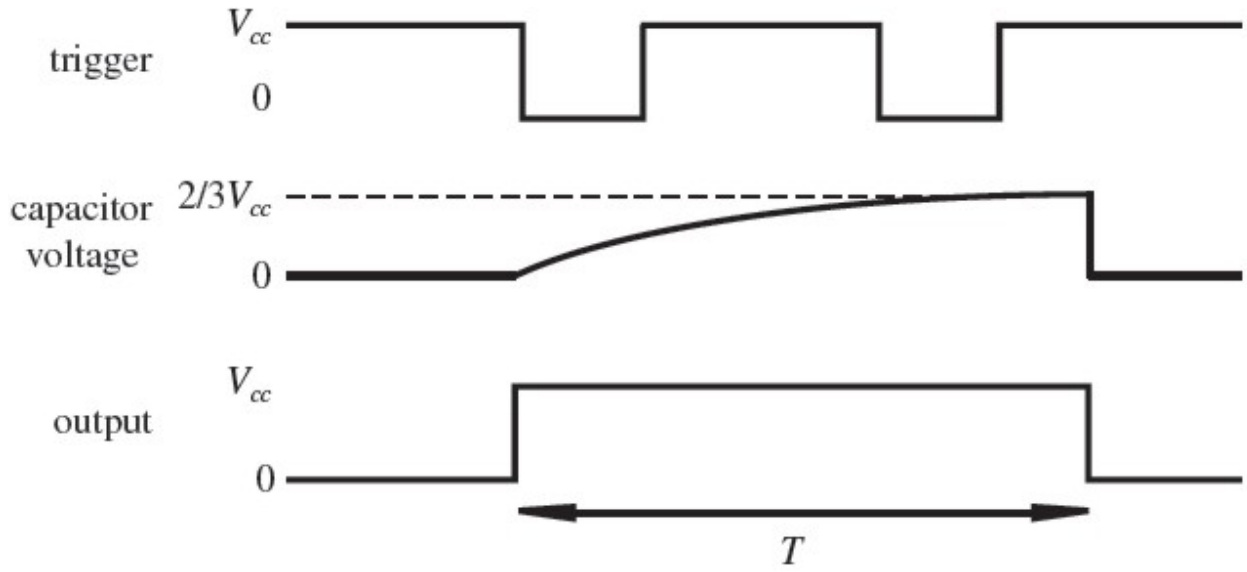


Figure 6.43 One-shot timing (p. 250)

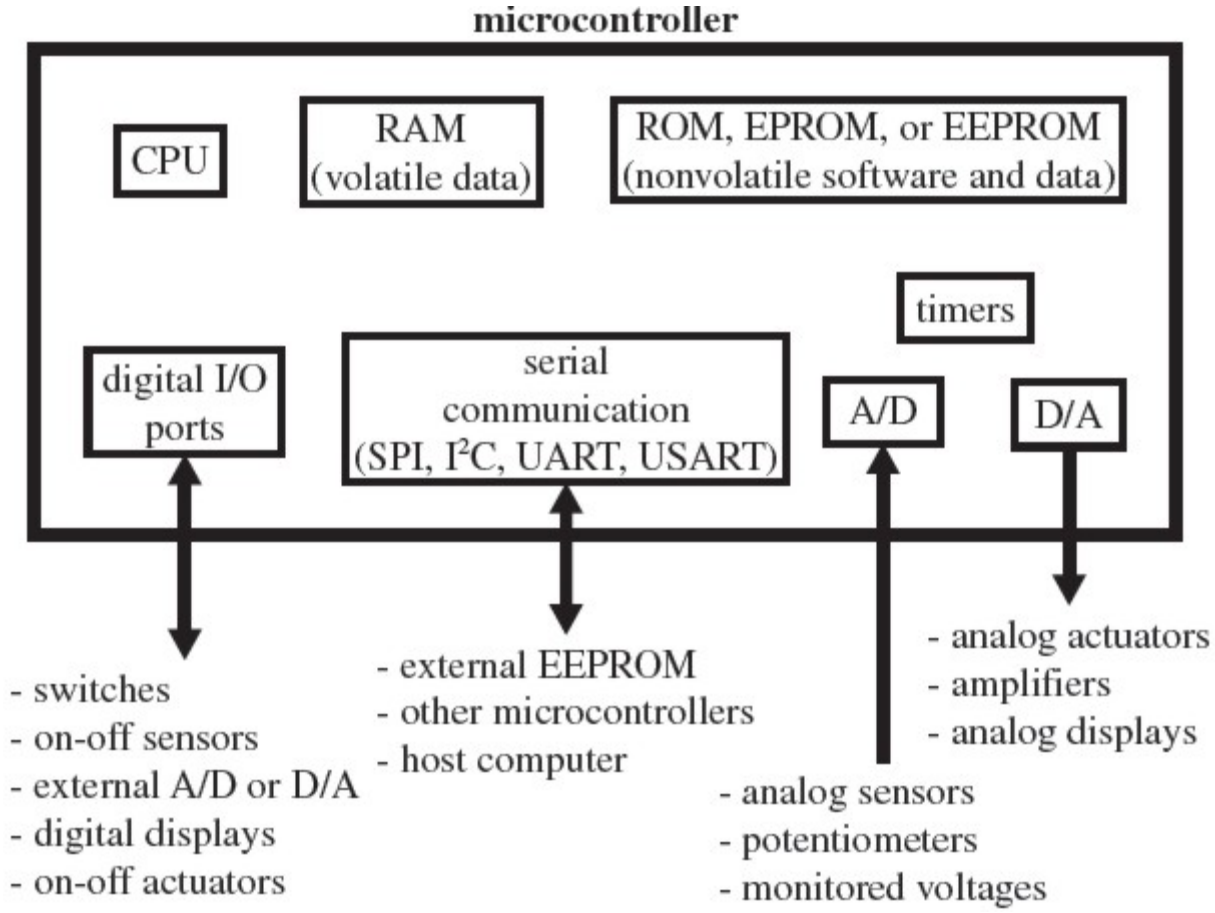


Figure 7.2 Components of a typical full-featured microcontroller (p. 271)

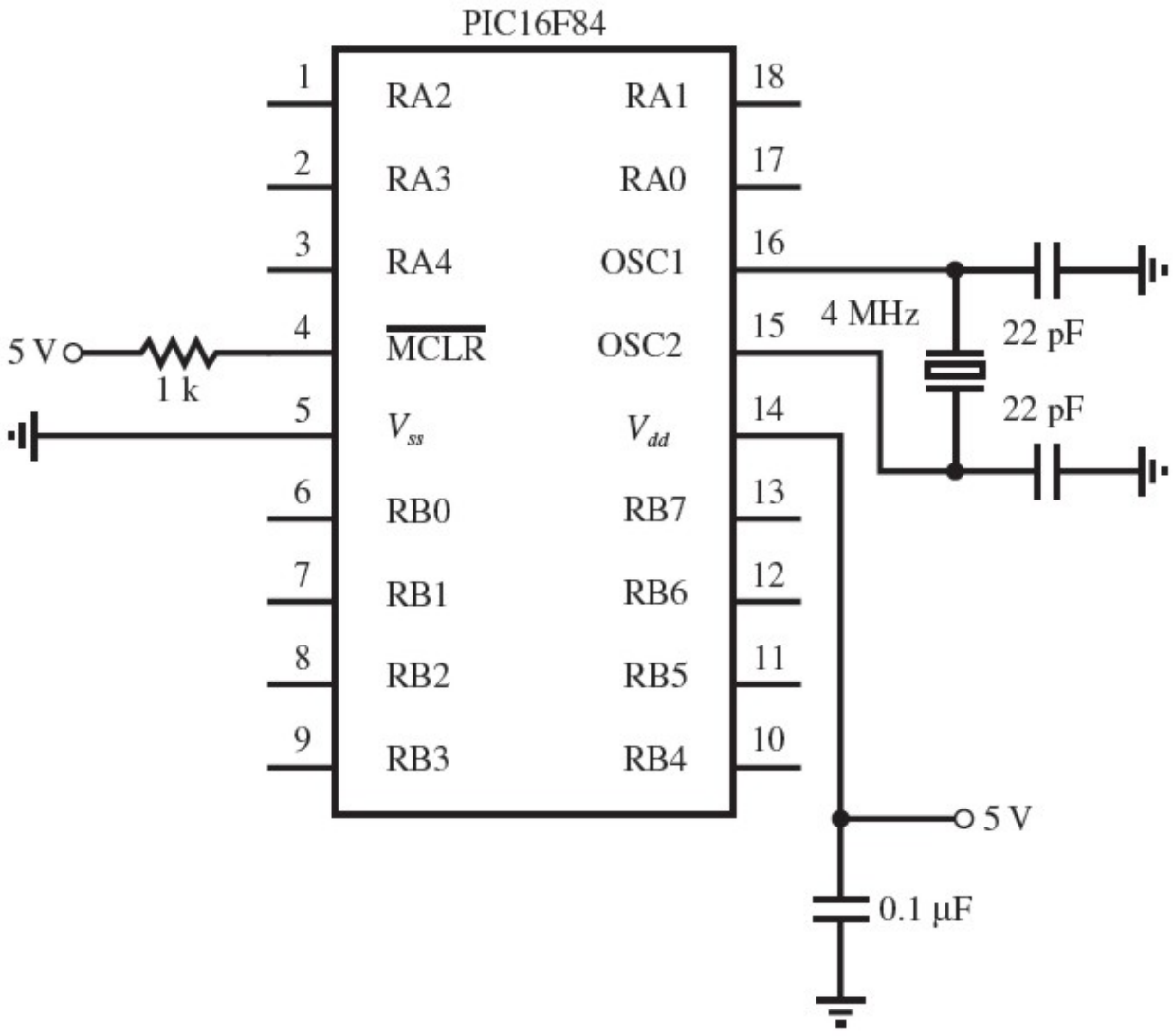


Figure 7.4 PIC16F84 pin-out and required external components (p. 274)

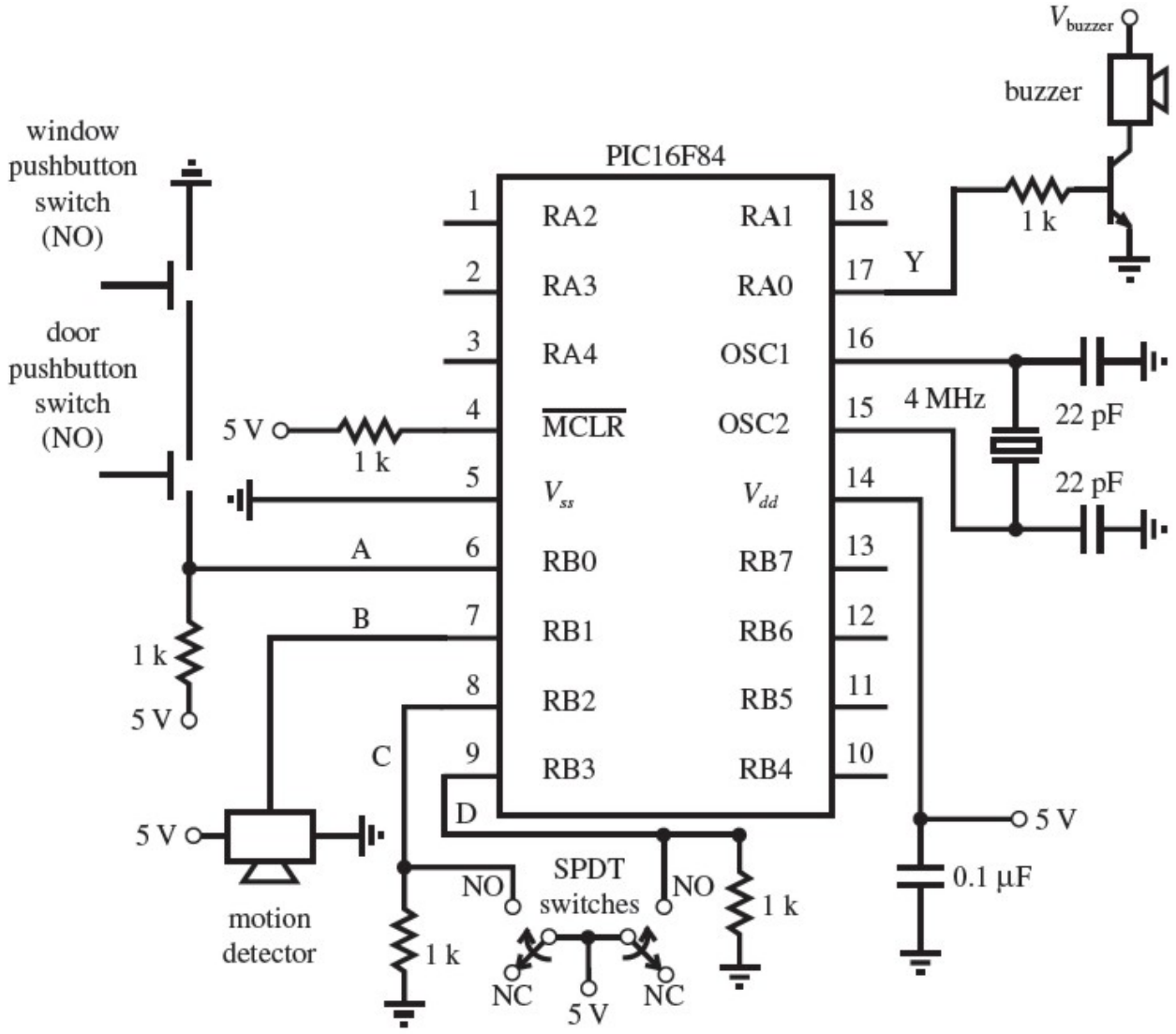
Math operator or function	Description
A + B	Add A and B
A − B	Subtract B from A
A * B	Multiply A and B
A / B	Divide A by B
A // B	Return the remainder (modulus) of the division of B into A
A << n	Shift A n bits to the left
A >> n	Shift A n bits to the right
COS A	Return the cosine of A
A MAX B	Return the maximum of A and B
A MIN B	Return the minimum of A and B
SIN A	Return the sine of A
SQR A	Return the square root of A
A & B	Return the bitwise AND of A and B
A | B	Return the bitwise OR of A and B
A ^ B	Return the bitwise Exclusive OR of A and B
~A	Return the bitwise NOT of A

Table 7.3 Selected PicBasic Pro math operators and functions (p. 285)

Table 7.4 PicBasic Pro logical comparison operators

Operator	Description
= or ==	equal
<> or !=	not equal
<	less than
>	greater than
<=	less than or equal to
>=	greater than or equal to
&&	"And" compound comparison
||	"Or" compound comparison
~	"Not" logical inversion
^^	"Xor" (exclusive "Or") logical comparison

Table 7.4 PicBasic Pro logical comparison operators (p. 287)



Example 7.5 PicBasic Pro Program for the Home Security System Example (p. 286)

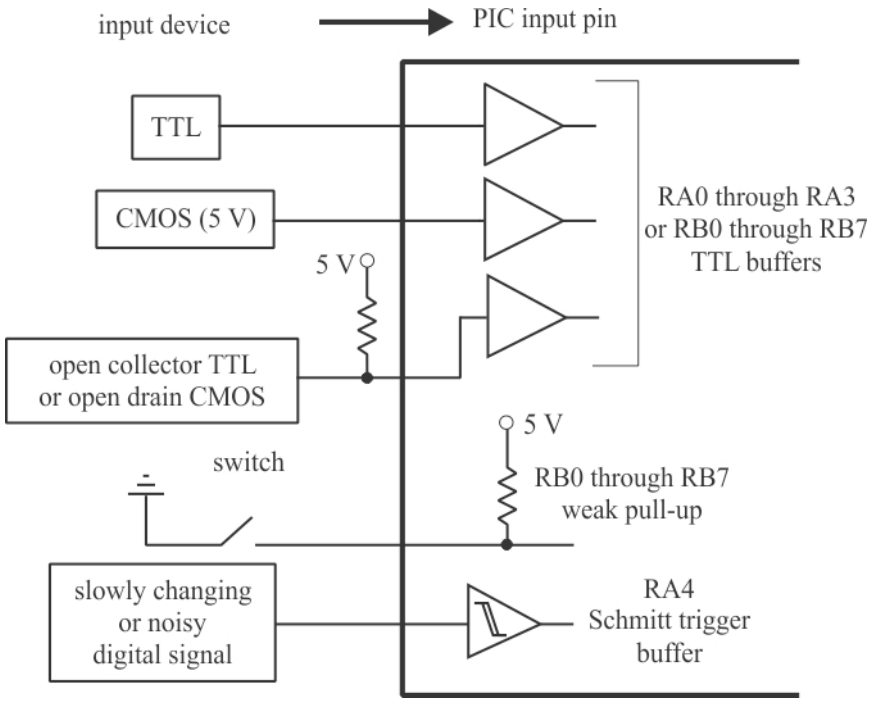


Figure 7.19 Interface circuits for input devices (p. 329)

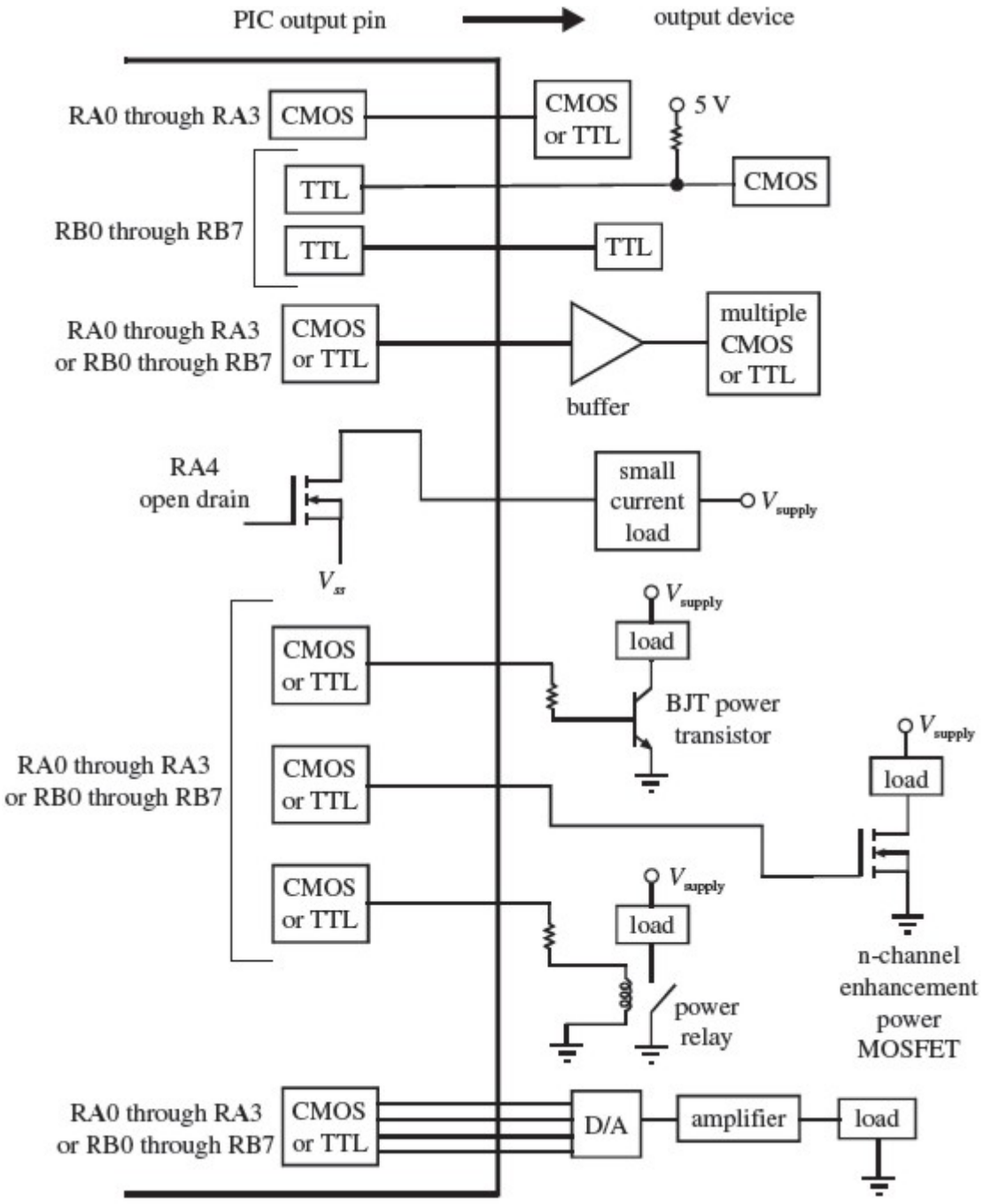


Figure 7.20 Interface circuits for output devices (p. 330)

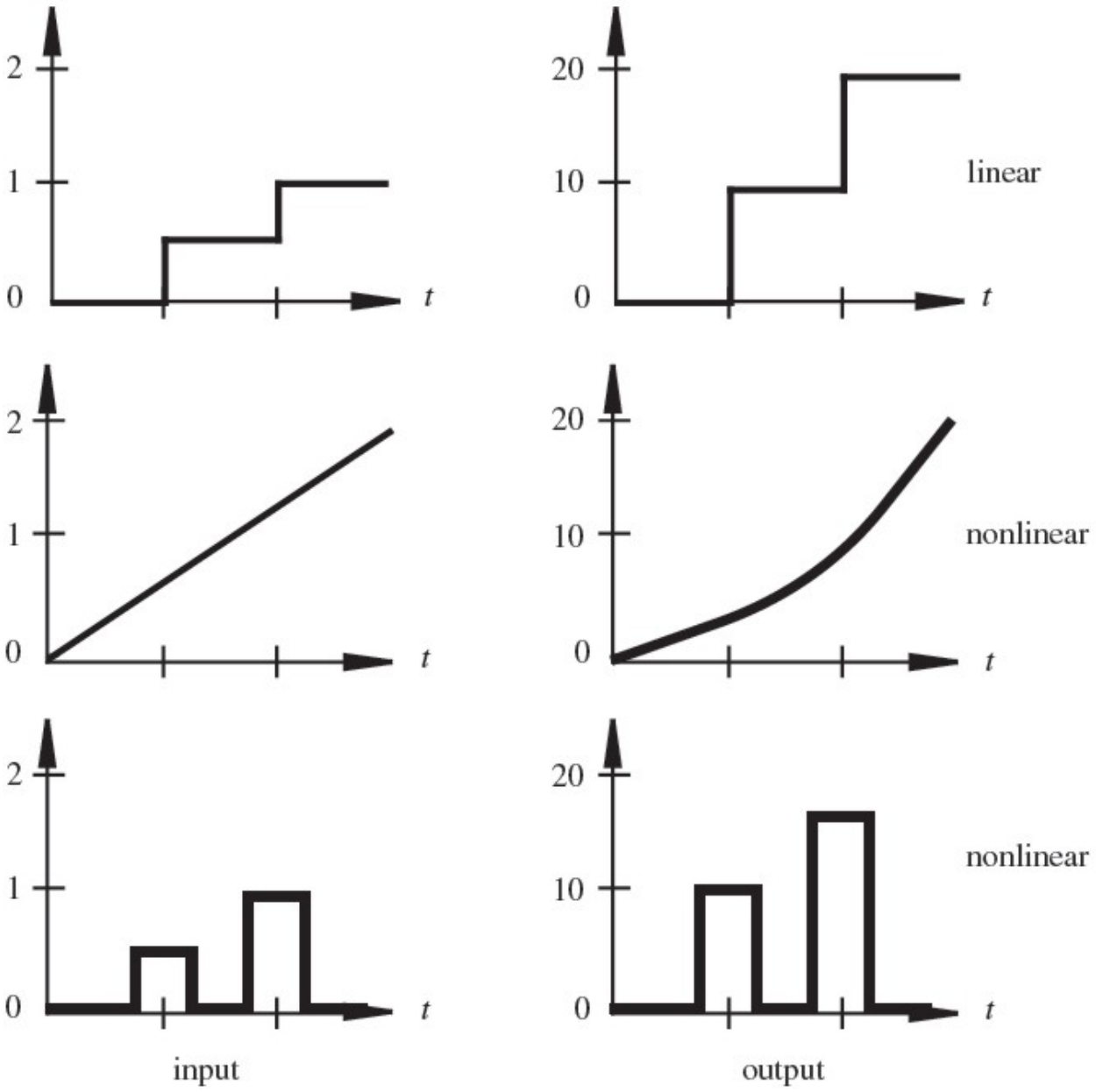


Figure 4.2 Amplitude linearity and nonlinearity (p. 125)

FOURIER SERIES REPRESENTATION OF SIGNALS

$$F(t) = C_0 + \sum_{n=1}^{\infty} A_n \cos(n\omega_0 t) + \sum_{n=1}^{\infty} B_n \sin(n\omega_0 t) \tag{4.3}$$

$$A_n = \frac{2}{T}\int_0^T F(t)\cos(n\omega_0 t)\mathrm{d}t \tag{4.4}$$

$$B_n = \frac{2}{T}\int_0^T F(t)\sin(n\omega_0 t)\mathrm{d}t \tag{4.5}$$

$$C_0 = \frac{1}{T}\int_0^T F(t)\mathrm{d}t = \frac{A_0}{2} \tag{4.6}$$

Section 4.3 FOURIER SERIES REPRESENTATION OF SIGNALS (pg. 126)

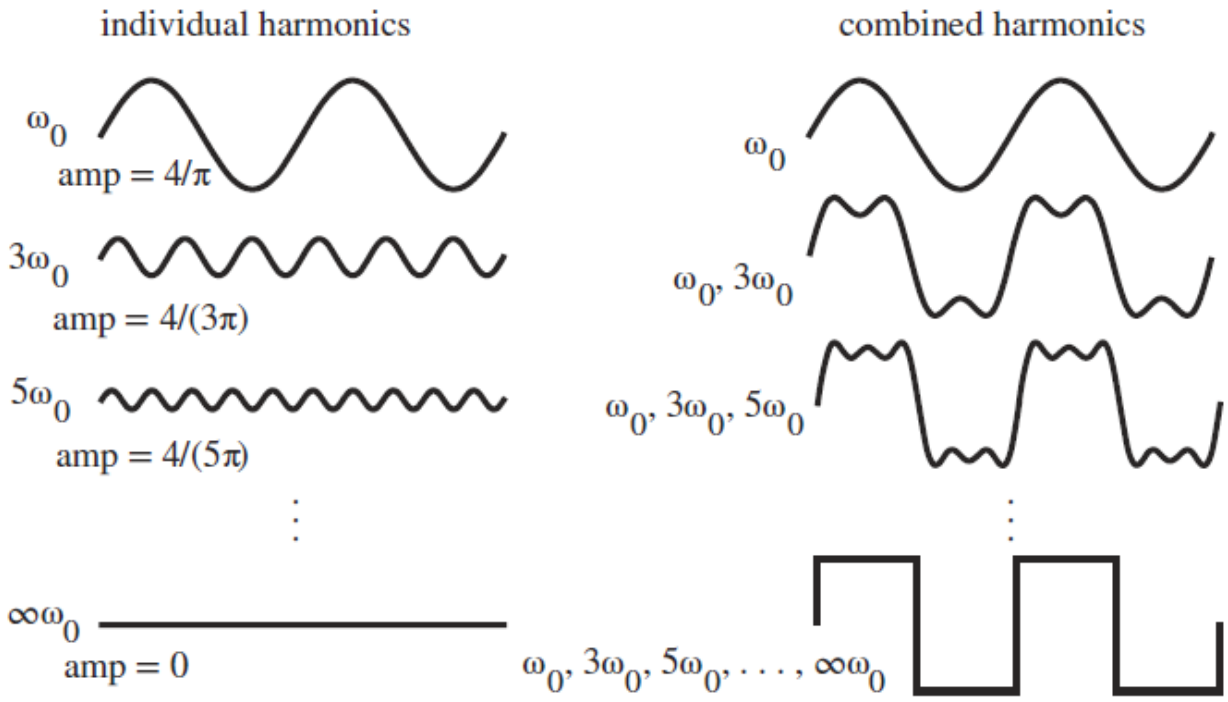


Figure 4.4 Harmonic decomposition of a square wave (p. 128)

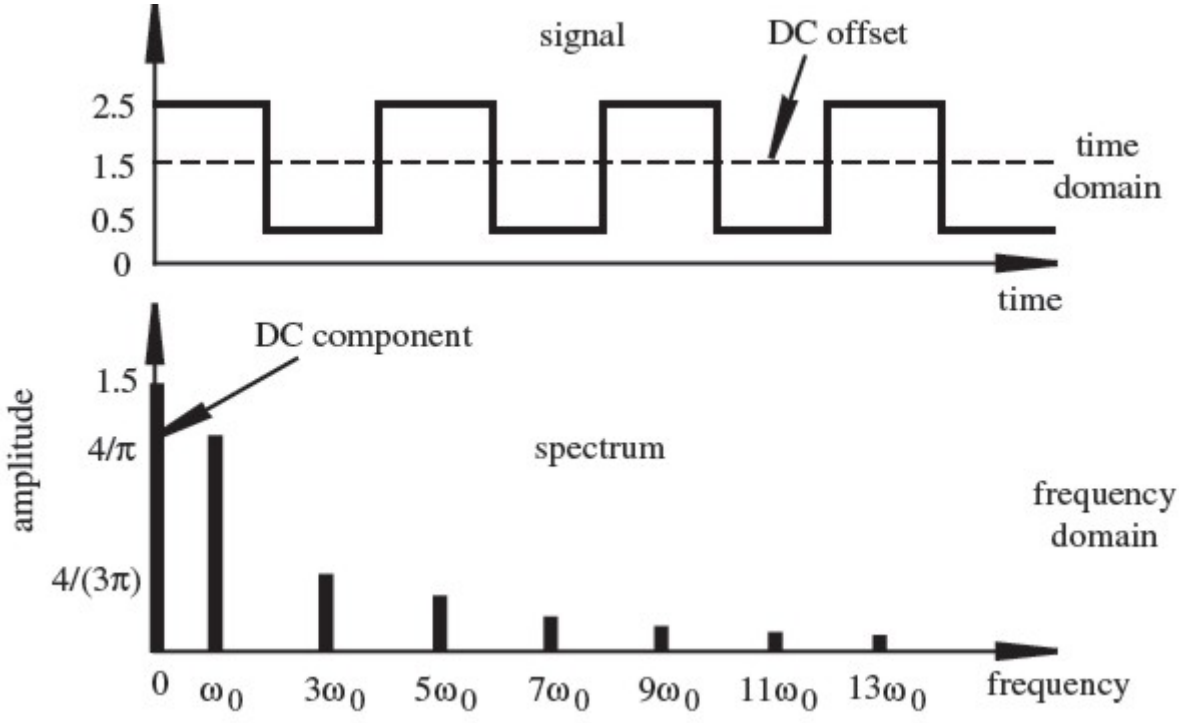


Figure 4.5 Spectrum of a square wave (p. 129)

4.4 BANDWIDTH AND FREQUENCY RESPONSE

$$\text{dB} = 20 \log_{10}\left(\frac{A_{\text{out}}}{A_{\text{in}}}\right) \tag{4.17}$$

$$\frac{P_{\text{out}}}{P_{\text{in}}} = \frac{1}{2} \tag{4.19}$$

$$\frac{A_{\text{out}}}{A_{\text{in}}} = \sqrt{\frac{P_{\text{out}}}{P_{\text{in}}}} = \sqrt{\frac{1}{2}} \approx 0.707 \tag{4.20}$$

$$\text{dB} = 20 \log_{10} \sqrt{\frac{1}{2}} \approx -3 \text{ dB} \tag{4.21}$$

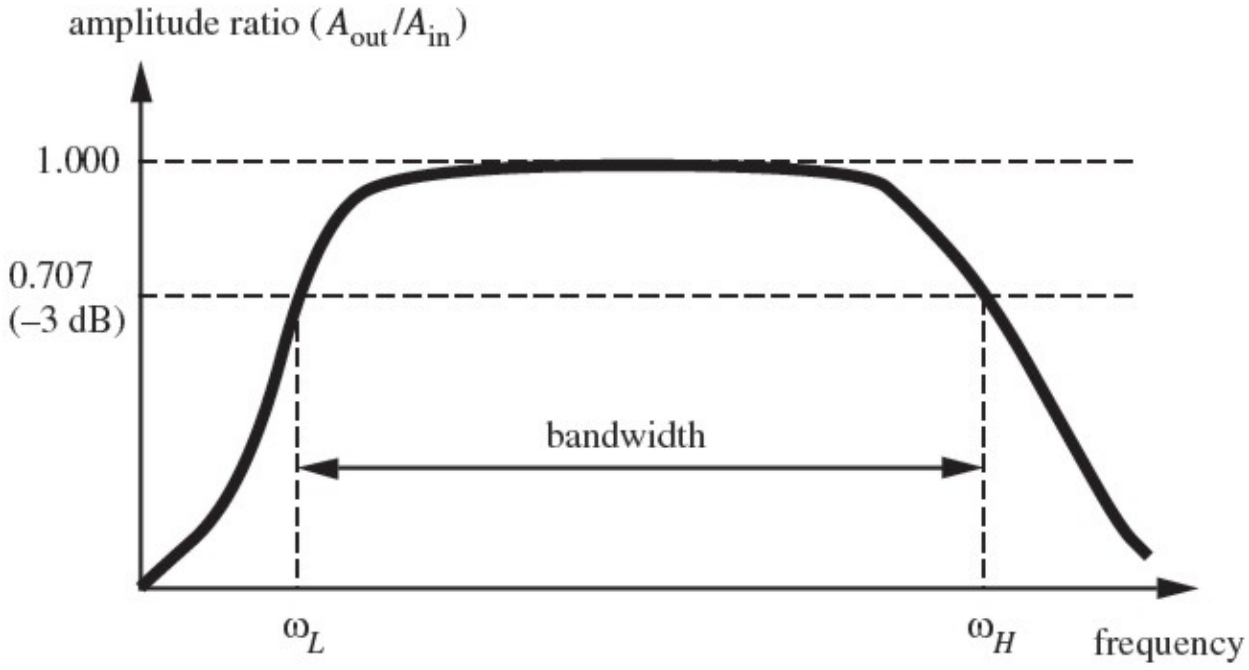


Figure 4.6 Frequency response and bandwidth (p. 130)

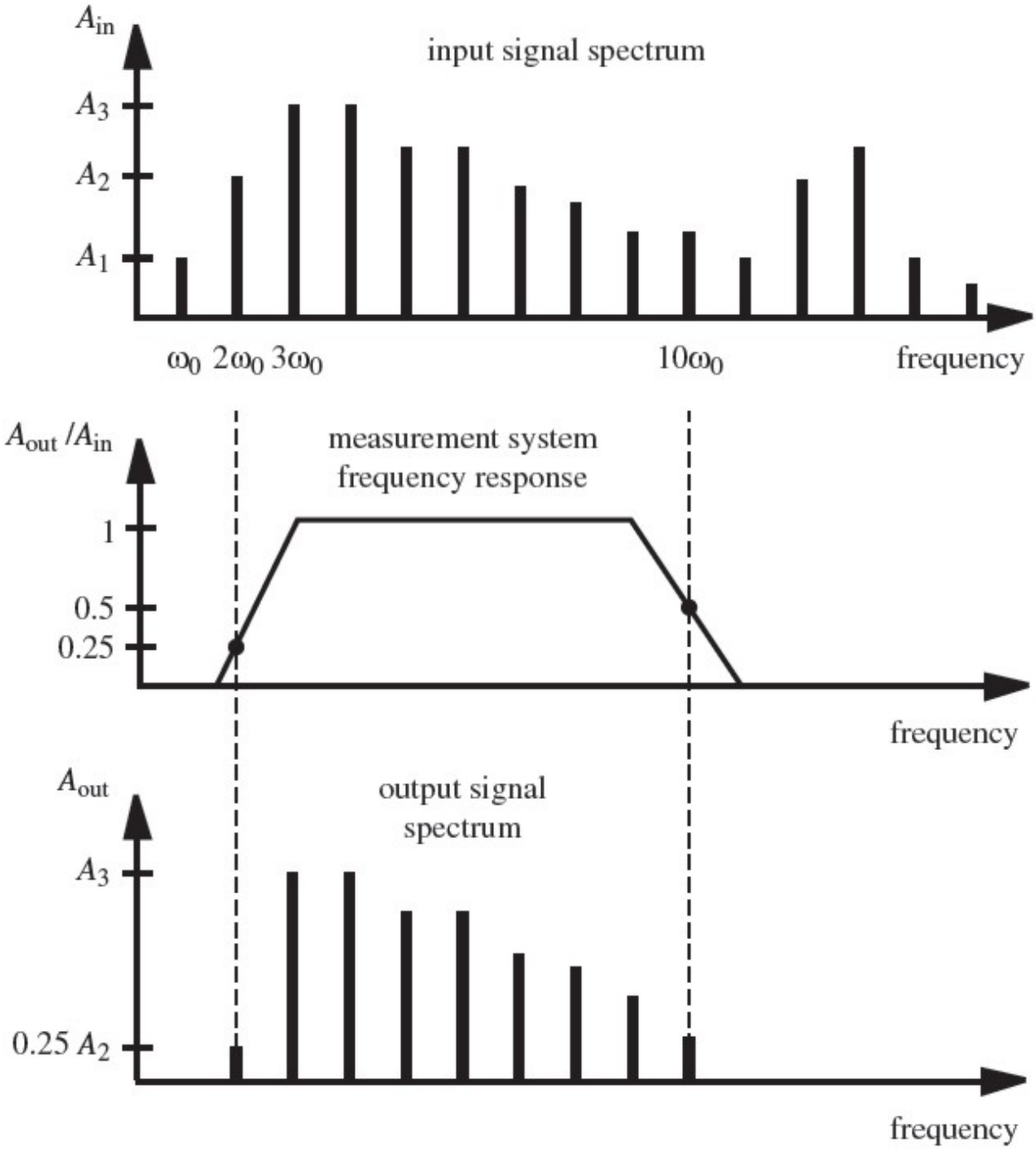
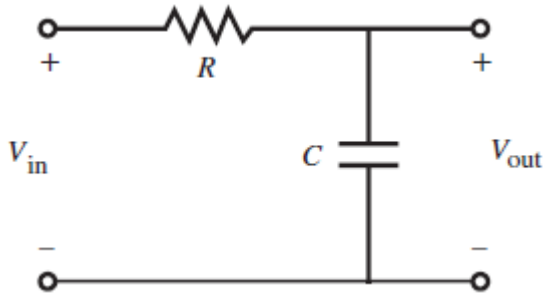


Figure 4.7 Effect of measurement system bandwidth on signal spectrum (p. 132)



$$V_{out} = \frac{\frac{1}{j\omega C}}{\frac{1}{j\omega C} + R} V_{in}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{j\omega RC + 1}$$

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{1}{\sqrt{1 + (\omega RC)^2}}$$

$$\omega_c = \frac{1}{RC}$$

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{1}{\sqrt{2}} = 0.707$$

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{1}{\sqrt{1 + (\omega/\omega_c)^2}}$$

Example 4.1 Bandwidth of an Electrical Network (p. 133)

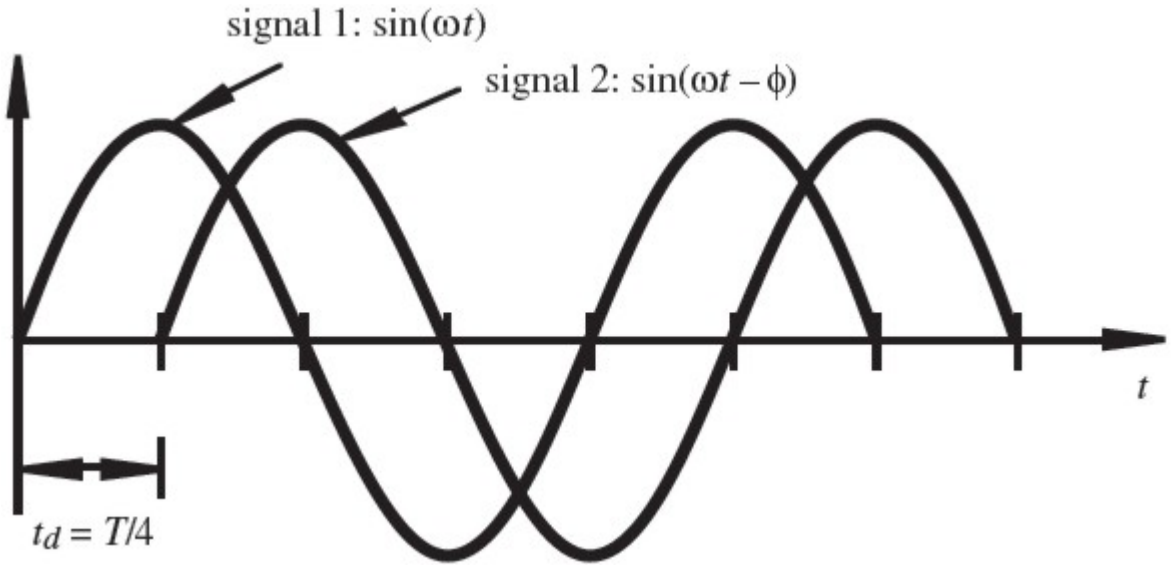


Figure 4.8 Relationship between phase and time displacement (p. 135)

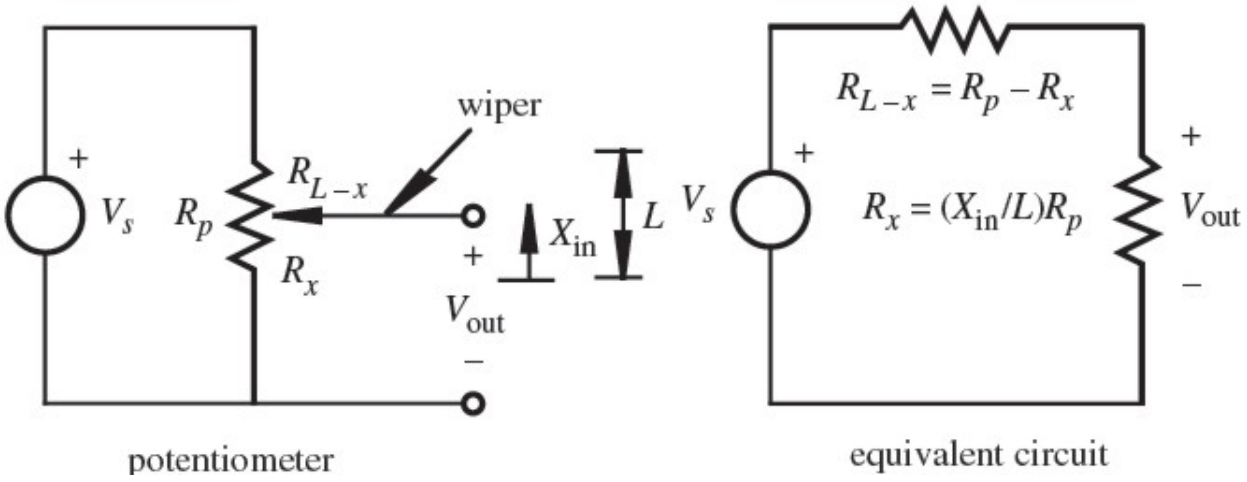


Figure 4.11 Displacement potentiometer (p. 138)

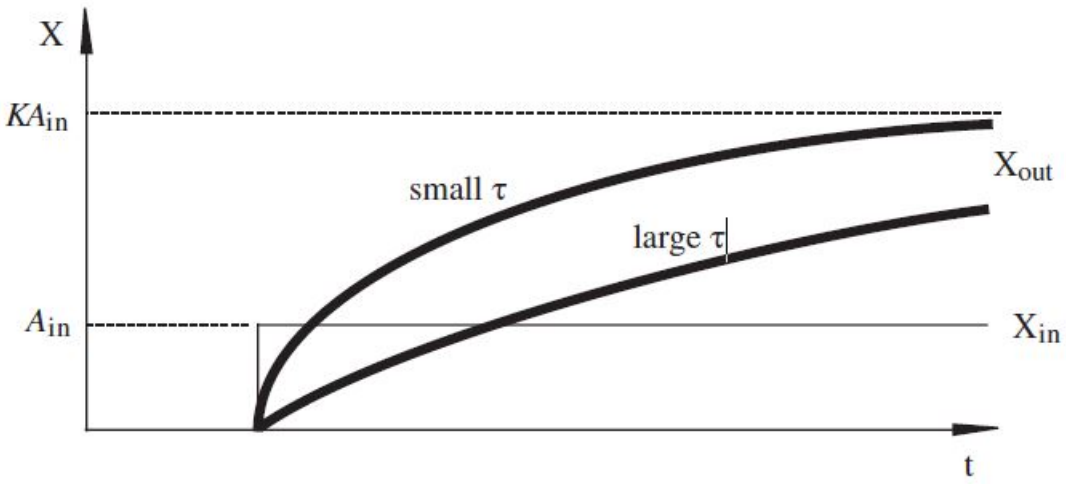


Figure 4.12 First-order response (p. 141)

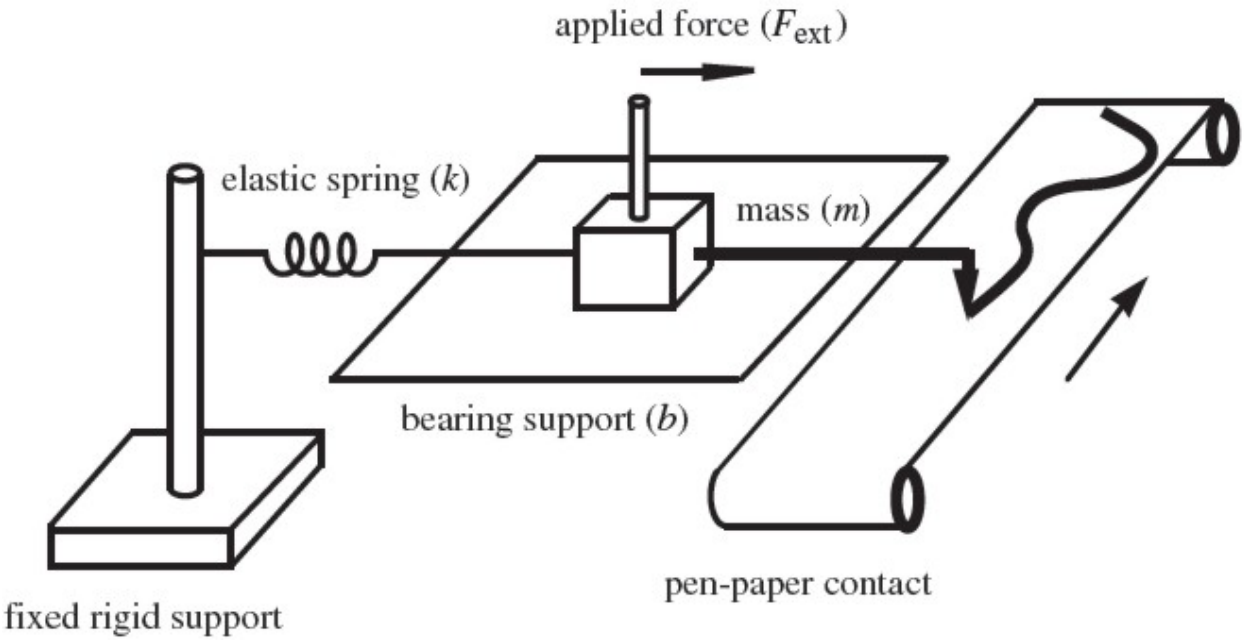


Figure 4.15 Strip chart recorder as an example of a second-order system (p. 144)

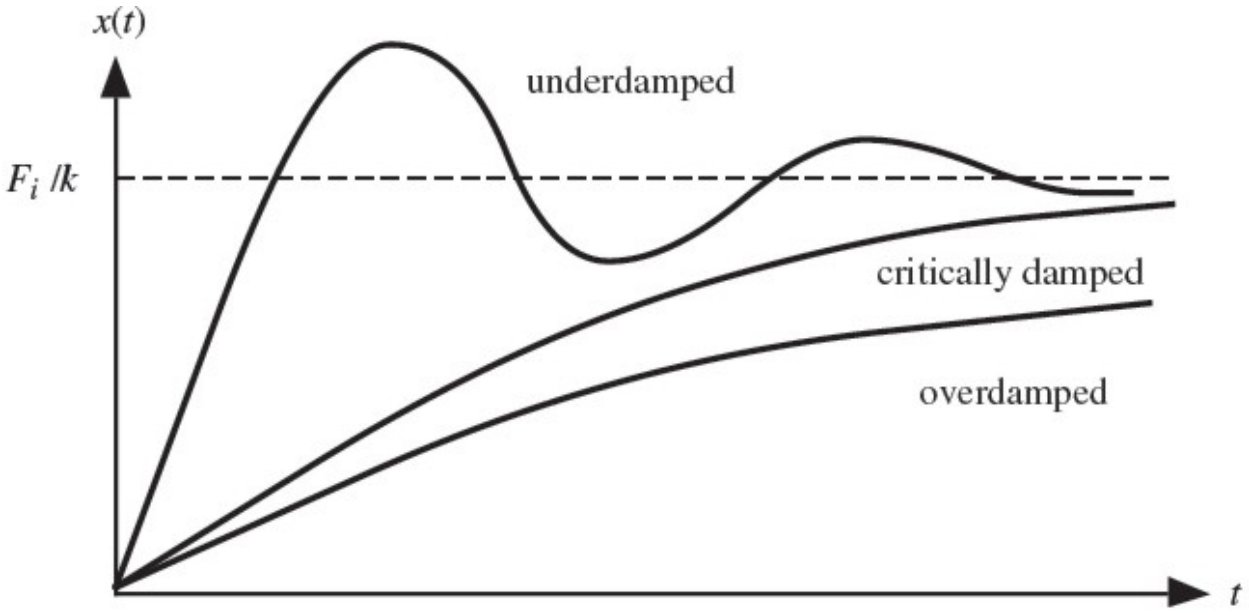


Figure 4.17 Second-order step responses (p. 148)

4.10.2 Frequency Response of a System

$$F_{ext}(t) = F_i \sin(\omega t)$$

$$x(t) = X_o \sin(\omega t + \phi)$$

Analytical Procedure to Determine the Frequency Response of a System

1. *Find the Laplace transform of the system differential equation assuming initial conditions are zero:* $x(0) = dx/dt\ (0) = 0$. *The Laplace transform converts the differential equation into an algebraic equation that is related to the frequency response of the system.*

$$\frac{d^2x(t)}{dt^2} + 2\zeta\omega_n\frac{dx(t)}{dt} + \omega_n{}^2x(t) = \frac{\omega_n{}^2}{k}F_{ext}(t) \tag{4.78}$$

$$(s^2 + 2\zeta\omega_n s + \omega_n{}^2)X(s) = \frac{\omega_n{}^2}{k}F_{ext}(s) \tag{4.79}$$

2. *Find the* **transfer function** *of the system, which is the ratio of the output and input Laplace transforms.*

$$G(s) = \frac{X(s)}{F_{ext}(s)} = \frac{\frac{\omega_n{}^2}{k}}{(s^2 + 2\zeta\omega_n s + \omega_n{}^2)} \tag{4.80}$$

3. *To simulate a harmonic input, replace* s *with* $j\omega$ *in the transfer function. This yields the frequency response behavior of the system.*

$$G(j\omega) = \frac{1/k}{\left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right] + j\left(2\zeta\frac{\omega}{\omega_n}\right)} \tag{4.81}$$

4. *Find the desired* ***amplitude ratio*** *between the output and input by determining the magnitude of the complex transfer function:*

$$\text{mag}[G(j\omega)] = |G(j\omega)| \tag{4.82}$$

$$\frac{X_o}{F_i/k} = \frac{1}{\left\{\left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]^2 + 4\zeta^2\left(\frac{\omega}{\omega_n}\right)^2\right\}^{1/2}} \tag{4.83}$$

5. *Find the* ***phase angle*** ϕ *between the output and input by determining the argument of the complex transfer function:*

$$\phi = \arg[G(j\omega)] = \angle G(j\omega) \tag{4.84}$$

$$\phi = 0 - \tan^{-1}\left\{\frac{2\zeta\frac{\omega}{\omega_n}}{\left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]}\right\} = -\tan^{-1}\left\{\frac{2\zeta}{\frac{\omega_n}{\omega} - \frac{\omega}{\omega_n}}\right\} \tag{4.85}$$

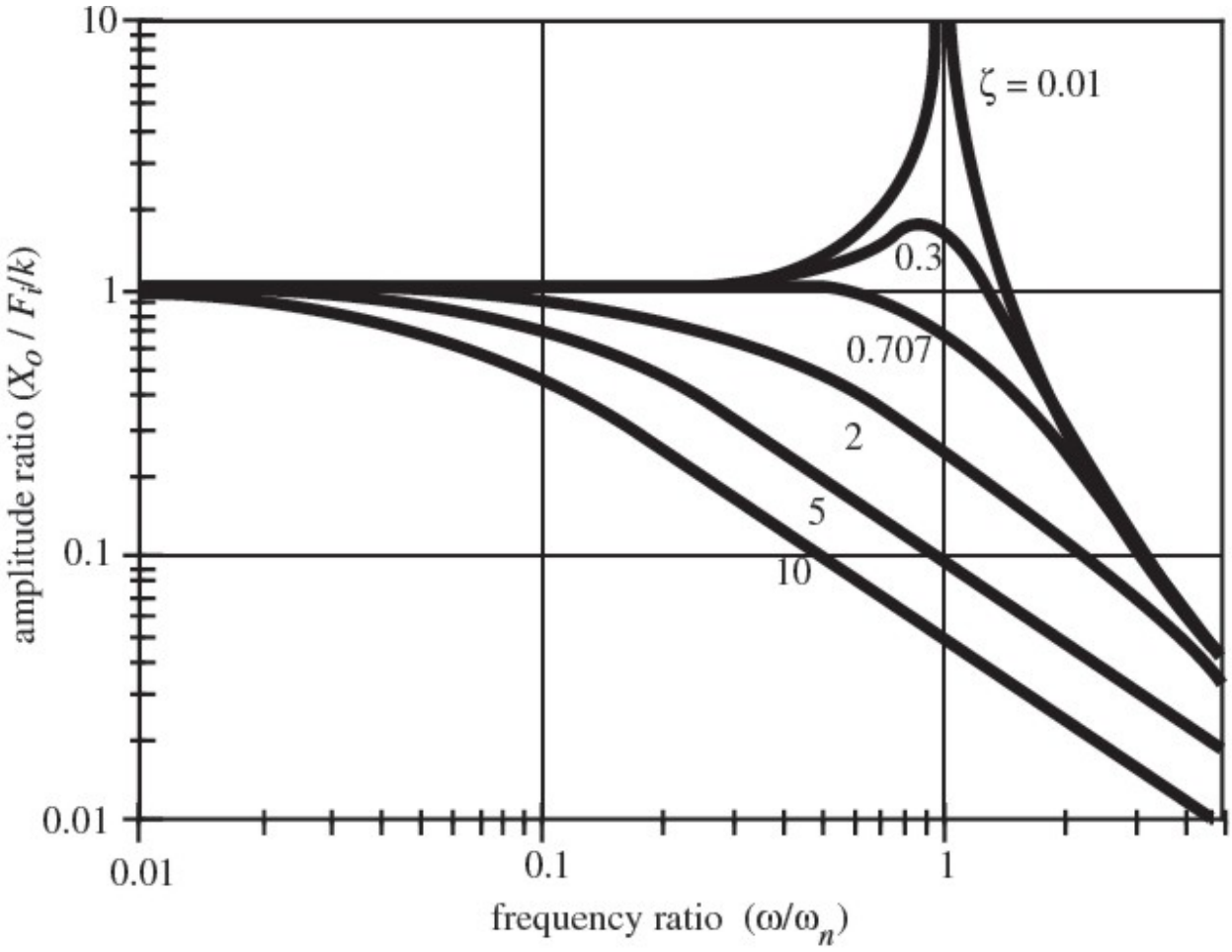


Figure 4.19 Second-order system amplitude response (p. 151)

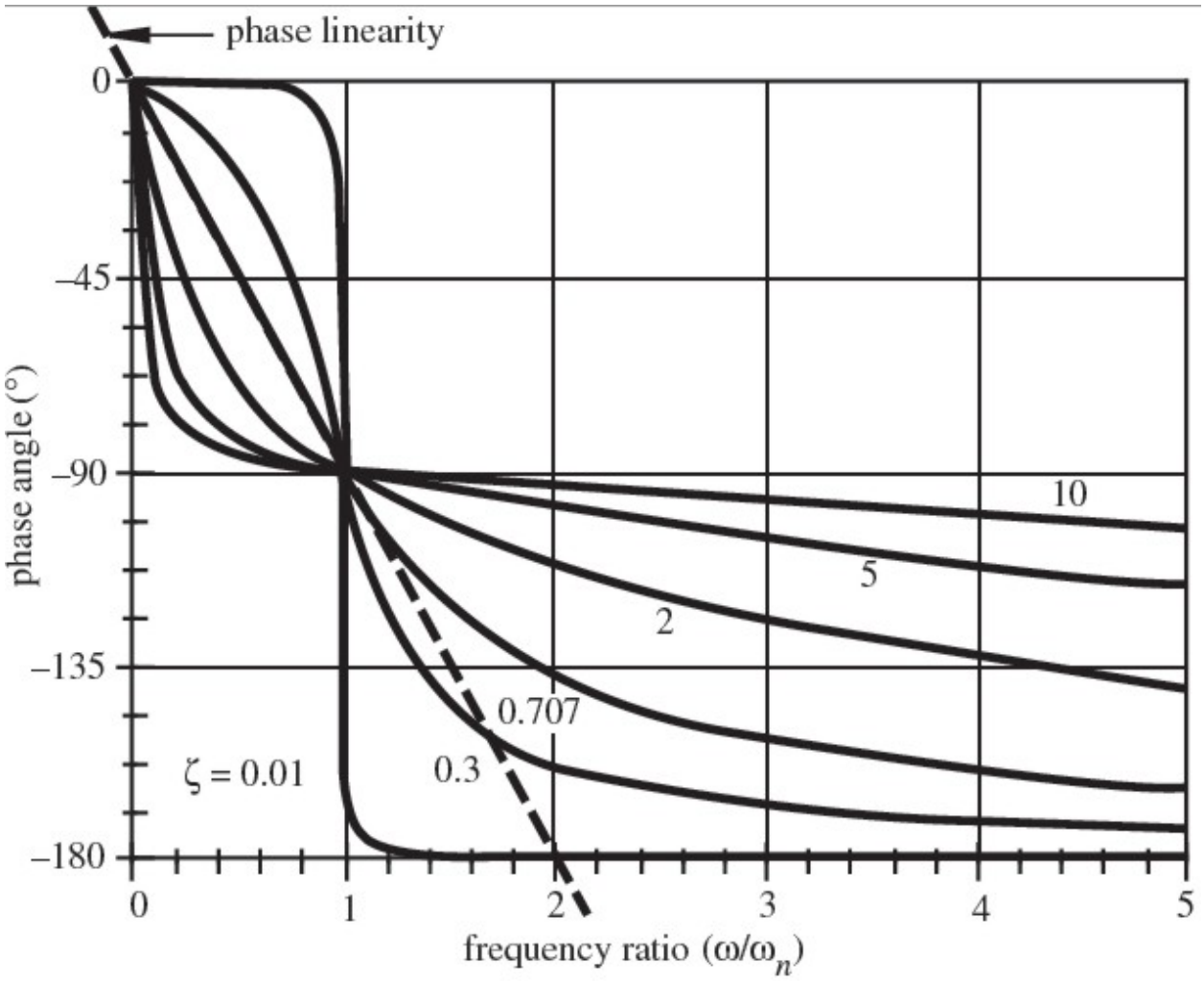


Figure 4.20 Second-order system phase response (p. 152)

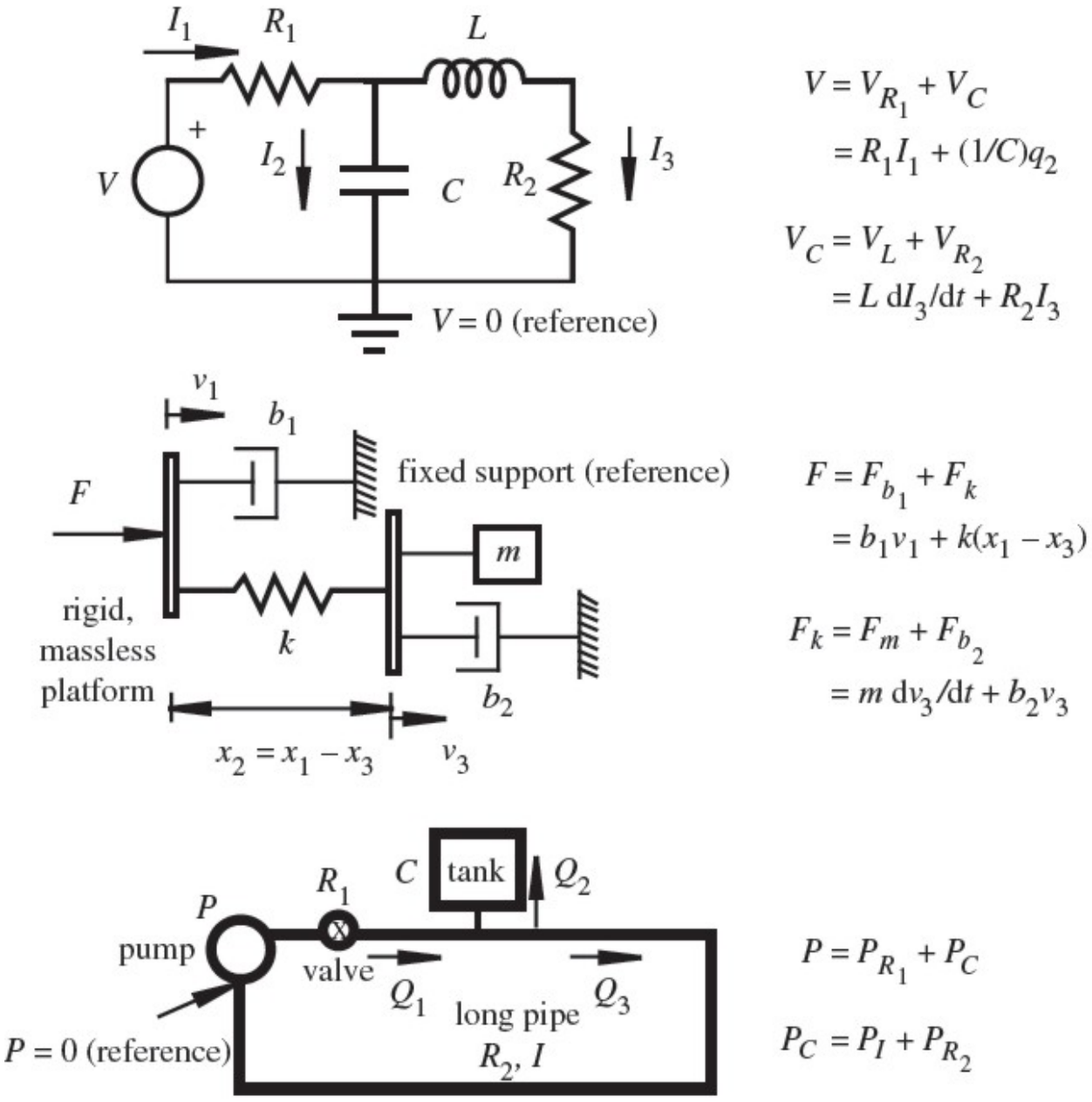


Figure 4.21 Example of system analogies (p. 158)

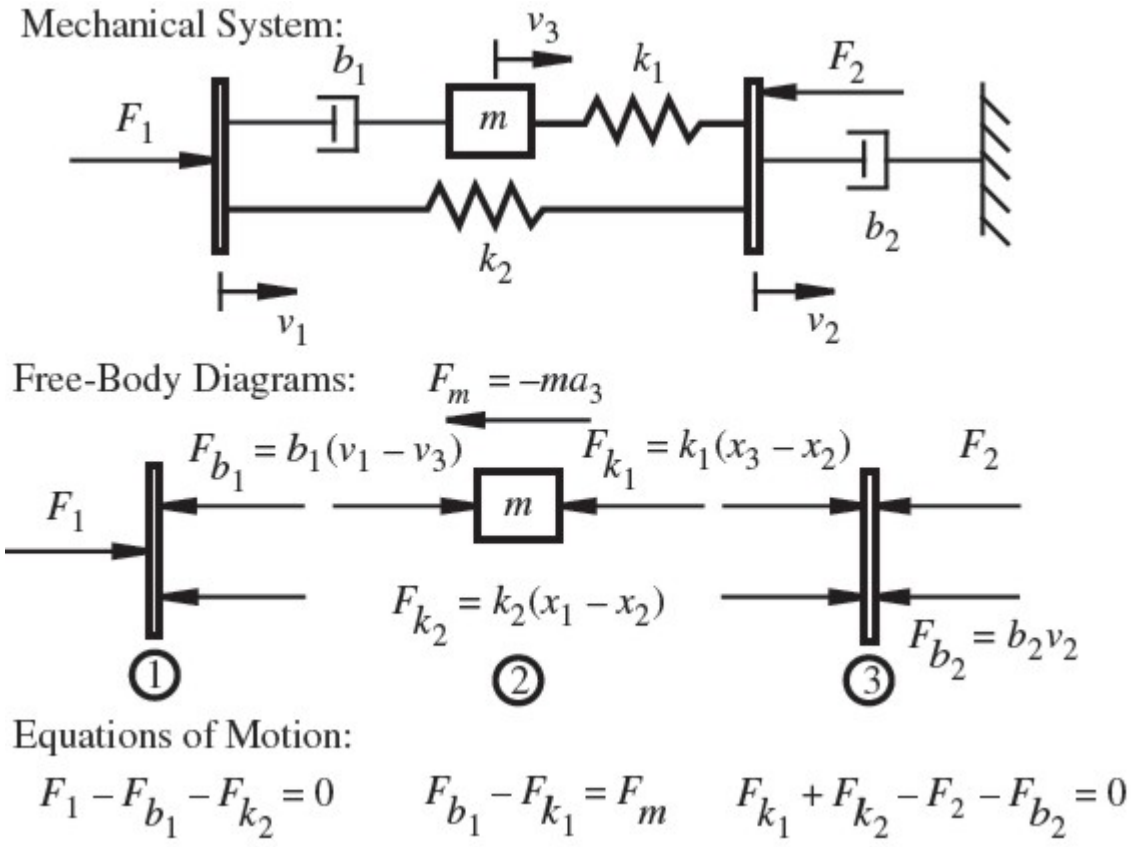


Figure 4.22 Mechanical system analogy example (p. 159)

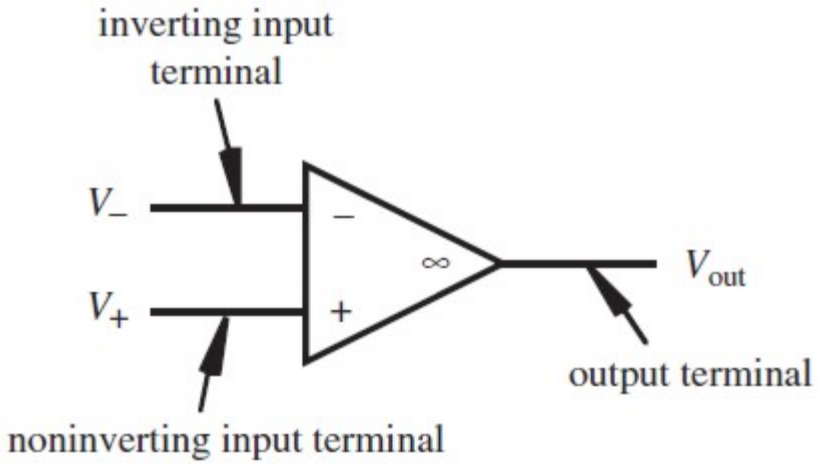


Figure 5.2 Op amp terminology and schematic representation (p. 171)

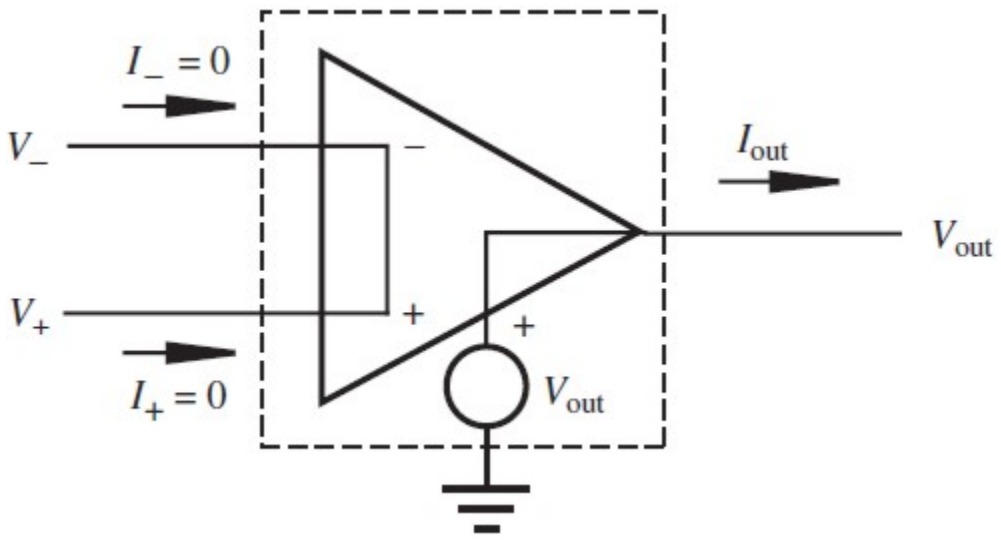


Figure 5.4 Op amp equivalent circuit (p. 172)

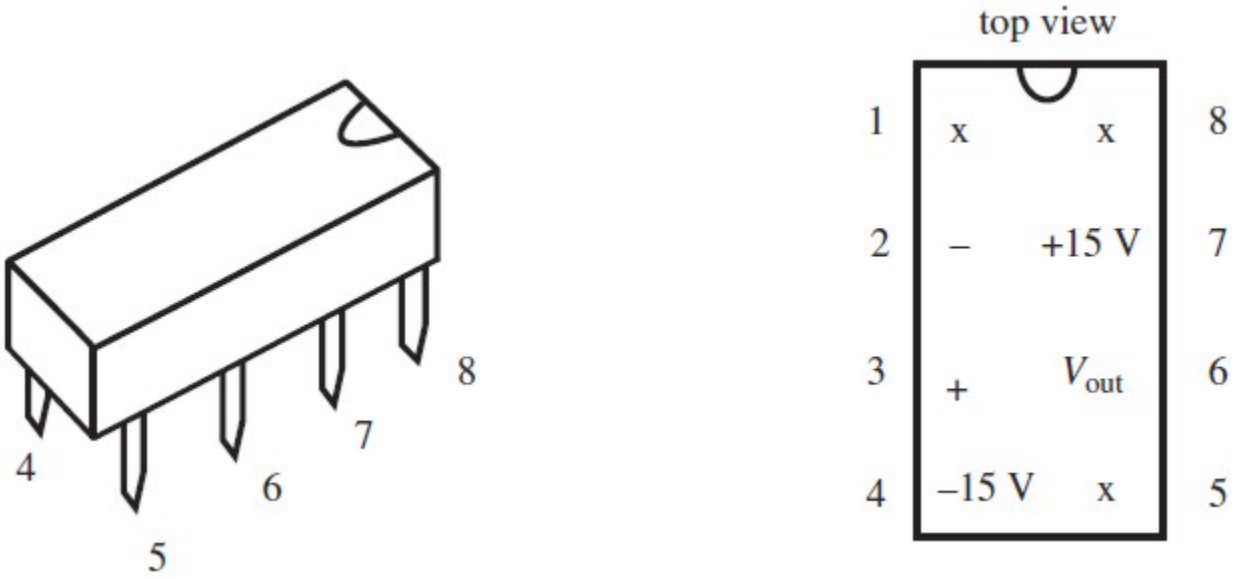


Figure 5.5 741 op amp pin-out (p. 173)

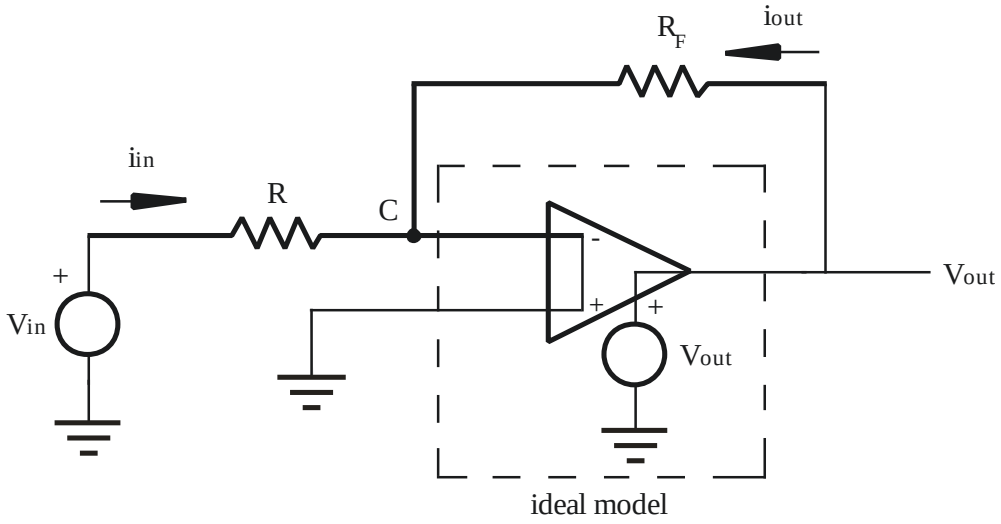
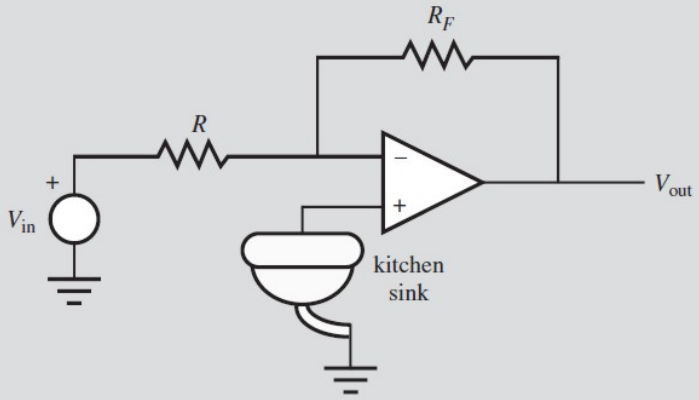


Figure 5.8 Equivalent circuit for an inverting amplifier (p. 175)

■ CLASS DISCUSSION ITEM 5.1

Kitchen Sink in an Op Amp Circuit

Consider the following op amp circuit:



What is the effect of the kitchen sink at the noninverting input of the op amp?

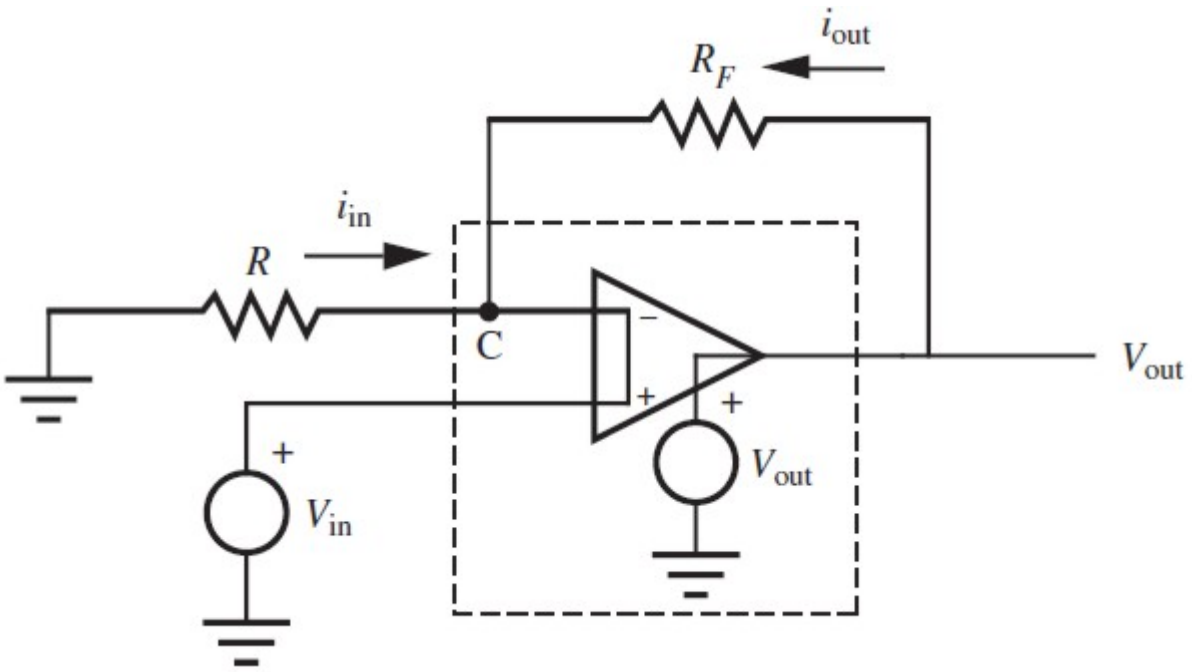


Figure 5.11 Equivalent circuit for a noninverting amplifier (p. 177)

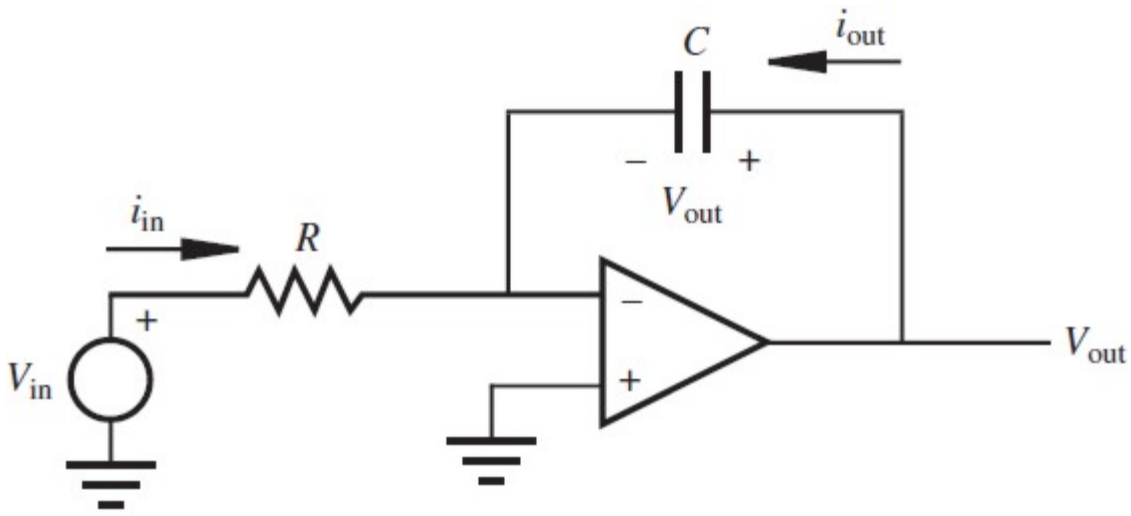


Figure 5.19 Ideal integrator (p. 185)

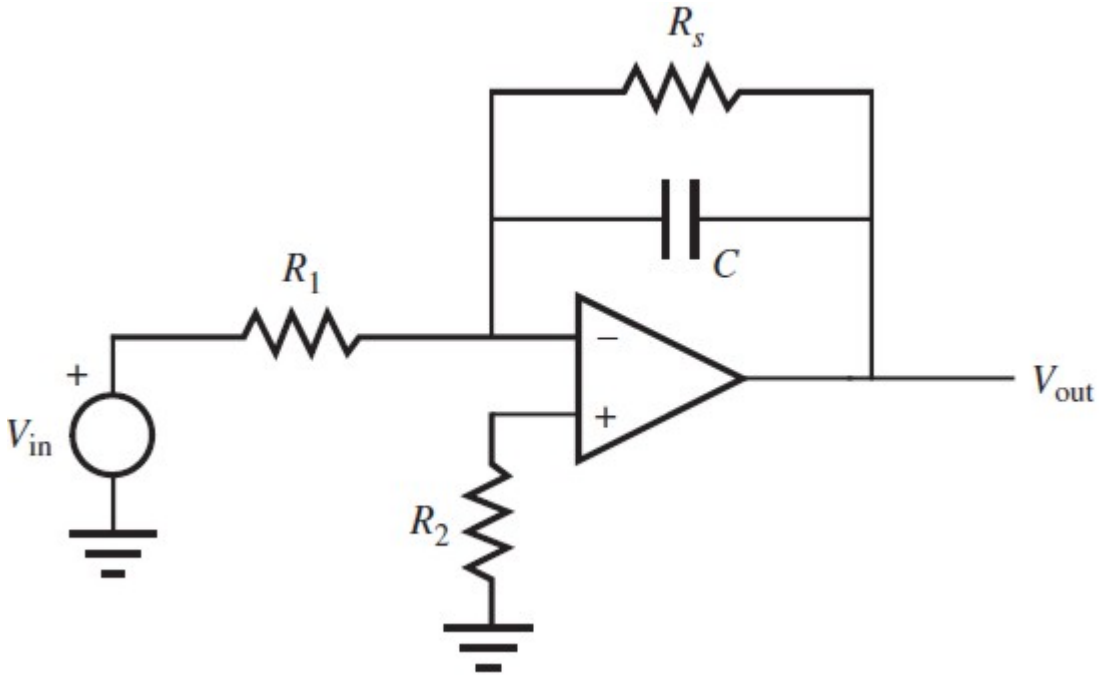


Figure 5.20 Improved integrator (p. 186)

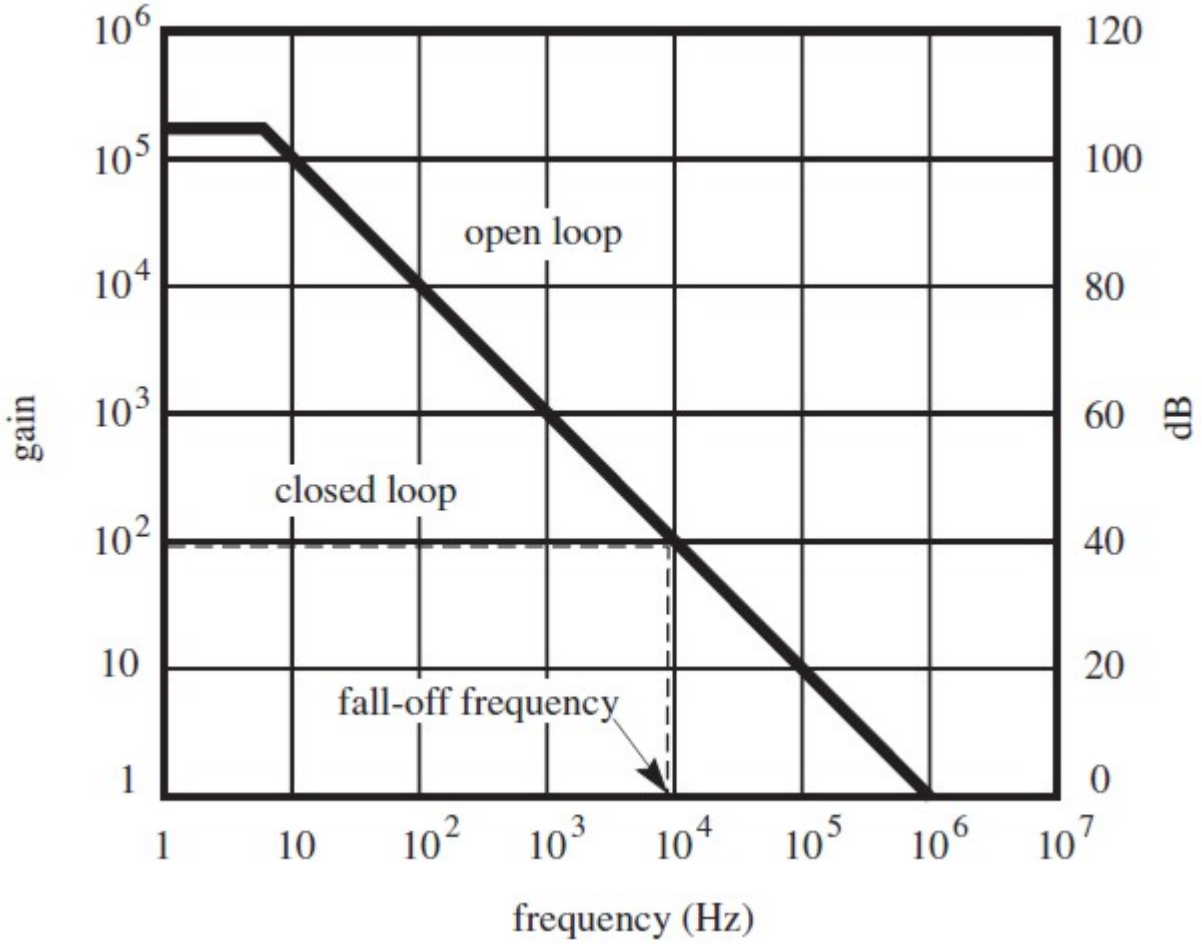
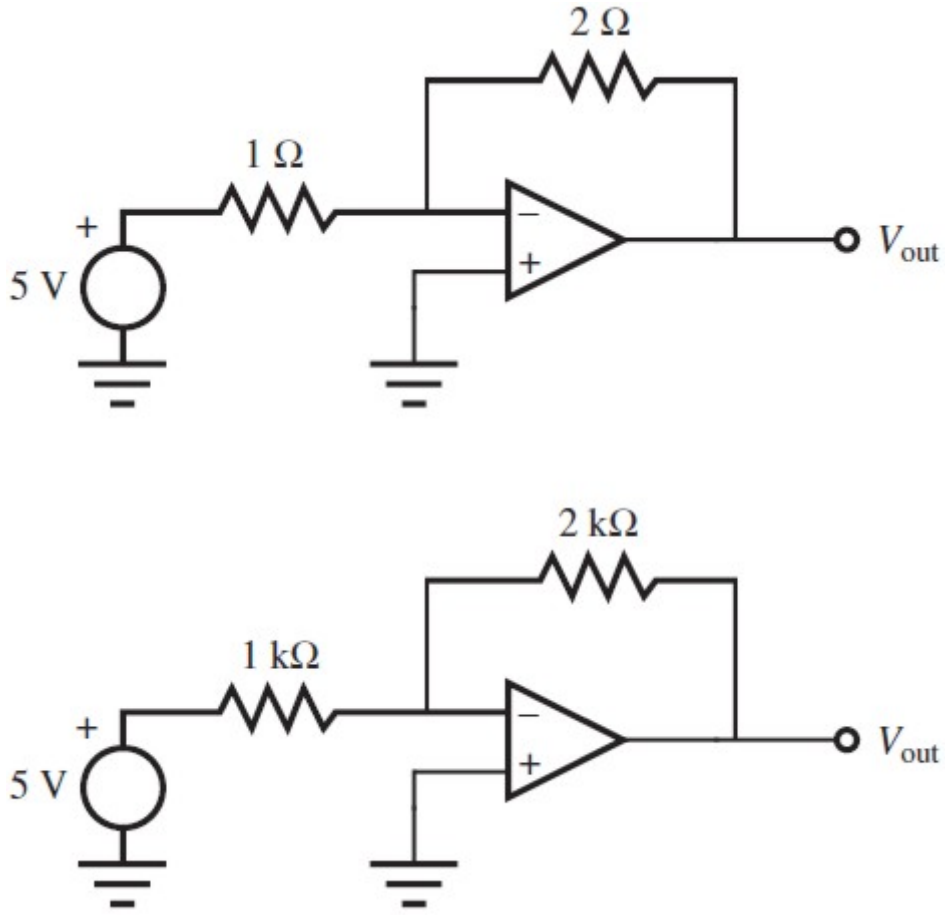


Figure 5.26 Typical op amp open- and closed-loop response (p. 191)



Example 5.1 Sizing Resistors in Op Amp Circuits (p. 195)

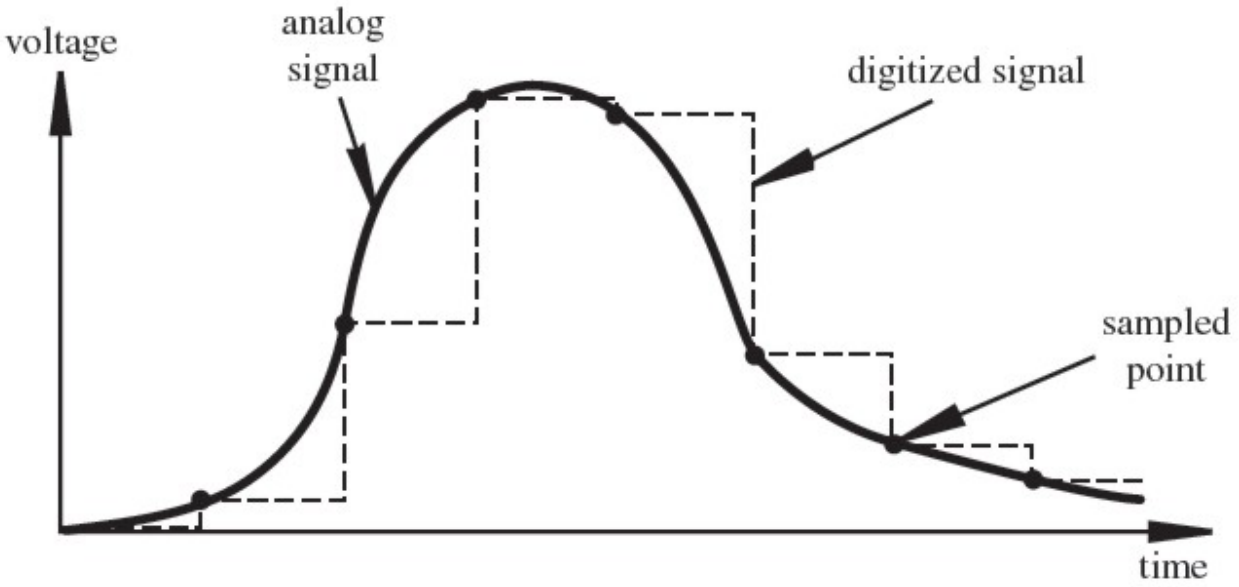


Figure 8.1 Analog signal and sampled equivalent (p. 377)

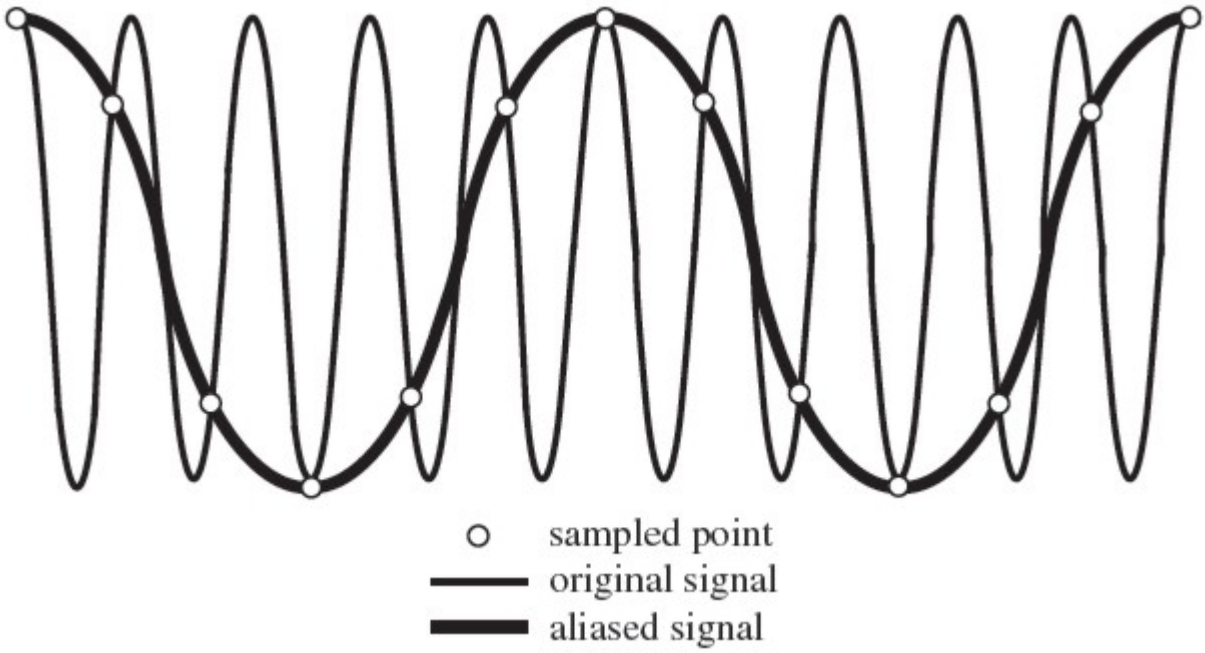
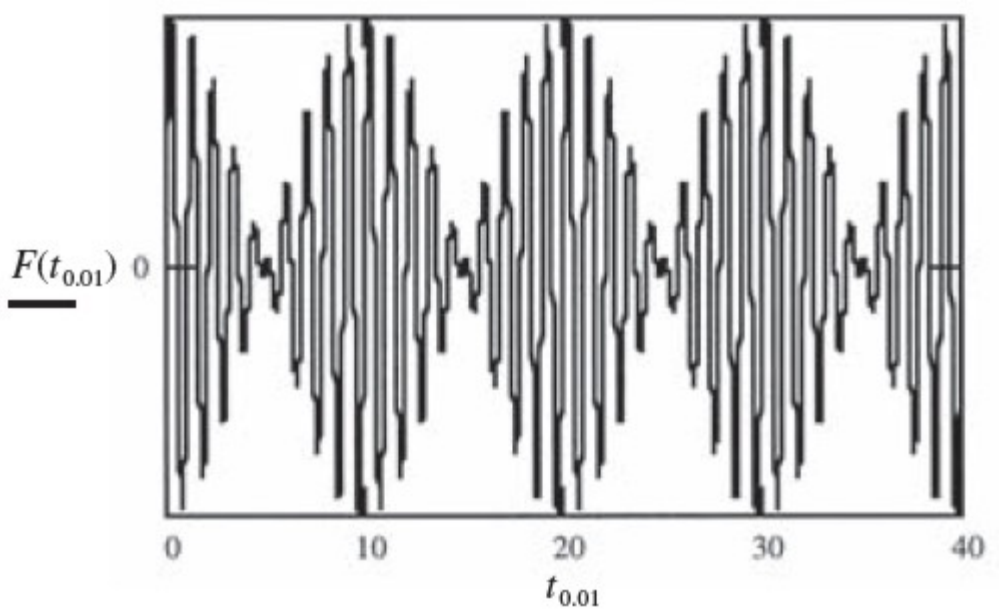
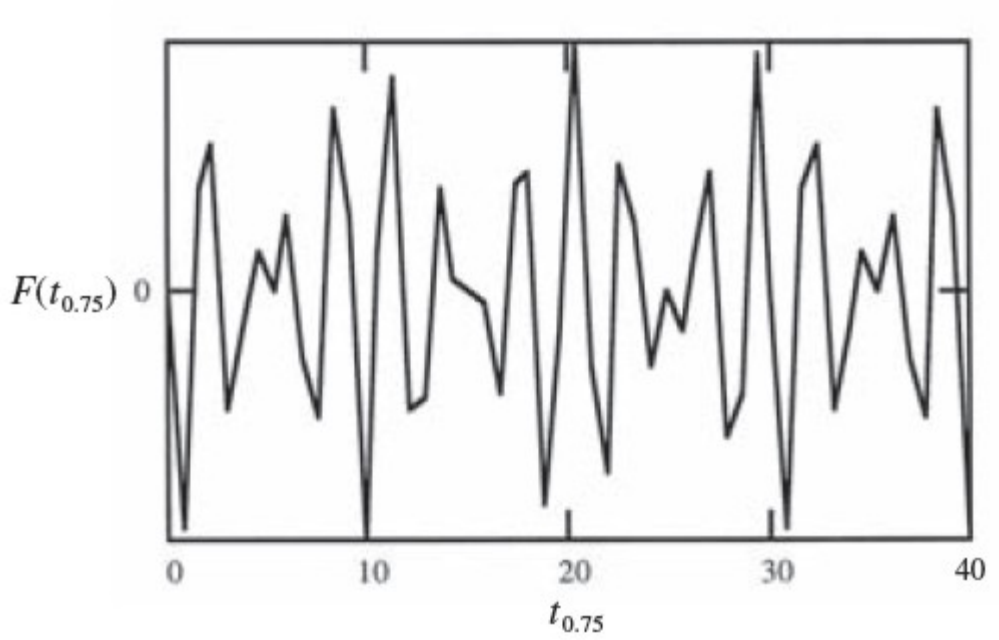


Figure 8.2 Aliasing (p. 378)





Example 8.1 Sampling Theorem and Aliasing (p. 379)

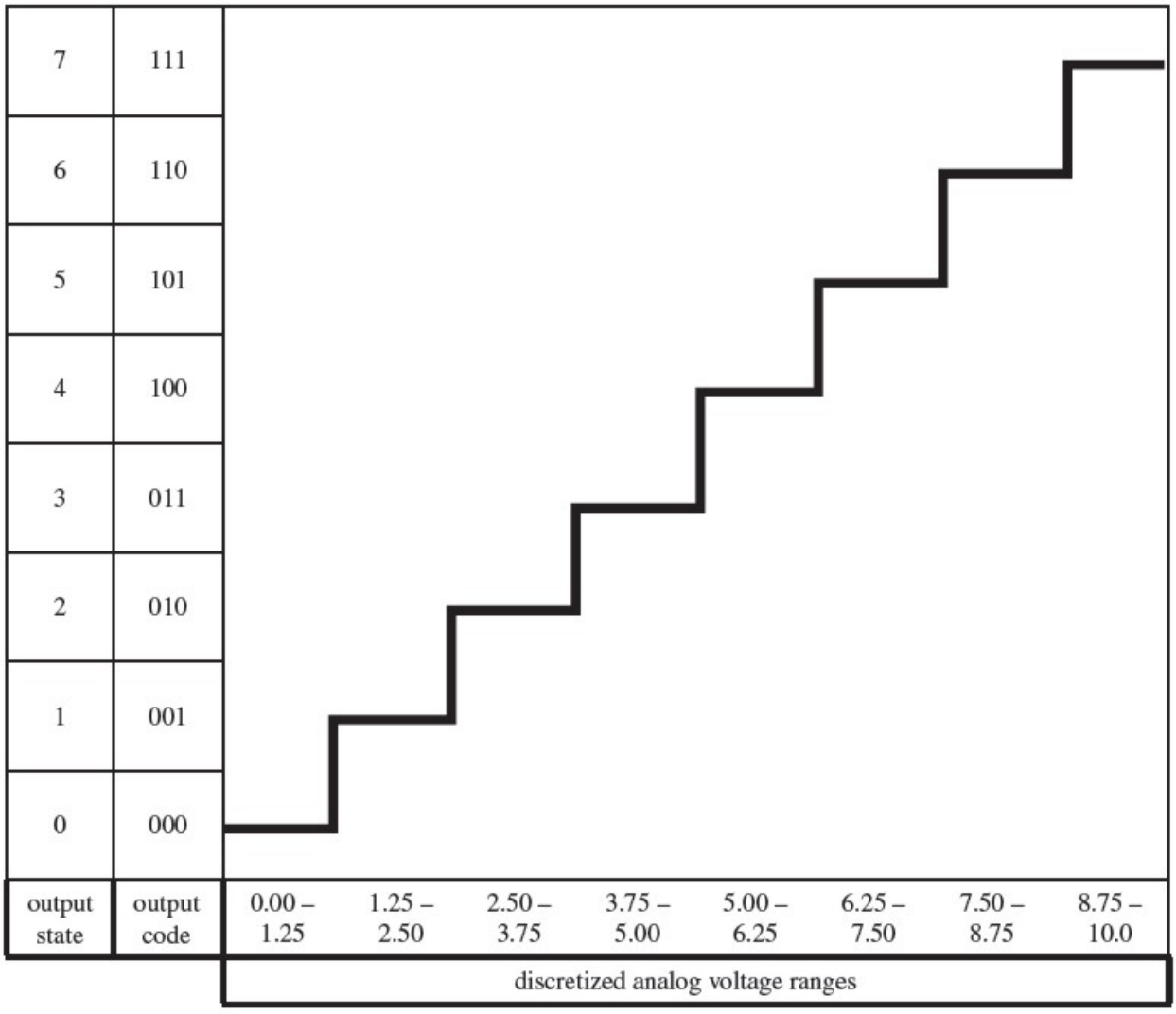


Figure 8.7 Analog-to-digital conversion (p. 384)

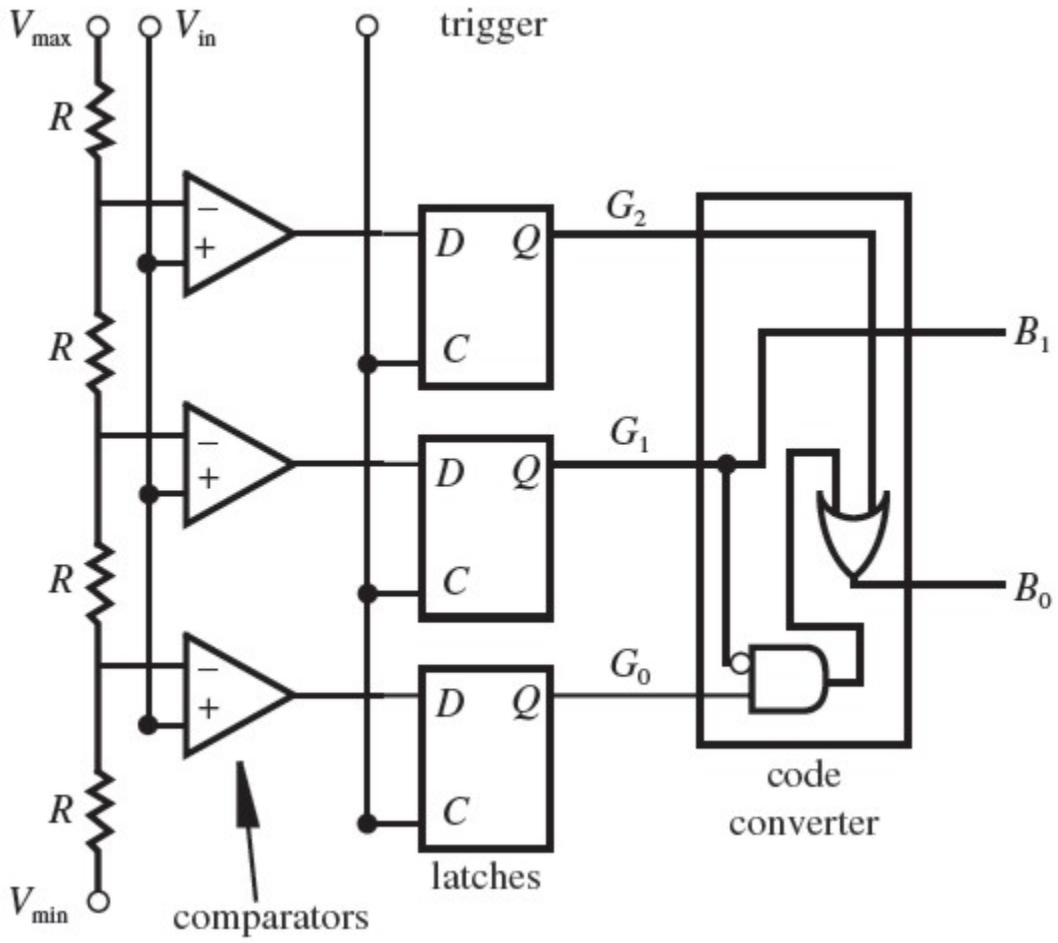


Figure 8.11 A/D flash converter (p. 390)

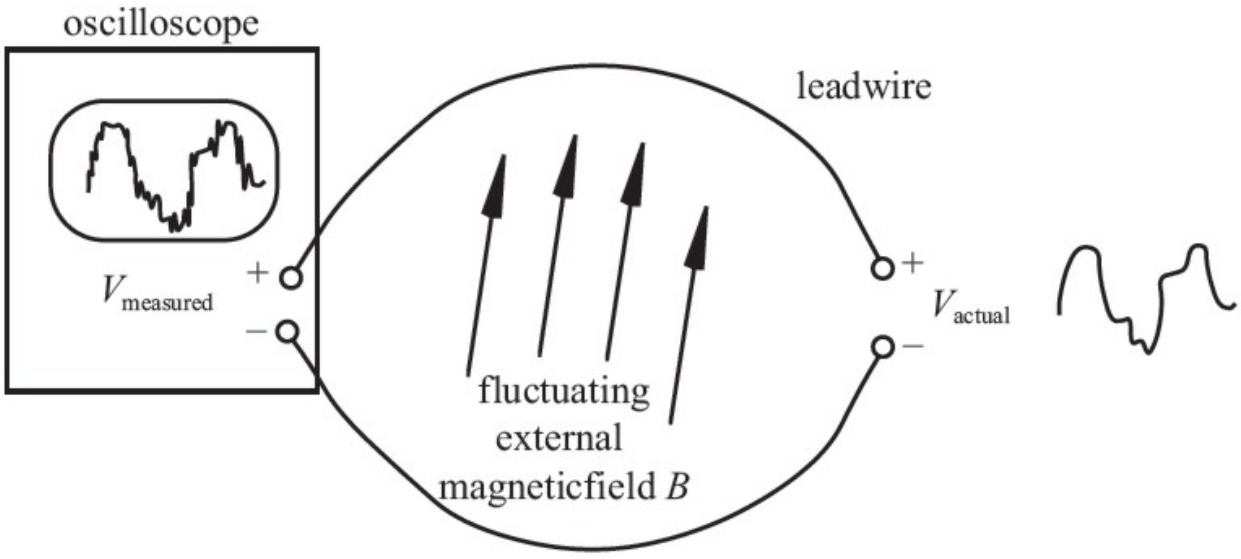


Figure 2.49 Inductive coupling (p. 62)

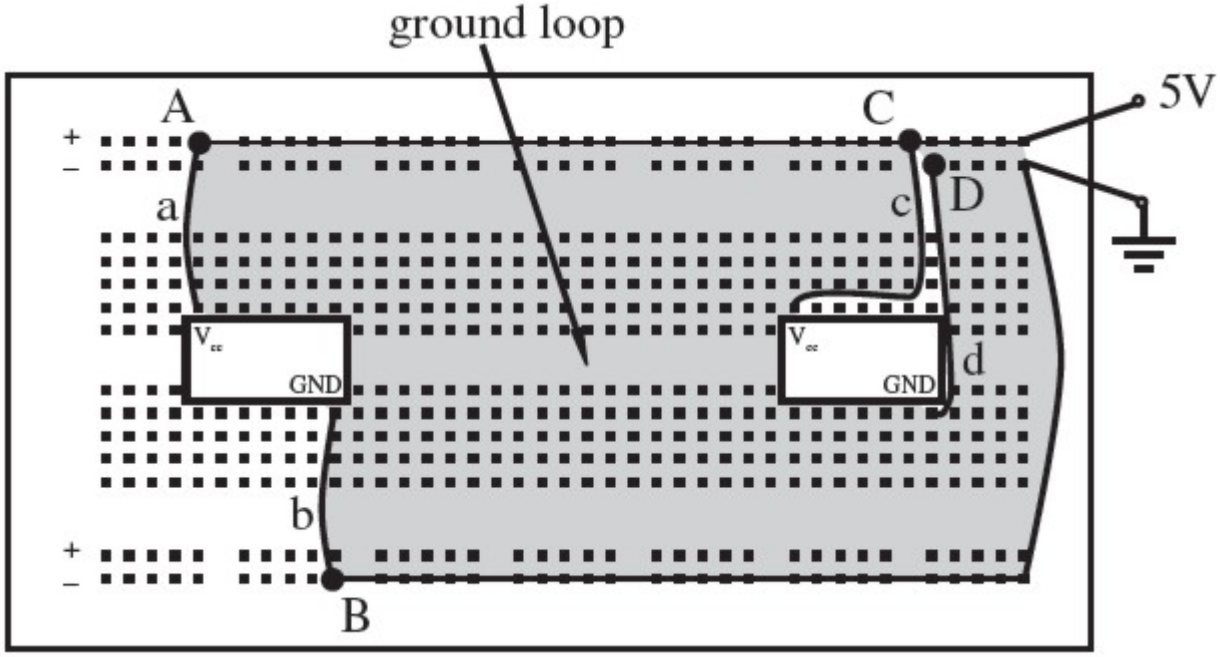


Figure 2.50 Ground loop (p. 63)

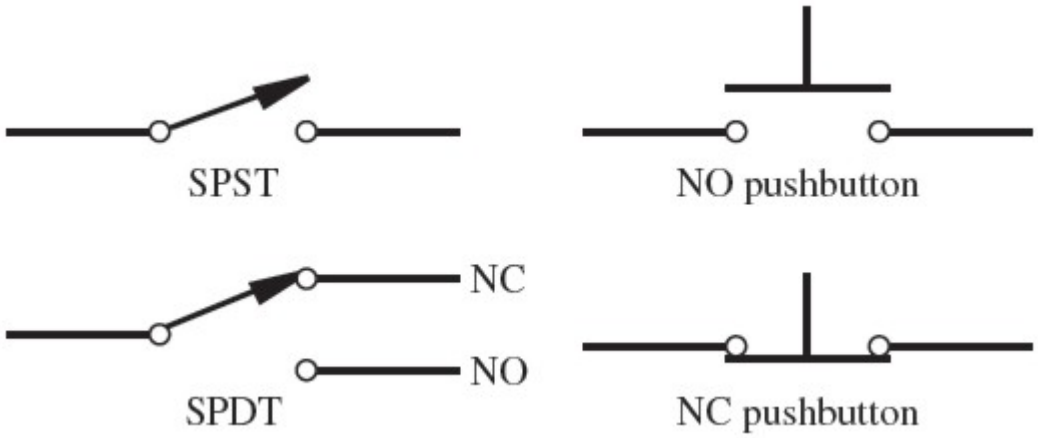


Figure 9.2 Switches (p. 412)

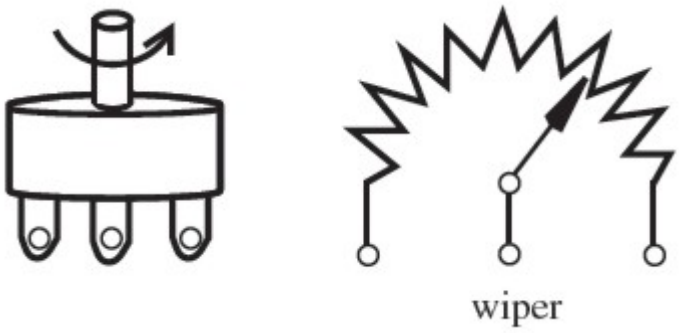


Figure 9.4 Potentiometer (p. 413)

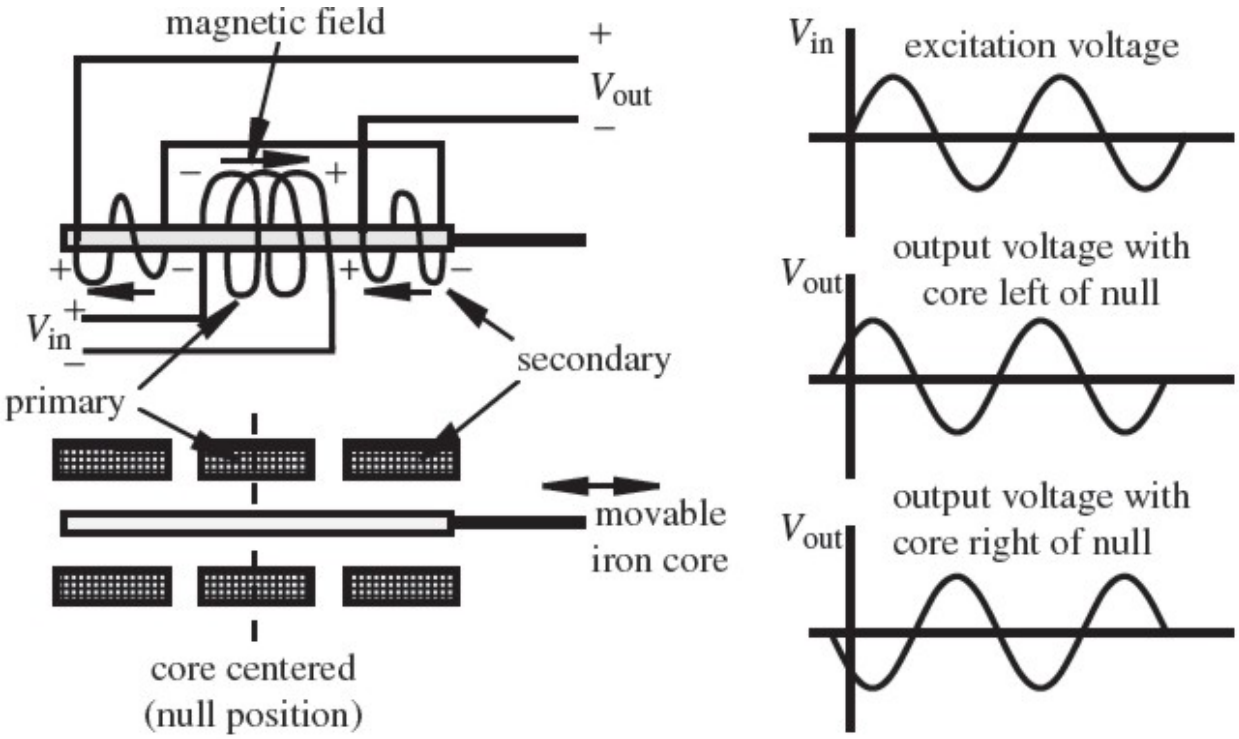


Figure 9.6 Linear variable differential transformer (p. 415)

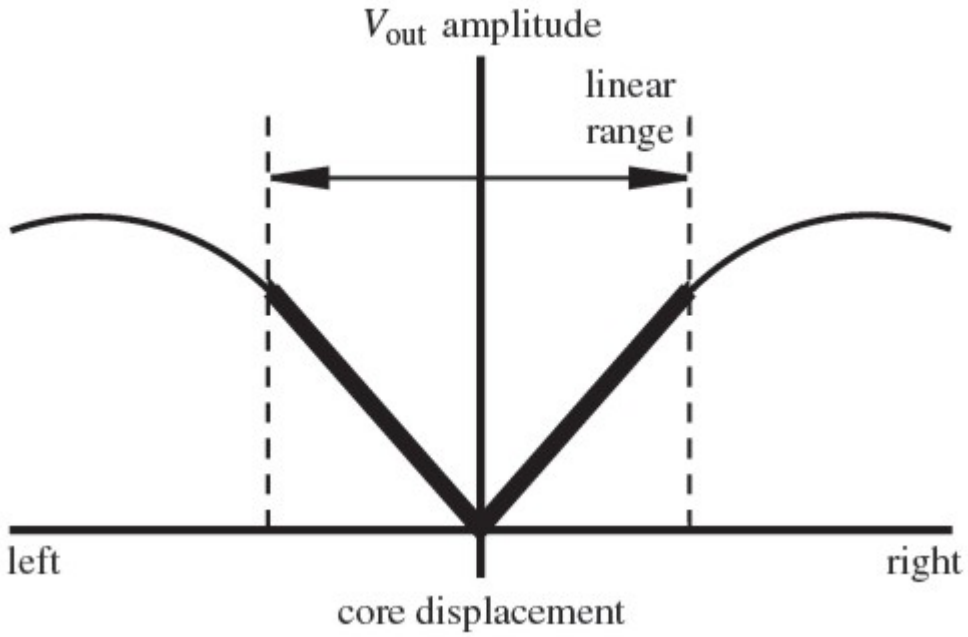


Figure 9.8 LVDT linear range (p. 415)

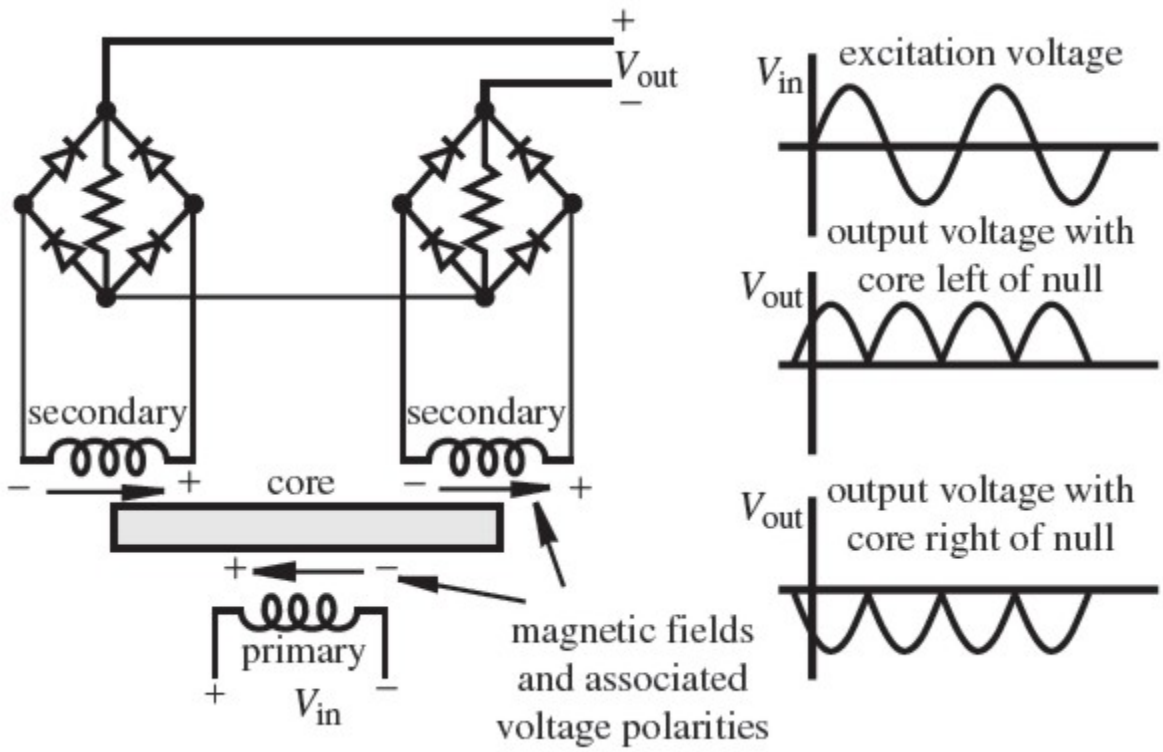


Figure 9.9 LVDT demodulation (p. 415)

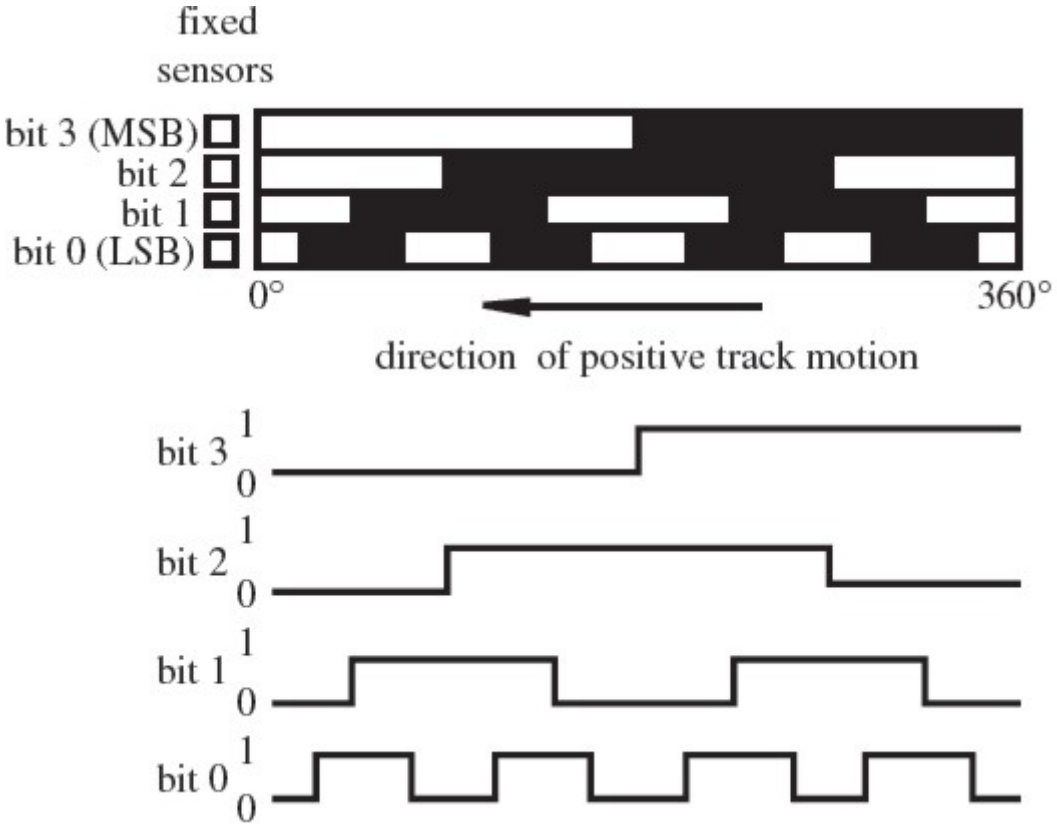
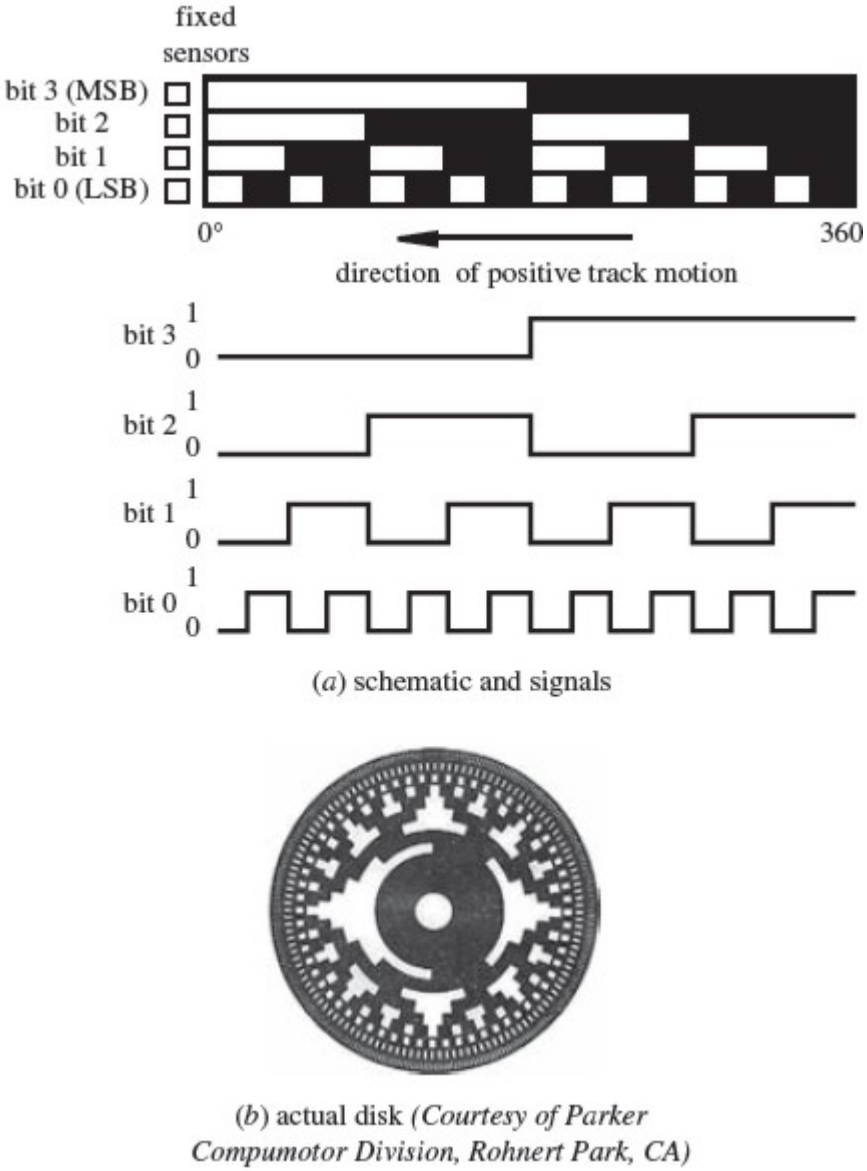


Figure 9.11 4-bit gray code absolute encoder disk track patterns (p. 419)



(*a*) schematic and signals

(*b*) actual disk *(Courtesy of Parker Compumotor Division, Rohnert Park, CA)*

Figure 9.12 4-bit natural binary absolute encoder disk track patterns (p. 419)

Decimal Code	Rotation Range (°)	Natural binary code ($B_3B_2B_1B_0$)	Gray code ($G_3G_2G_1G_0$)
0	0–22.5	0000	0000
1	22.5–45	0001	0001
2	45–67.5	0010	0011
3	67.5–90	0011	0010
4	90–112.5	0100	0110
5	112.5–135	0101	0111
6	135–157.5	0110	0101
7	157.5–180	0111	0100
8	180–202.5	1000	1100
9	202.5–225	1001	1101
10	225–247.5	1010	1111
11	24 7.5–270	1011	1110
12	270–292.5	1100	1010
13	292.5–315	1101	1011
14	315–337.5	1110	1001
15	337.5–360	1111	1000

Table 9.1 4-bit gray and natural binary codes (p. 420)

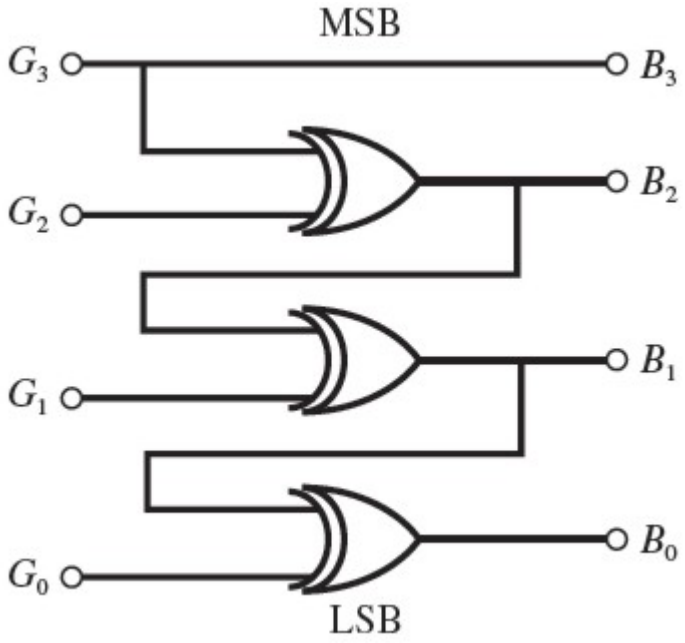
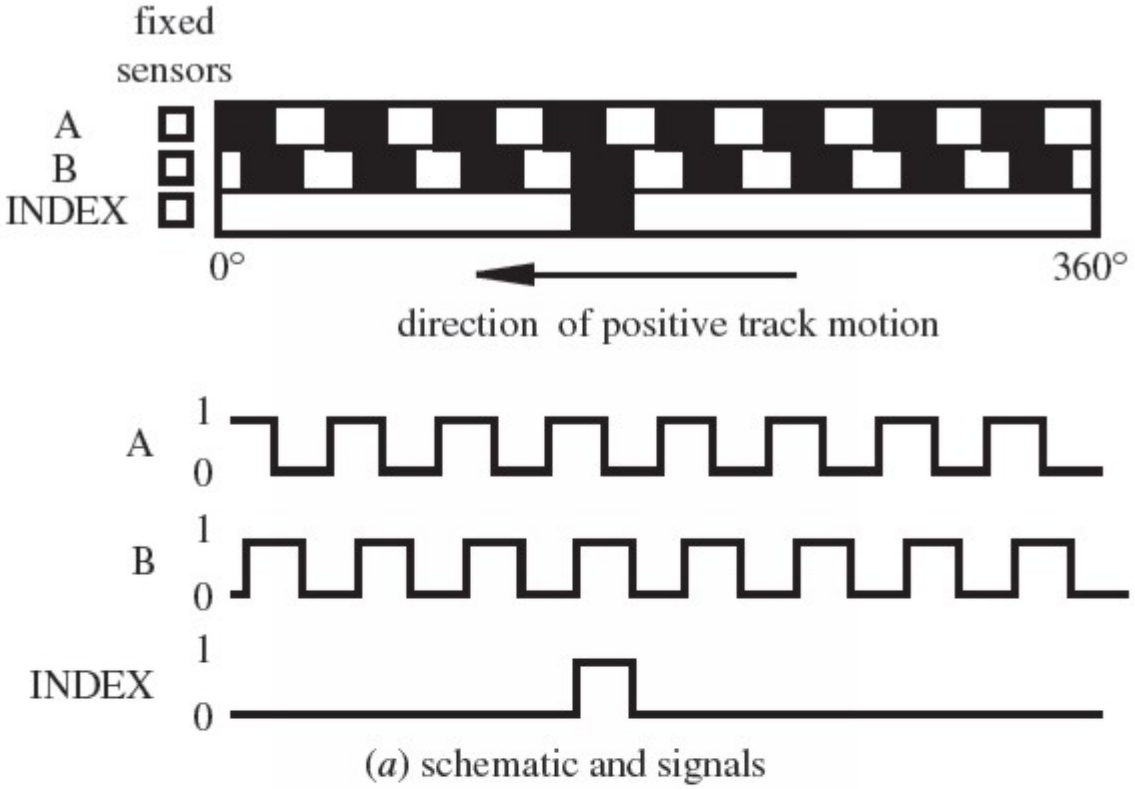


Figure 9.13 Gray-code-to-binary-code conversion (p. 420)



(*a*) schematic and signals

(*b*) actual disk *(Courtesy of Parker Compumotor Division, Rohnert Park, CA)*

Figure 9.14 Incremental encoder disk track patterns (p. 421)

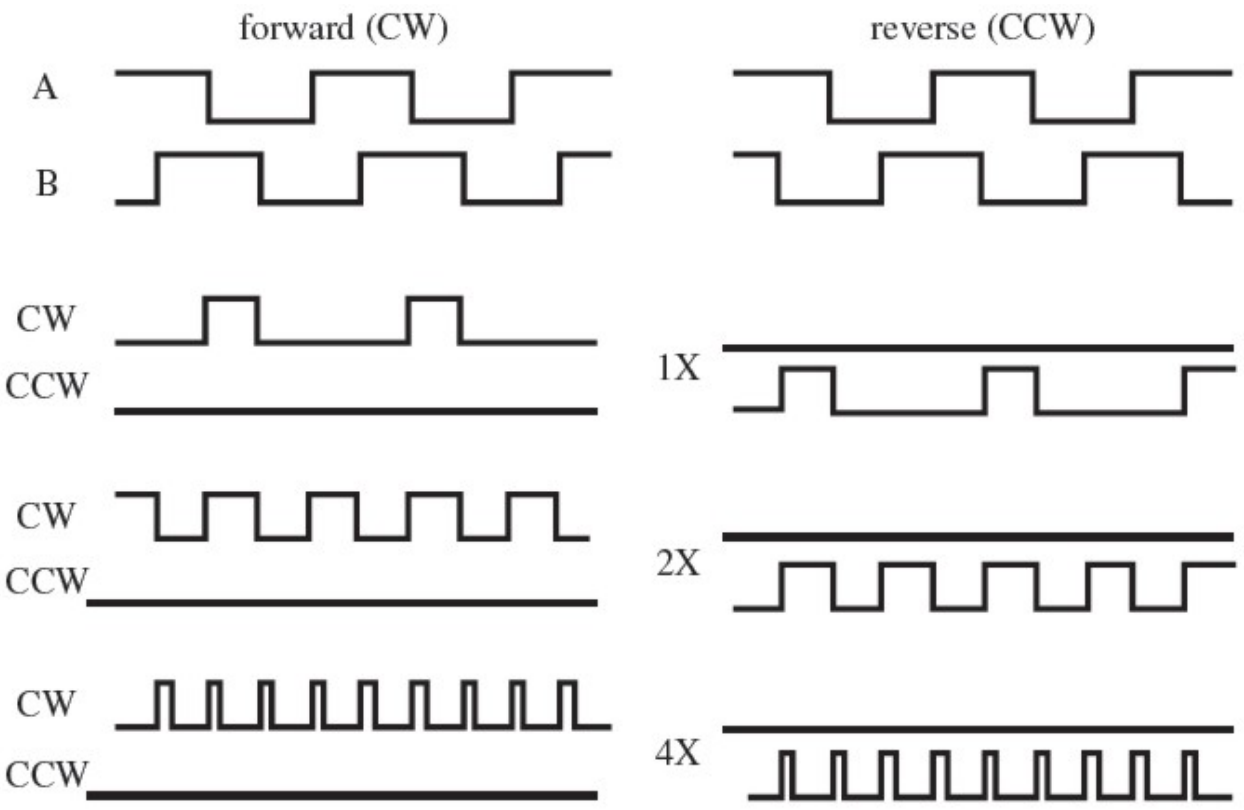


Figure 9.15 Quadrature direction sensing and resolution enhancement (p. 422)

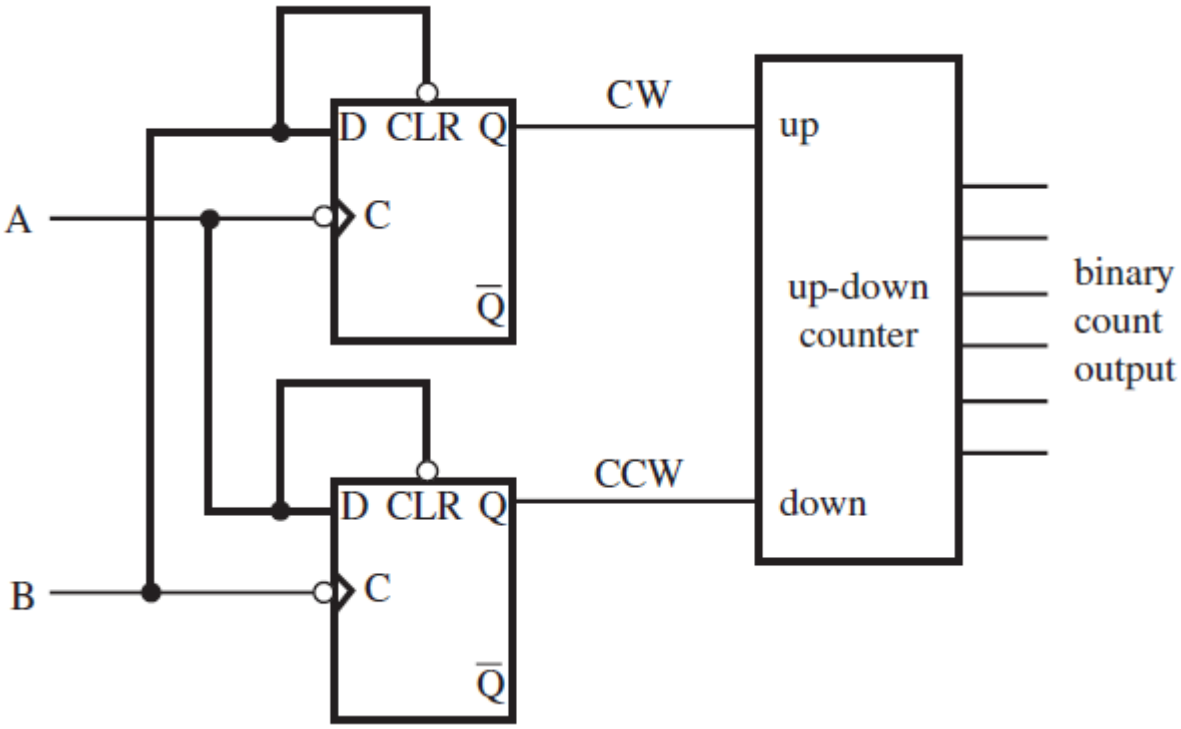


Figure 9.16 1X quadrature decoder circuit (p. 423)

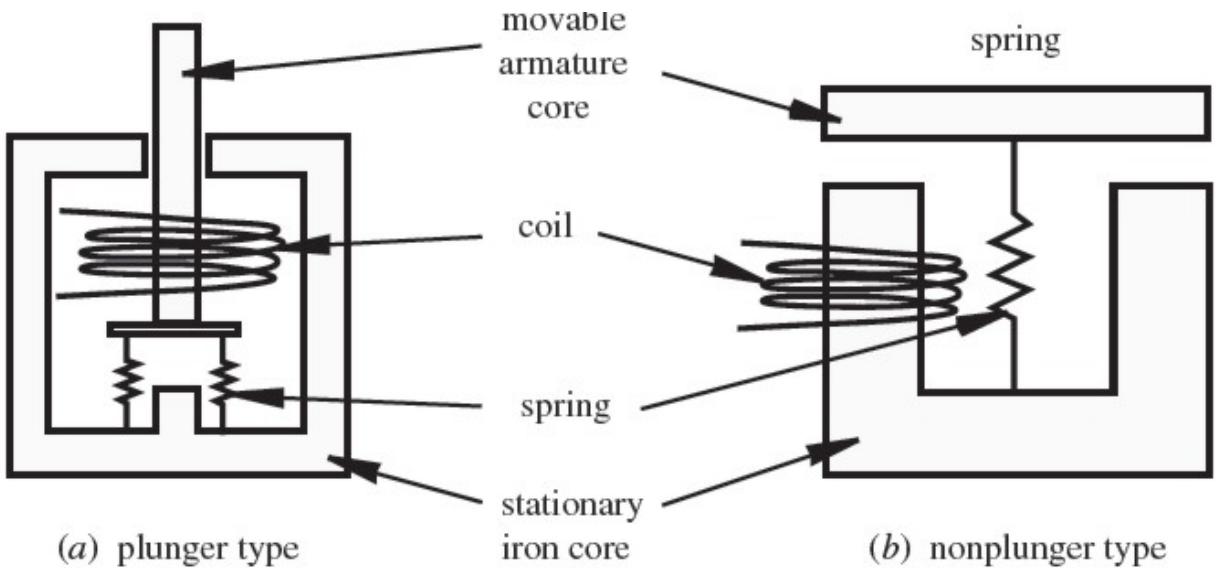


Figure 10.2 Solenoids (p. 468)

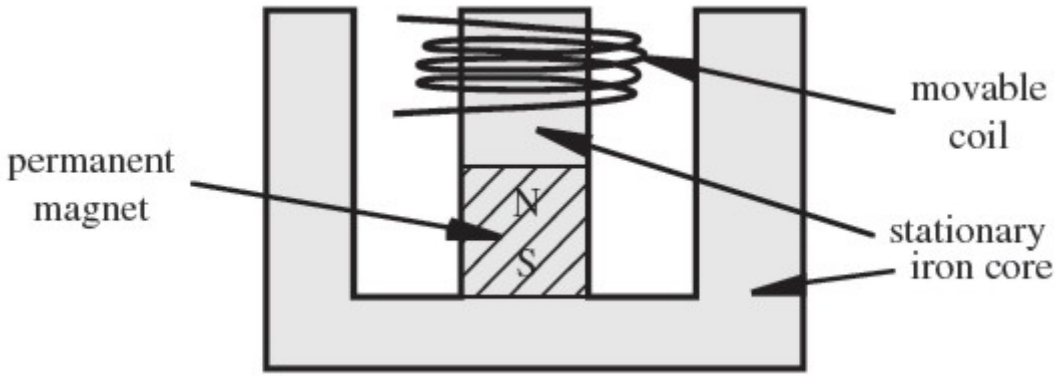


Figure 10.3 Voice coil (p. 468)

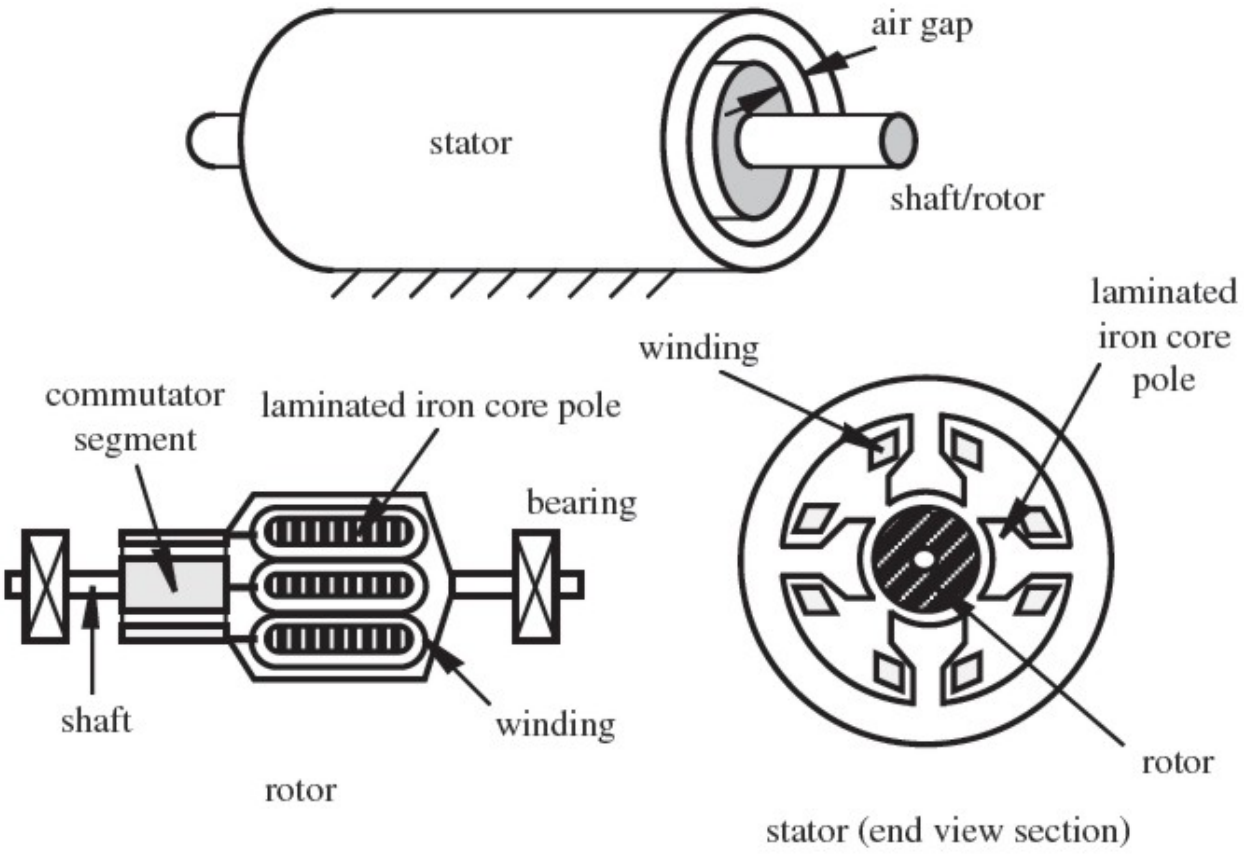


Figure 10.6 Motor construction and terminology (p. 470)

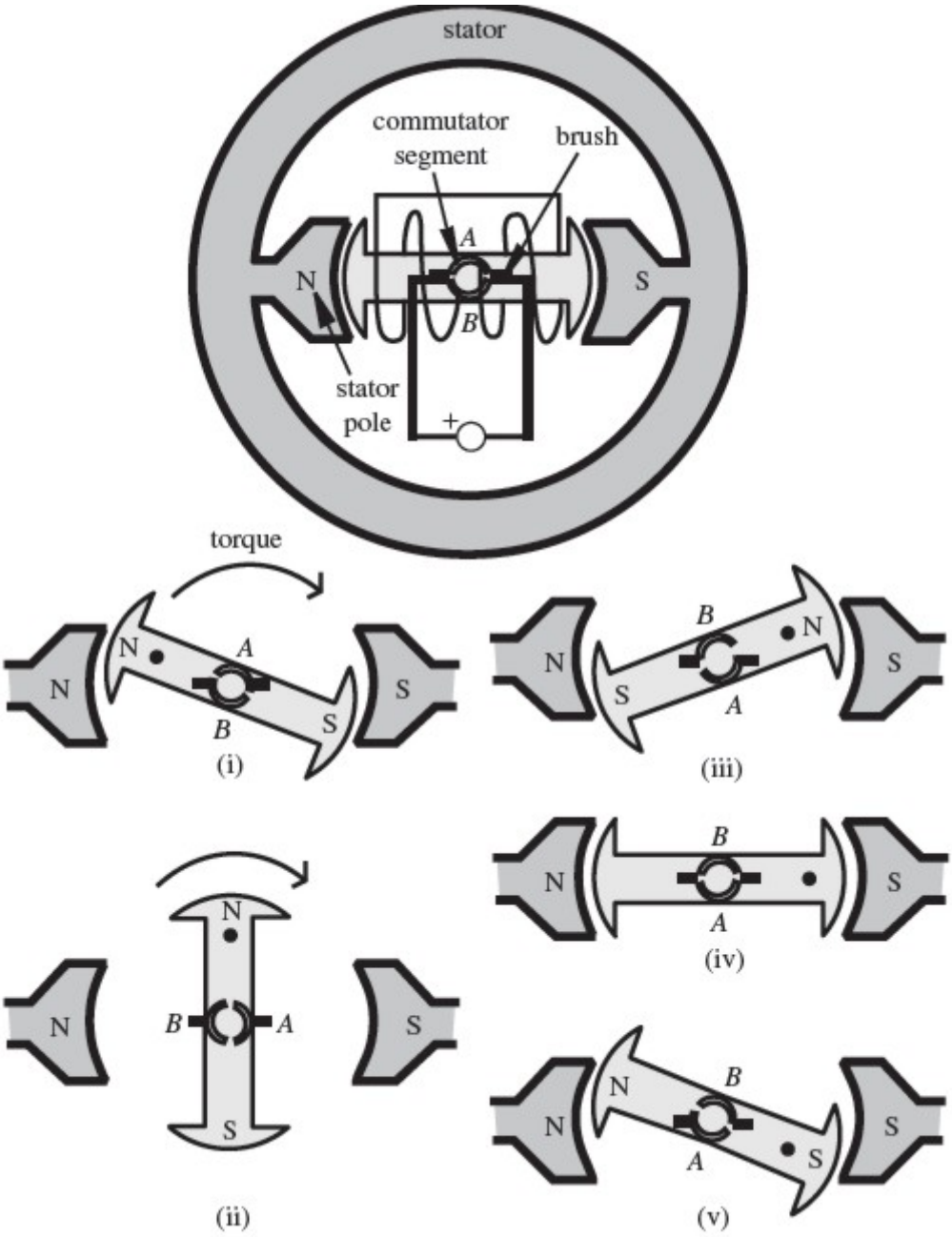


Figure 10.10 Electric motor field-field interaction (p. 474)

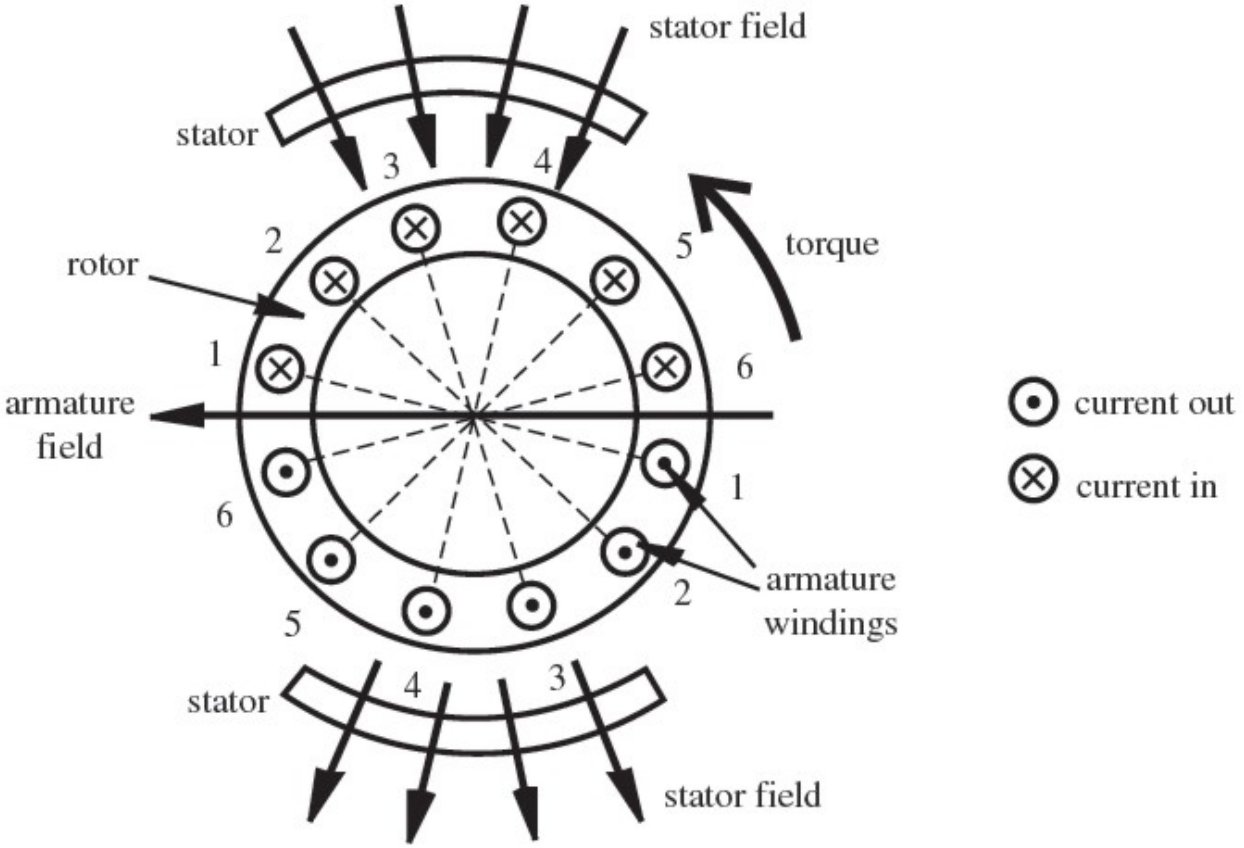


Figure 10.8 Electric motor field-current interaction (p. 472)

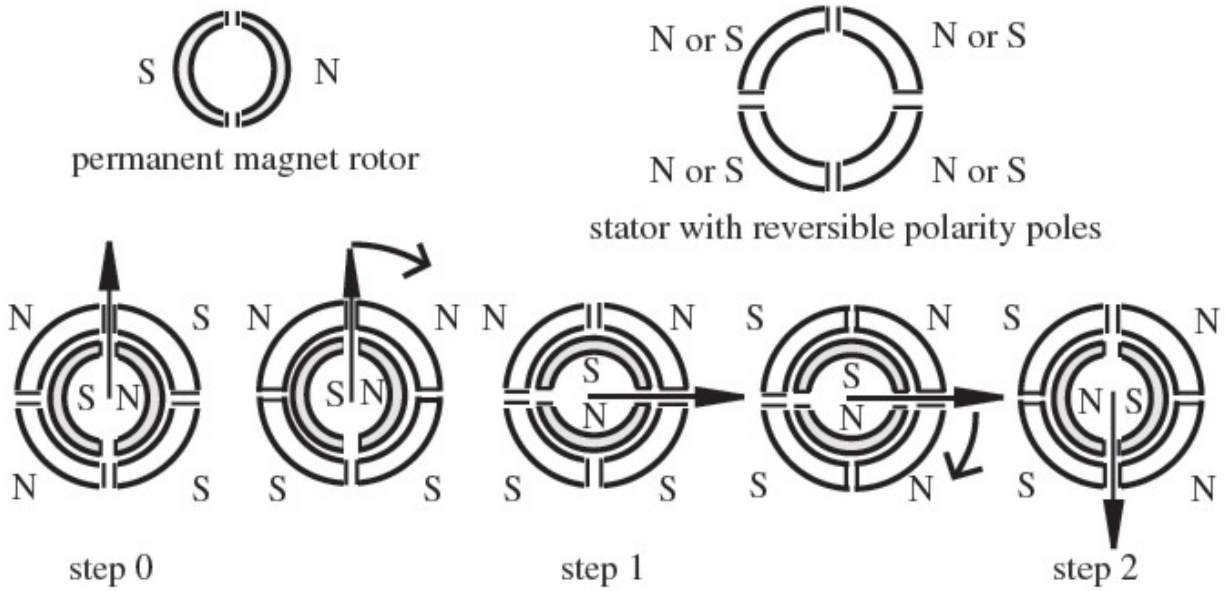


Figure 10.24 Stepper motor step sequence (p. 490)

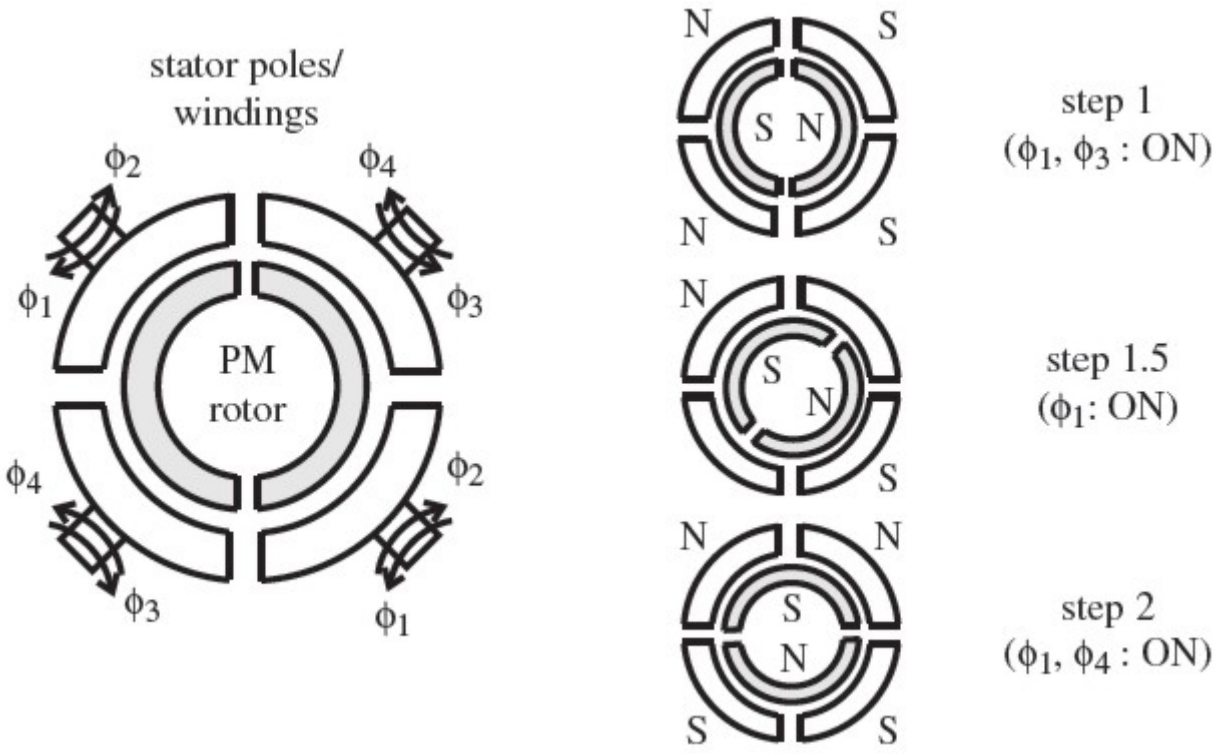


Figure 10.28 Example of a unipolar stepper motor (p. 492)

	Step	ϕ_1	ϕ_2	ϕ_3	ϕ_4
CW	1	ON	OFF	ON	OFF
↓	2	ON	OFF	OFF	ON
CCW	3	OFF	ON	OFF	ON
↑	4	OFF	ON	ON	OFF

Table 10.1 Unipolar full-step phase sequence (p. 493)

	Step	ϕ_1	ϕ_2	ϕ_3	ϕ_4
CW	1	ON	OFF	ON	OFF
↓	1.5	ON	OFF	OFF	OFF
	2	ON	OFF	OFF	ON
	2.5	OFF	OFF	OFF	ON
CCW	3	OFF	ON	OFF	ON
↑	3.5	OFF	ON	OFF	OFF
	4	OFF	ON	ON	OFF
	4.5	OFF	OFF	ON	OFF

Table 10.2 Unipolar half-step phase sequence (p. 493)

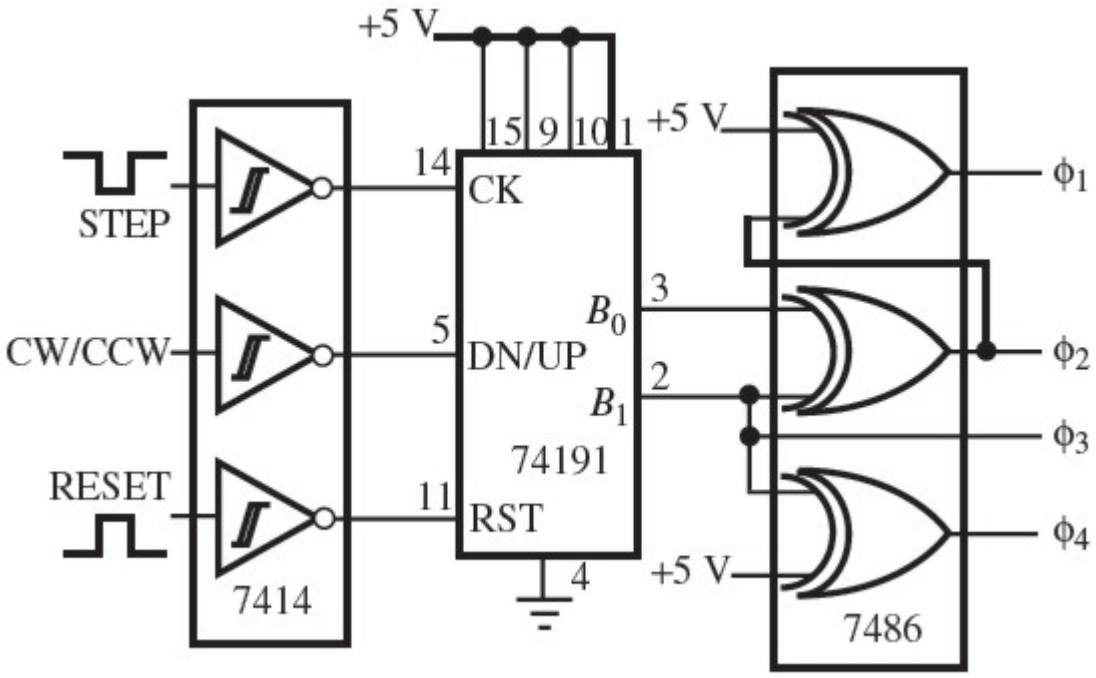
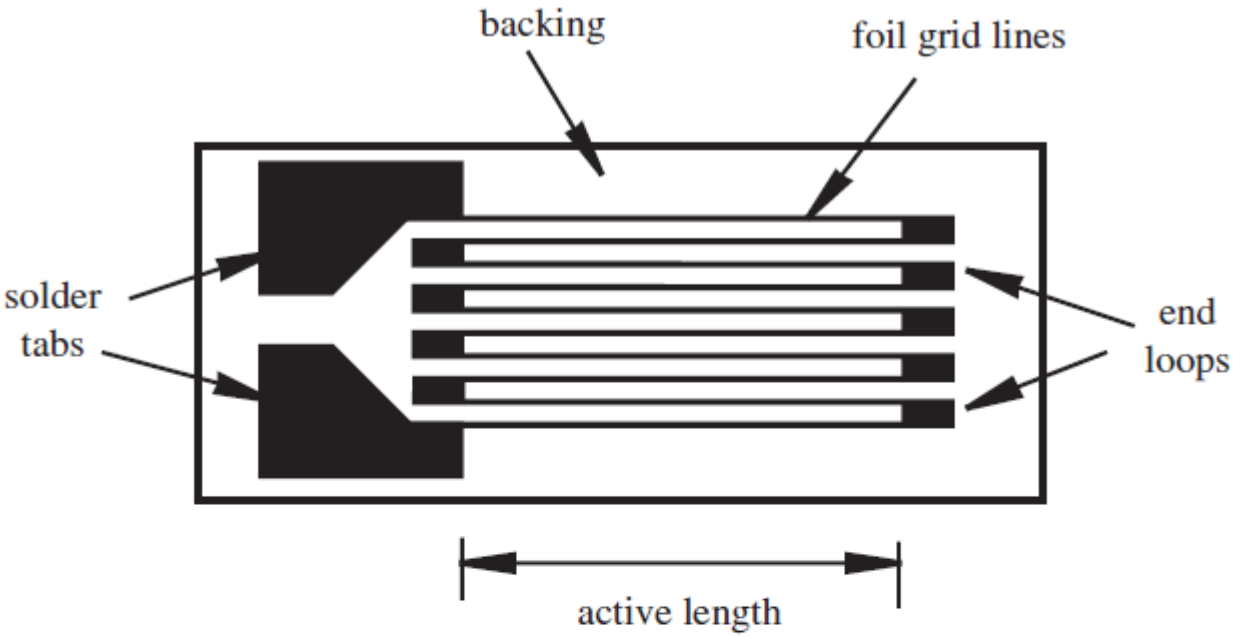
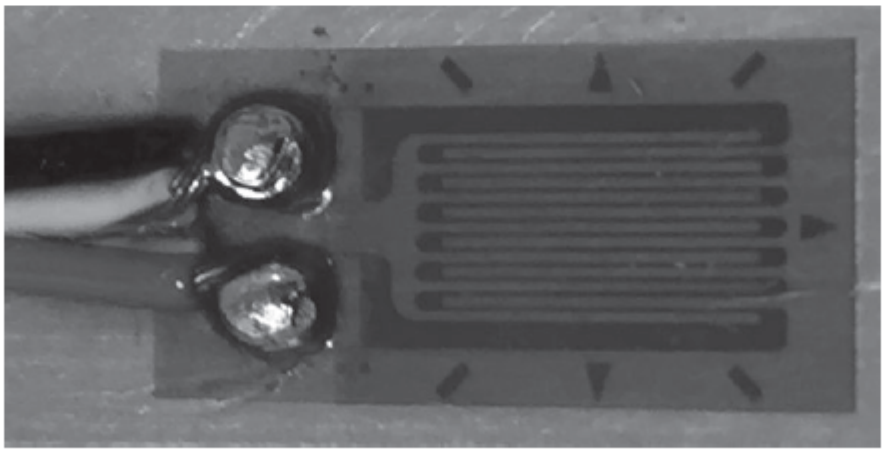


Figure 10.29 Unipolar stepper motor full-step drive circuit (p. 496)



(*a*) schematic



(*b*) actual *(Courtesy of Measurements Group Inc., Raleigh, NC)*

Figure 9.17 Metal foil strain gage construction (p. 426)

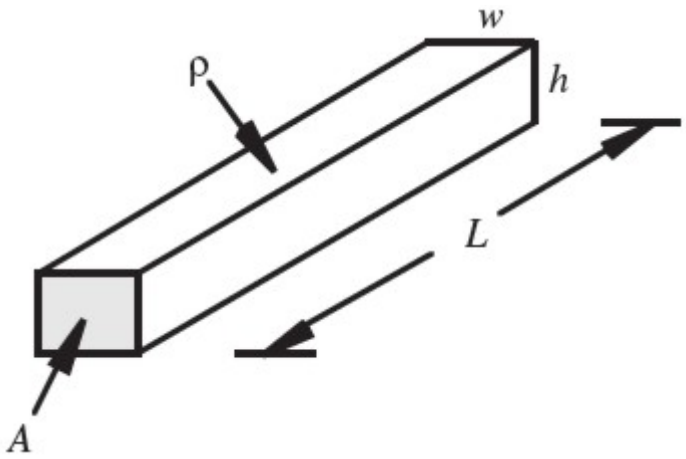


Figure 9.18 Rectangular conductor (p. 427)

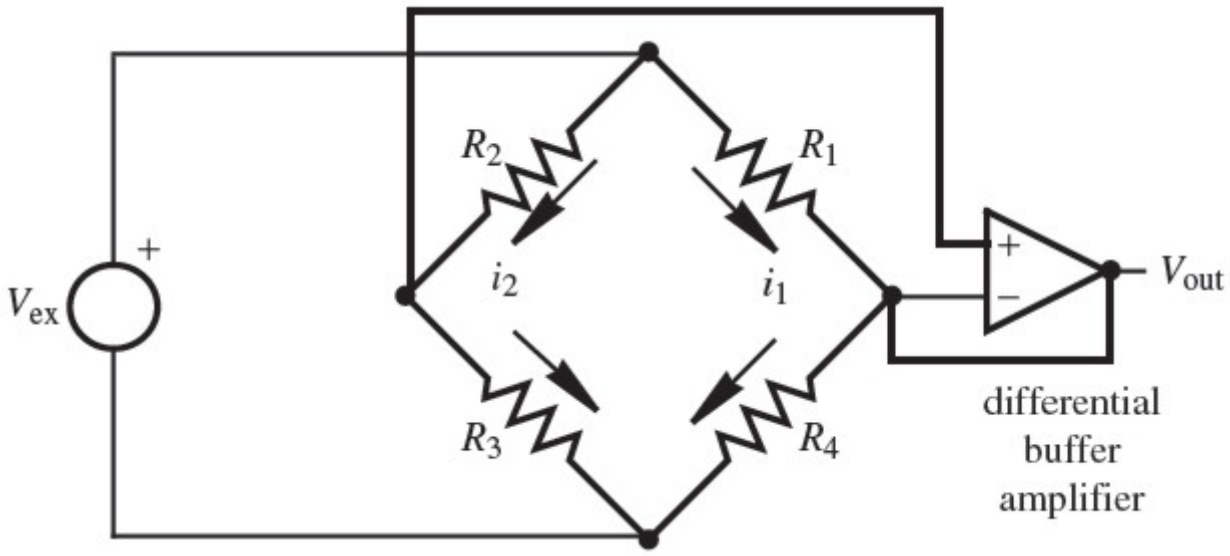
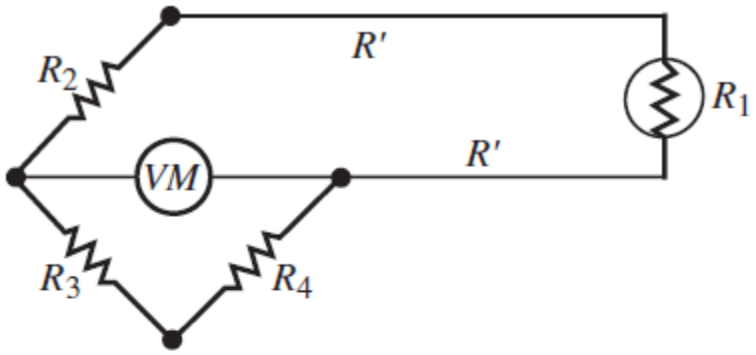
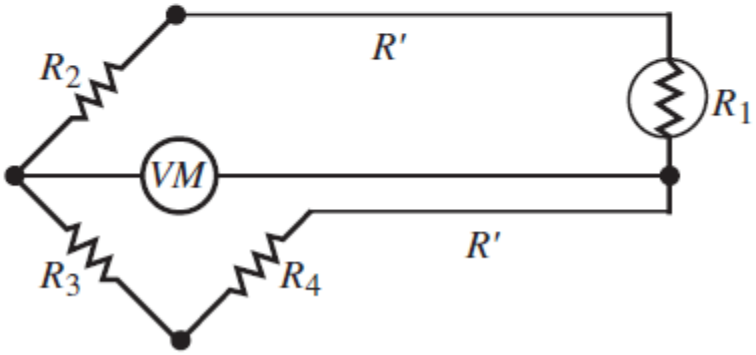


Figure 9.20 Dynamic unbalanced bridge circuit (p. 431)



(*a*) 2-wire connection



(*b*) 3-wire connection

Figure 9.21 Leadwire effects in 1/4 bridge circuits (p. 433)

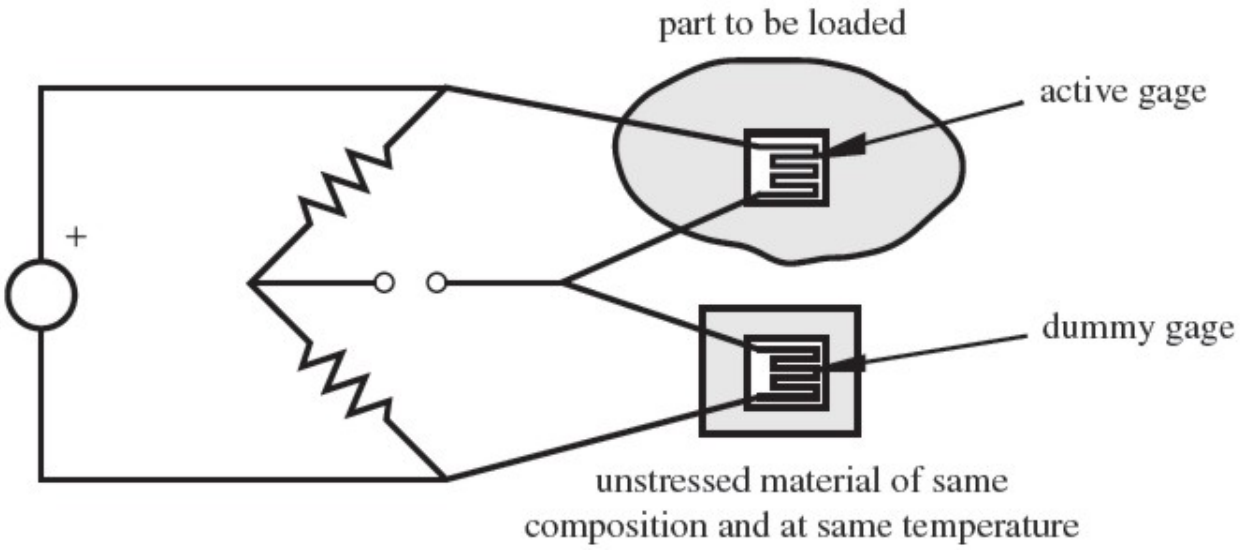


Figure 9.23 Temperature compensation with a dummy gage in a half bridge circuit (p. 433)

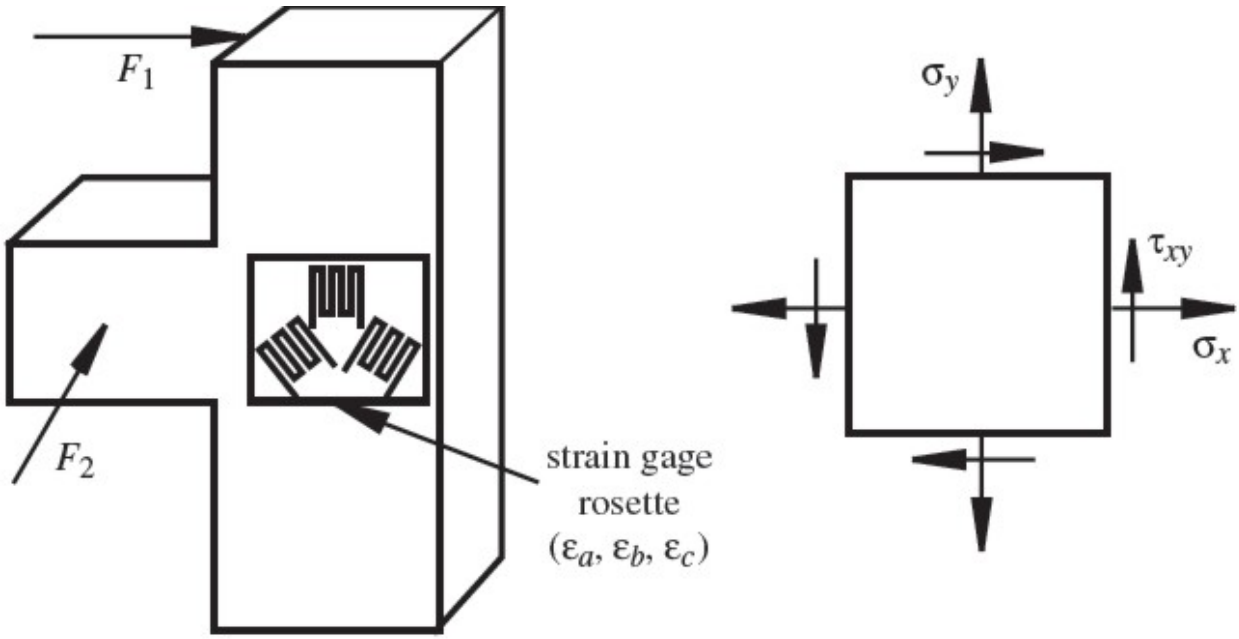


Figure 9.26 General state of planar stress on the surface of a component (p. 436)

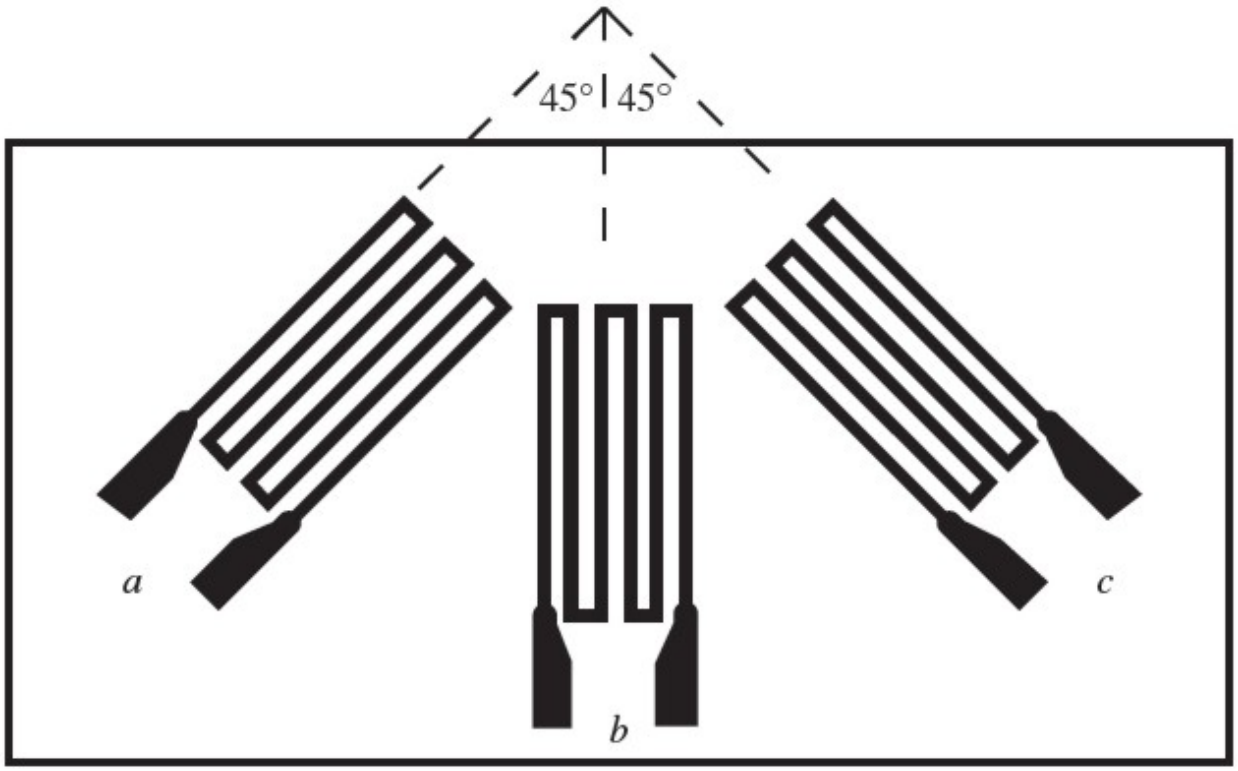


Figure 9.29 Rectangular strain gage rosette (p. 437)

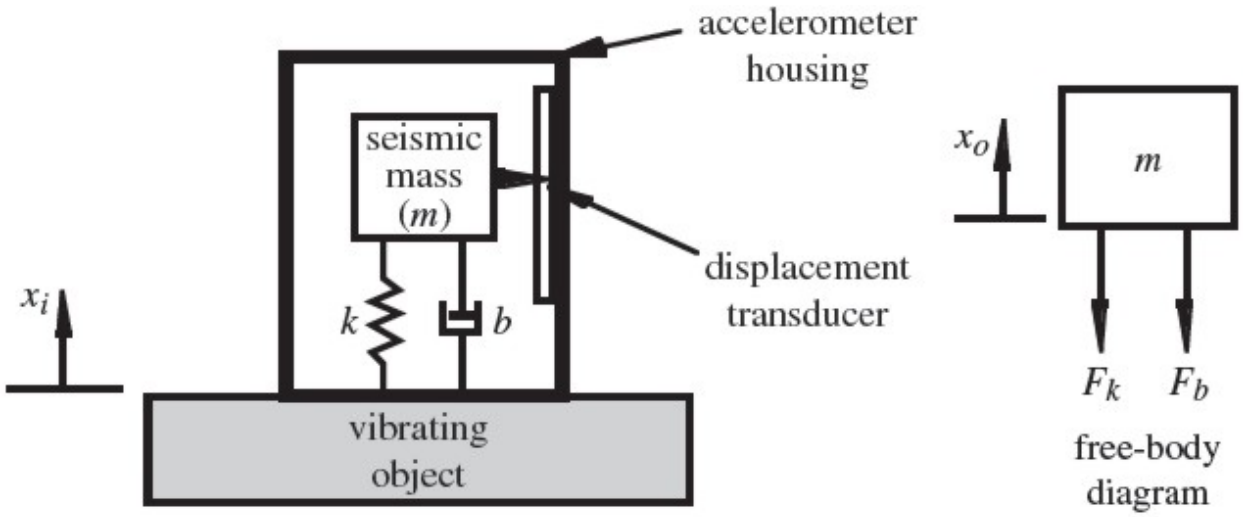


Figure 9.44 Accelerometer displacement references and free-body diagram (p. 451)

Accelerometer Frequency Response Analysis

$$x_i(t) = X_i \sin(\omega t)$$

$$x_r(t) = X_r \sin(\omega t + \phi)$$

$$\frac{X_r}{X_i} = \frac{(\omega/\omega_n)^2}{\left(\left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]^2 + 4\zeta^2\left(\frac{\omega}{\omega_n}\right)^2\right)^{1/2}} \tag{9.67}$$

$$\phi = -\tan^{-1}\left(\frac{2\zeta(\omega/\omega_n)}{1 - \left(\frac{\omega}{\omega_n}\right)^2}\right) \tag{9.68}$$

$$\ddot{x}_i(t) = -X_i\omega^2 \sin(\omega t) \tag{9.69}$$

$$H_a(\omega) = \frac{X_r\omega_n^2}{X_i\omega^2} = \frac{1}{\left(\left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]^2 + 4\zeta^2\left(\frac{\omega}{\omega_n}\right)^2\right)^{1/2}} \tag{9.71}$$

$$X_r = \left(\frac{1}{\omega_n^2}\right) H_a(\omega)(X_i\omega^2) \tag{9.72}$$

$$(X_i\omega^2) = (\omega_n^2)X_r \tag{9.74}$$

$$\ddot{x}_i(t) = \omega_n^2 x_r(t) \tag{9.75}$$

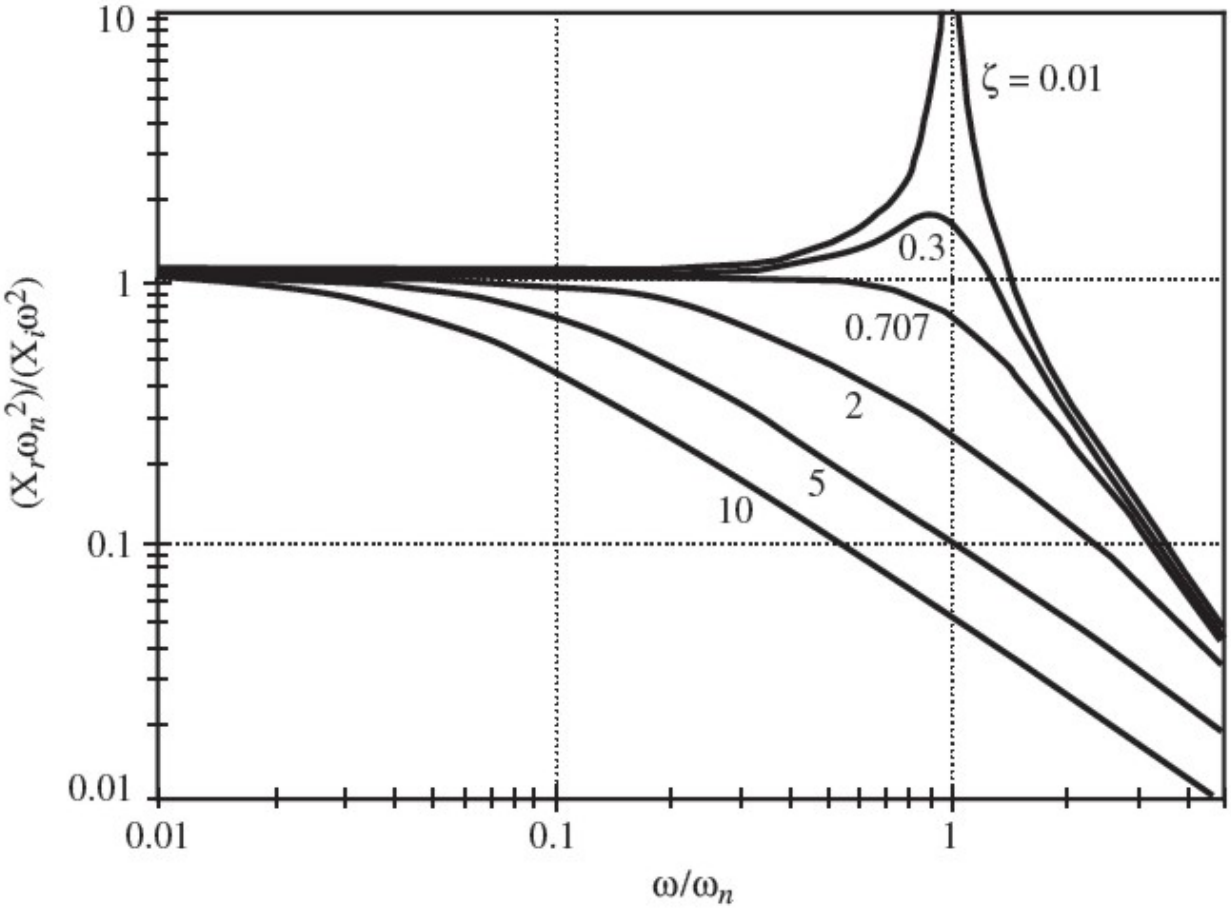


Figure 9.45 Ideal accelerometer amplitude response (p. 453)

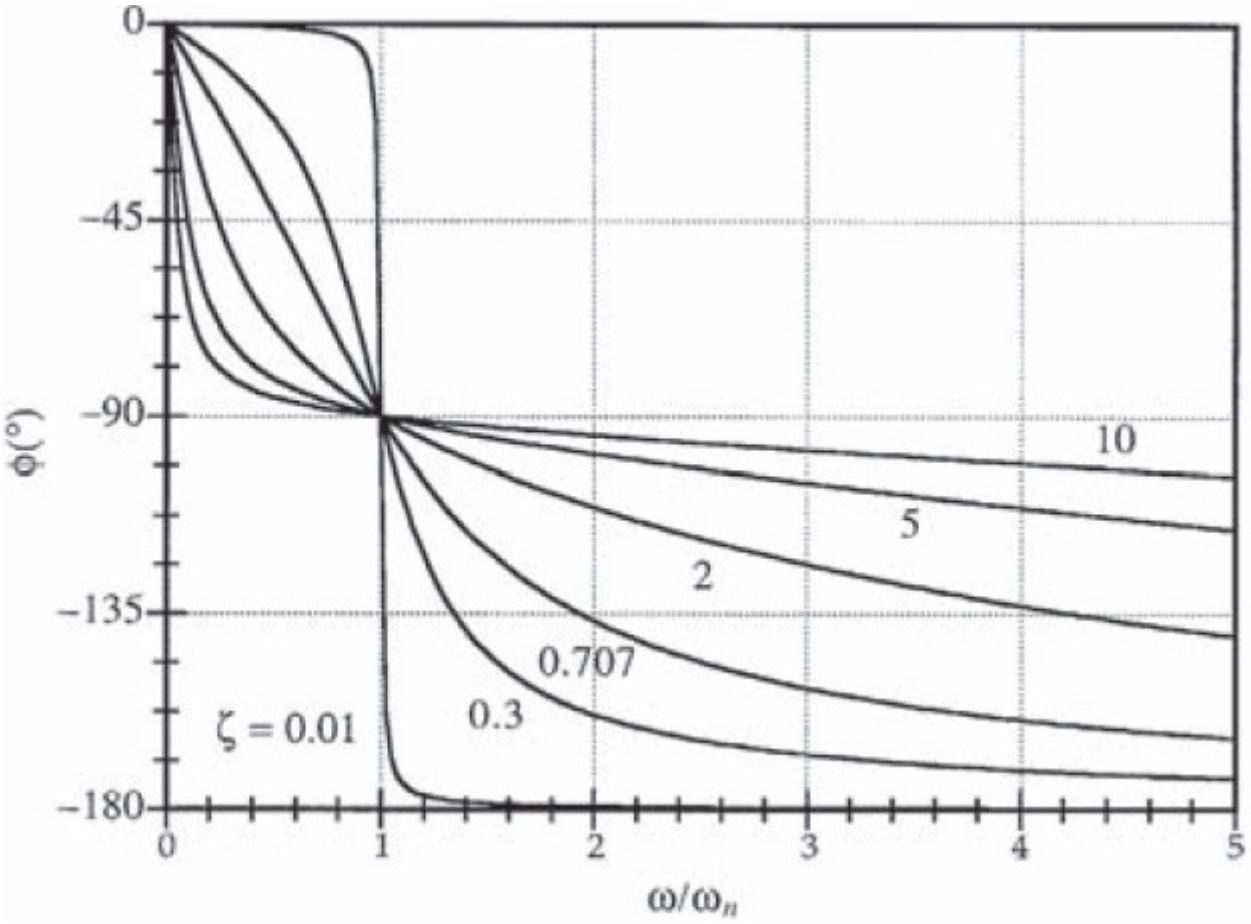
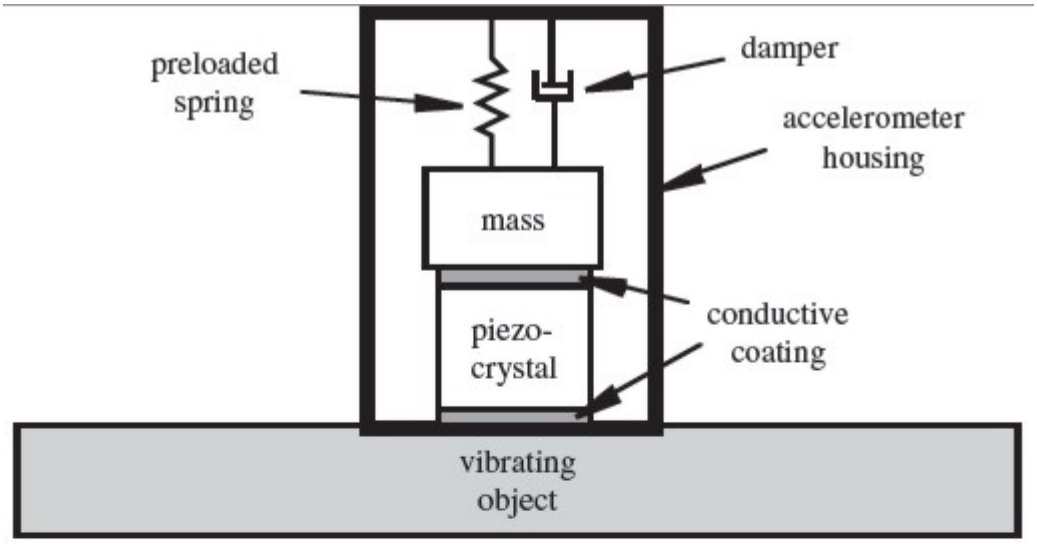


Figure 9.48 Ideal accelerometer phase response (p. 454)



(*a*) schematic illustration

Figure 9.48 Piezoelectric accelerometer construction (p. 456)

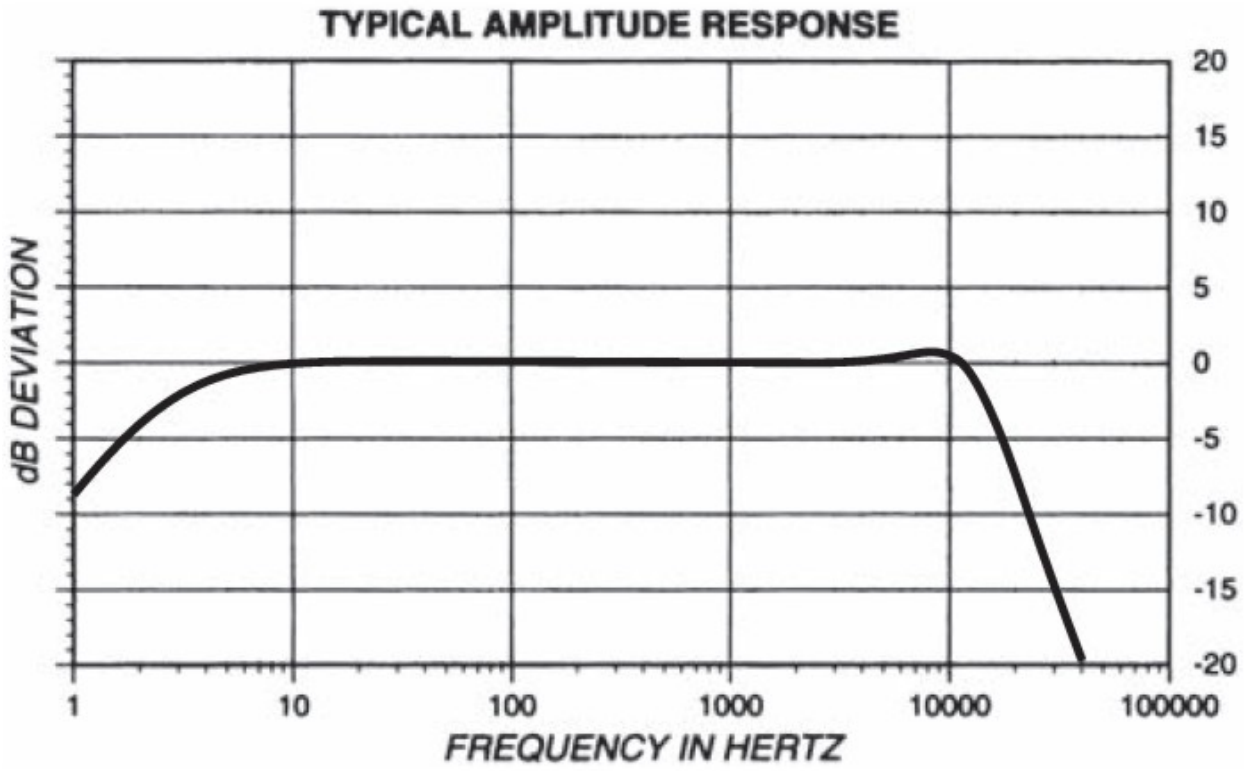


Figure 9.51 Piezoelectric accelerometer frequency response (p. 458)

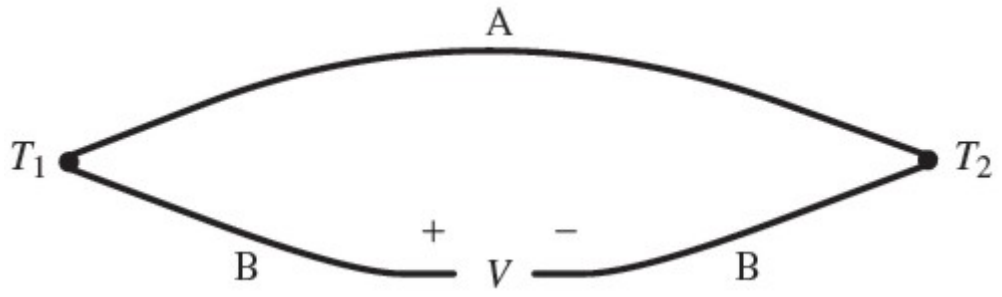


Figure 9.34 Thermocouple circuit (p. 443)

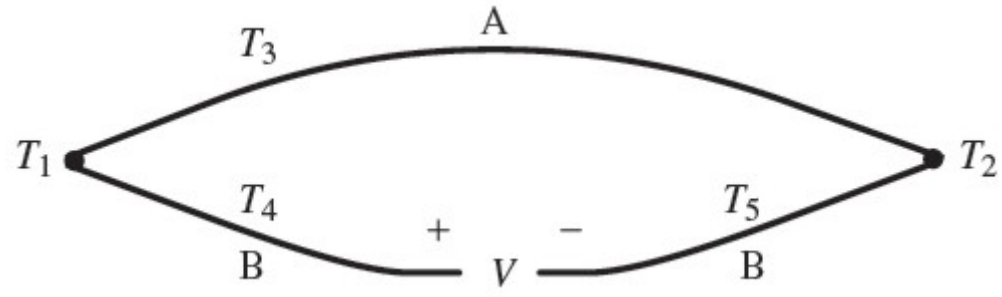


Figure 9.35 Law of leadwire temperatures (p. 444)

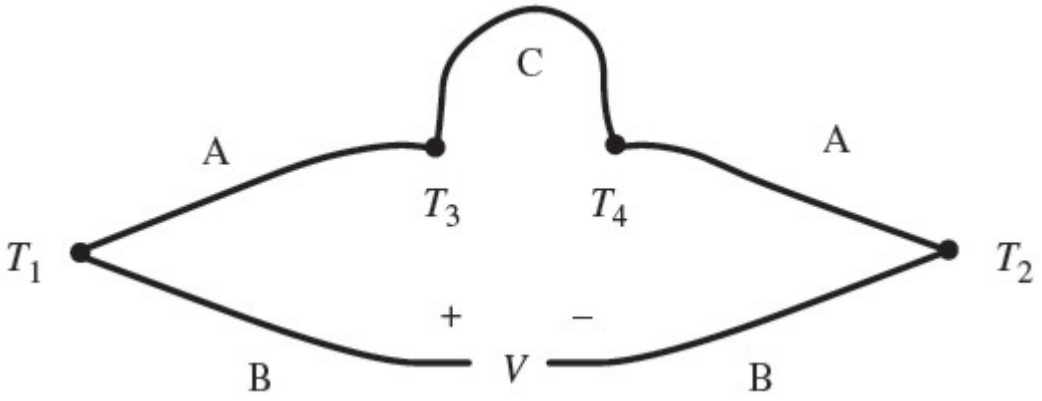


Figure 9.36 Law of intermediate leadwire metals (p. 444)

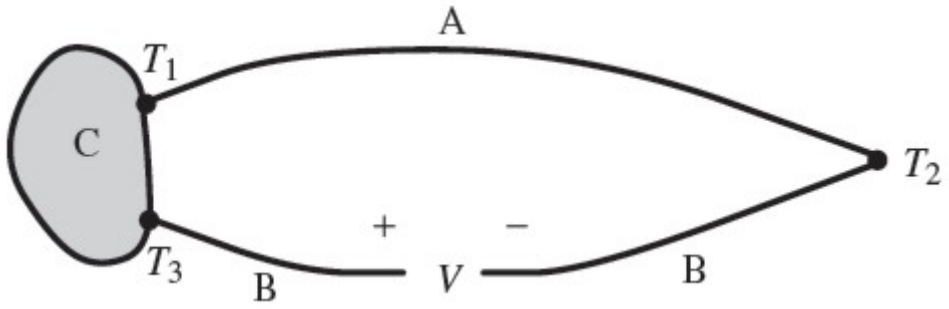


Figure 9.37 Law of intermediate junction metals (p. 445)

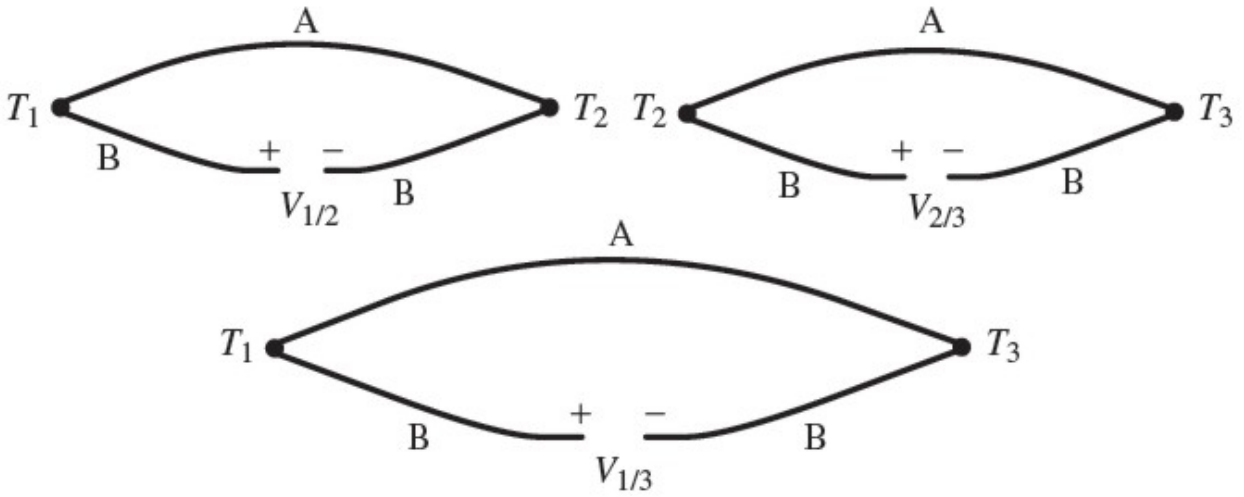


Figure 9.38 Law of intermediate temperatures (p. 445)

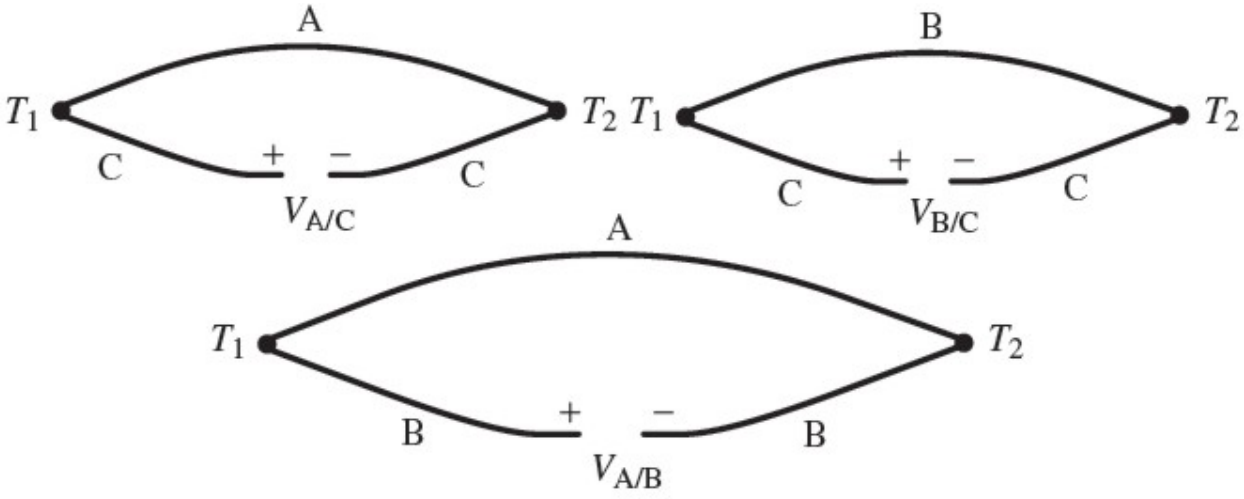


Figure 9.39 Law of intermediate metals (p. 446)

Comprehensive Case Study Truth Table

D	C	B	A	h	g	f	e	d	c	b	a
0	0	0	0	1	1	1	1	0	0	0	0
0	0	0	1	1	1	1	1	0	0	0	0
0	0	1	0	1	1	1	1	0	0	0	1
0	0	1	1	1	1	1	1	0	0	0	1
0	1	0	0	1	1	1	1	0	0	1	1
0	1	0	1	1	1	1	1	0	0	1	1
0	1	1	0	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	0	1	1	1
1	0	0	0	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1	1
1	0	1	0	1	1	0	0	1	1	1	1
1	0	1	1	1	1	0	0	1	1	1	1
1	1	0	0	1	0	0	0	1	1	1	1
1	1	0	1	1	0	0	0	1	1	1	1
1	1	1	0	0	0	0	0	1	1	1	1
1	1	1	1	0	0	0	0	1	1	1	1