

STABILITY, YIELD AND EFFICIENCY OF CdS/CdTe DEVICES

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Thin Film Partnership Program
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1. SUMMARY

Under Phase I of the Thin Film Partnership Program, we have made significant progress towards demonstrating consistent stability for thin film CdTe photovoltaics. We have repeatedly shown that devices with good stability can be produced if processed at optimal conditions. We have found that among the processing steps for fabrication of CdTe devices, the CdCl₂ treatment and back contact processing have the most effect on performance. Small changes in processes can lead to significant differences in device stability.

In an effort to improve the understanding of device performance, our devices have been characterized by a variety of analytical techniques in collaboration with many research groups. These studies demonstrated that there is doping at the back of CdTe due to the copper based back contact processing and that there is little change in this copper distribution with stress.

Significant improvements have been made to our laboratory's research capabilities. The uniformity and repeatability of our pilot scale device fabrication system has been enhanced. Device testing facilities have been improved with more accurate, faster current-voltage (J-V) measurement systems; the addition of capacitance measuring and cryostat hardware; and the construction of fixtures for exposing devices to indoor accelerated stress and outdoor conditions.

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2. INTRODUCTION

The aim of this research is to develop a detailed understanding of device stability, efficiency and process yield and the demonstration of consistent device stability for CdTe PV devices. Devices are processed with a unique, continuous, in-line pilot system. The pilot system enables unique processing conditions not available with batch processing and allows the fabrication of a large number of devices.

2.1. Pilot System

The pilot scale system is a continuous, all in-line system where all device fabrication steps are performed in one vacuum boundary. These processing steps include glass heating, CdS and CdTe deposition, CdCl₂ heat treatment, back contact formation and back contact heat-treatment. The system operates at 40mTorr N₂. The required base pressure for the system is only 10⁻⁴ Torr, allowing the use of low cost hardware. A residual gas analyzer (RGA) is used to monitor chamber gas composition. Process stations are nearly identical in design and construction. A schematic of the pilot scale is shown in Figure 1.

An automated conveyor belt extends from air, through all the processing stations in vacuum and then back to air. The cycle time of each process station is 2 minutes, thus one substrate emerges from the system every 2 minutes. Currently the substrate size is 3.6 x 3.1 inches. The process modules are scaleable for processing larger substrates.

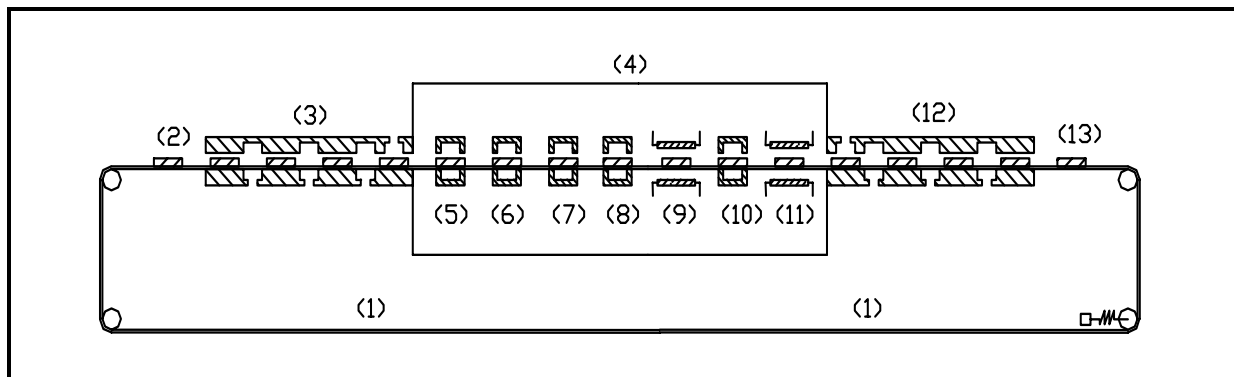


Figure 1: Schematic of the pilot system for CdTe PV fabrication, (1) belt conveyor, (2) glass substrate, (3) Air to vacuum to air (AVA) seal, (4) vacuum chamber, (5) heating module, (6) CdS deposition, (7) CdTe deposition, (8) CdCl₂ deposition and heat treatment, (9) CdCl₂ annealing and stripping, (10) back contact formation, (11) contact annealing, (12) AVA seal, (13) completed cell

2.2. Initial Device Performance

Devices have consistently been fabricated with 10.5 to 12.5% conversion efficiency with an NREL verified 12.44% with 71% fill factor. The highest efficiency measured on the devices produced with the pilot system is 13.0%. The device structure is glass/SnO_x:F/CdS/CdTe/carbon/nickel. The substrates are soda lime glass with the tin oxide coating from Pilkington (TEC 15); the tin oxide is unmodified. These devices had no anti-reflection coating. Back contact is formed in vacuum through the vapor deposition of a copper compound followed by annealing. Metallization (carbon and nickel) is performed by low cost spray processing outside of vacuum.

3. IMPROVEMENTS TO EXPERIMENTAL INFRASTRUCTURE

Under Phase I of this program, many of our research facilities including the pilot system have been upgraded. These improvements include:

- (a) Design and fabrication of fixtures for testing un-encapsulated cells outdoors,
- (b) Design and fabrication of improved indoor stress testers capable of testing a large number (over 250) of cells,
- (c) Upgrading the J-V hardware and installing C-V measurement and a cryostat systems,
- (d) Writing improved databases for tracking data,
- (e) Installation of a residual gas analyzer (RGA) on the pilot system, and
- (f) Improving the thermal uniformity of many process modules in the pilot system.

All these improvements are functioning well. A more detailed description of these activities can be found in the Appendices (Section 8.1.). These improvements have greatly facilitated our research capabilities; some of the salient research findings are discussed below.

4. RESEARCH RESULTS

4.1. Effect of Processing Parameters on Device Performance and Stability

The stability of approximately 500 devices, processed at different conditions, has been studied. It has been observed that small changes in processing conditions can have a significant effect on initial device performance and stability. The stability of devices processed at optimal condition is very promising (Section 4.2.1.).

4.1.1. CdCl₂ Processing Effects on Device Stability

The effectiveness of the CdCl₂ treatment has a very strong effect on initial efficiency and long-term device performance under stress. Figure 2 shows the effect of CdCl₂ treatment on initial device efficiency and long-term stability. A significant increase in series resistance is seen over time with non-optimum CdCl₂ treatment.

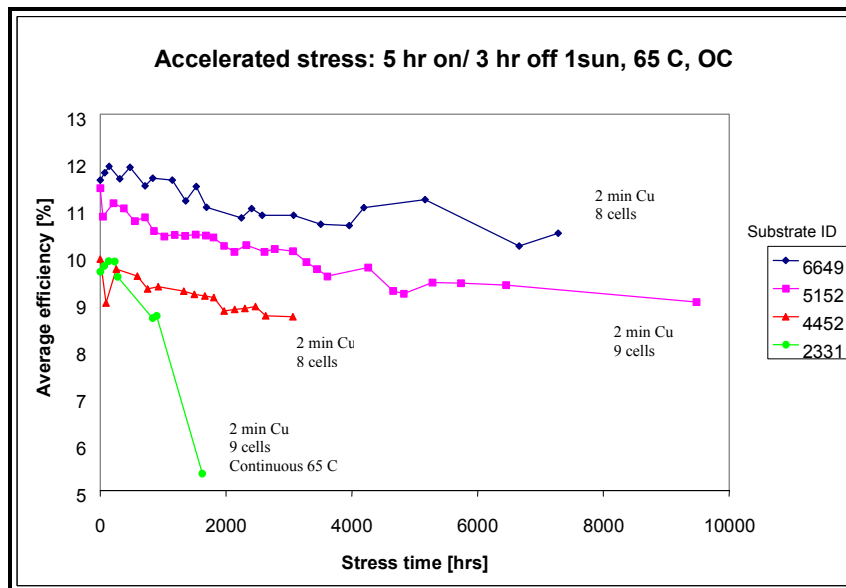


Figure 2: Effect of CdCl₂ treatment on stability, each line is an average of at least 8 cells all with the same back contact; stress condition: 1000 W/m² (5 hrs on out of 8 hr cycle) illumination, OC bias, 65 C temperature.

All the devices in Figure 2 have similar back contact but slightly different CdCl_2 treatments. The differences in the stability were due to changes in CdCl_2 flux during processing due to a subtle alteration of the source charge conditions and minor changes in processing temperatures. The better devices received higher CdCl_2 vapor flux. However, higher flux maybe beneficial only to a certain level. In our chloride treatment process, a CdCl_2 film is deposited, treatment takes place, and then the film is removed by precise control of the substrate temperature. Careful control of the substrate temperature to reduce substrate heating after removing the CdCl_2 film has been found to be critical to stability. It has been demonstrated elsewhere that a $\approx 5\%$ change in source temperature during CdCl_2 treatment can alter the device efficiency by nearly 50% [Mahathongdy 1999].

4.1.2. Back Contacting Processing Effects on Device Stability

Figure 3 shows the effect of back contact processing variation on stability. Non-optimum conditions lead to a significant increase in the series resistance and JV rollover is seen under light. As can be seen in Figure 3, the higher starting efficiencies do not always correlate to better stability. Furthermore, we have observed that there is an optimum amount of copper for producing stable devices.

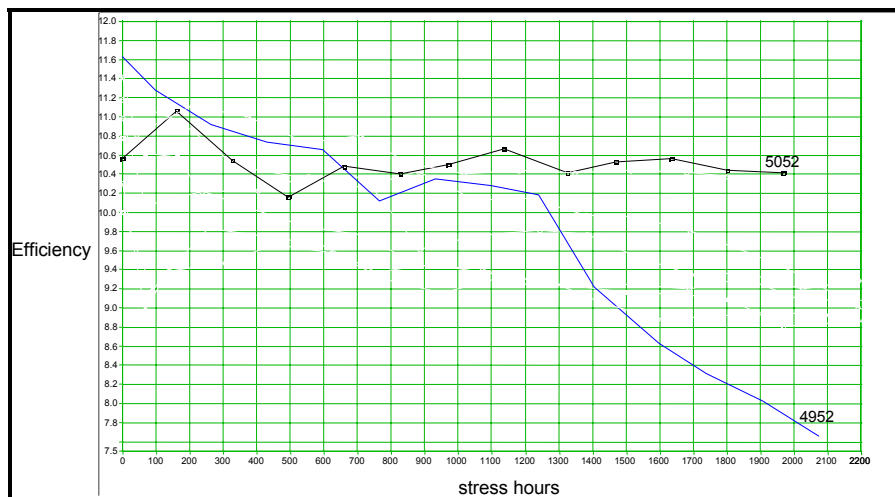


Figure 3: Effect of copper based back contact processing conditions on otherwise similarly prepared and stressed devices. Each line is average of 9 devices from same substrate, stress condition: 1000 W/m^2 (5 hrs on out of 8 hr cycle) illumination, OC bias, 65 C temperature.

4.1.3. Effect of Adsorbed Gasses On Device Stability

As demonstrated in Figure 2 (substrate 6649) when processed at optimal conditions, good efficiency and stability can be obtained with Cu based back contacts. However, very controlled processing is critical for obtaining these results. In one example with our devices, processing was halted after the chloride treatment (before back contact formation) and the device was allowed to see air briefly (a few minutes). Following this, our standard contact was grown in vacuum. The initial efficiency and the subsequent stability of these devices was significantly worse than the results without the exposure (other deposition parameters were held constant). Starting efficiency (average of 9 devices) with air exposure was 9.6%, compared to average starting efficiency of 11.2% for devices with no air exposure. Adsorbed gases and oxides modify the formation of the back contact.

4.1.4. Effect of Film Thickness on Device Performance

In addition to controlling the CdCl₂ treatment and the processing conditions for the back contact, it has been observed that the cadmium telluride thickness is a critical device parameter. Variations in CdTe thickness can alter the effectiveness of the CdCl₂ treatment due to changes in the film volume needed to be treated. Variations in CdTe thickness can also change the doping profile in the device. Table 1 shows how, for our process, decreasing the device thickness improves efficiency. However, too small a thickness can cause current losses and device shunting. The only change in processing for the substrates 8433 and 8633 was variation in the CdTe thickness.

Substrate ID: 8433		Substrate ID: 8633	
Number of Devices	3	Number of Devices	3
Device Thickness	25 kÅ	Device Thickness	17 kÅ
Standard Deviation	0.4	Standard Deviation	0.74
Mean Efficiency	10.9	Mean Efficiency	11.7

Table 1: Variation in average device efficiency with film thickness

4.2. Results of Ongoing Stability Testing

The behavior of nearly 500 devices subjected to stress conditions has been studied. Many tests are continuing. The stress conditions consist of 1 sun illumination, 65° C, OC with 5 hours of illumination out of an 8 hour cycle. Devices are also subjected to 77° C, 100° C and outdoor conditions. In addition to the effects of processing conditions on device stability other aspects have been observed during stability testing; these are discussed below.

4.2.1. Reproducibility of Stability

The stability performance of devices processed at the optimum conditions (to date) and subjected to indoor accelerated stress is shown in Figure 4. These two groups of devices were fabricated in two different process runs (runs 65 and 66). The fabrication process parameters including source temperatures, substrate temperatures, film thickness values, and lot numbers of source material were kept identical for both runs. Each group is from the same substrate and devices are 0.3 cm². Both groups have lost approximately 10% of their initial efficiency after approximately 7500 hours of stress. This demonstrates that stability can be reproduced if identical process conditions are maintained. A plot of dV/dJ vs. the inverse current density in light (not shown) has no curvature indicating no evidence of the formation of a blocking contact during stress.

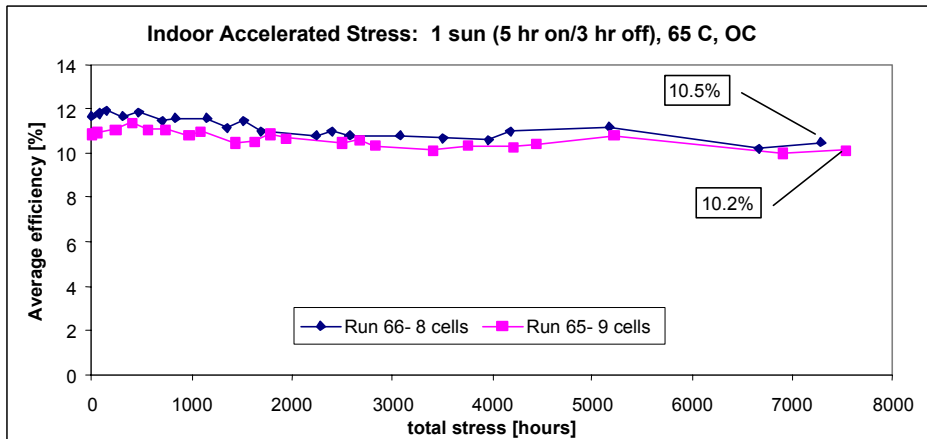


Figure 4: Stability of two groups of devices stressed indoors

4.2.2. Performance Under Outdoor Conditions

Two groups of three devices from these two fabrication runs (65 and 66) were also placed outdoors in the outdoor test fixture (See Section 8.1.1.). A third group of three devices from a different fabrication run (72) was also included. These devices were kept at open circuit bias. Figure 5 shows the average efficiency versus total time for these groups of cells. One set of three devices has been outside for almost a year. Within error of JV measurement (± 0.3 efficiency %) all three groups of these devices show no change in average efficiency over several months outdoors [Barth 2002].

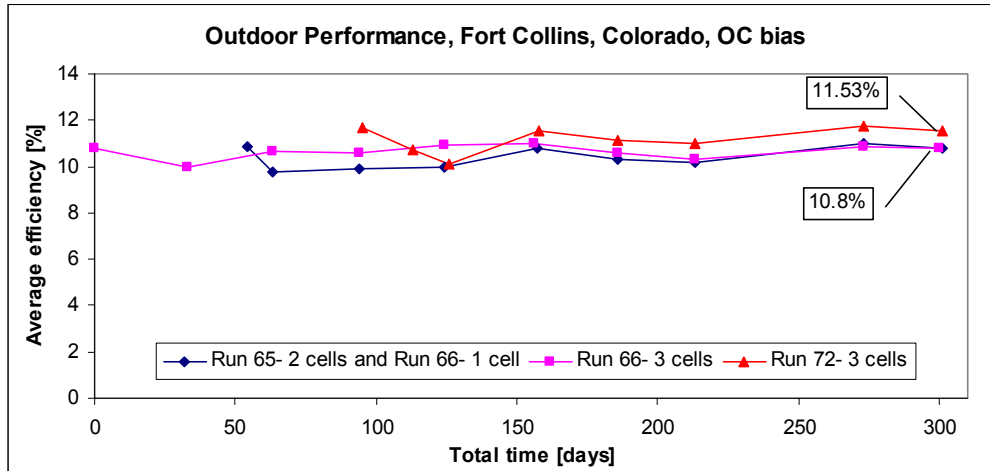


Figure 5: Stability of three groups of devices outdoors

4.2.3. Indoor Accelerated Stress and Outdoor testing, Correlation of Performance

In order to correlate indoor and outdoor stability, it is beneficial to classify the overall behavior into two types, Type I: small decrease in efficiency with time over long timeframes and Type II: short term rapid decrease in efficiency in both indoor stress and outdoor conditions. Type I behavior was shown in Figures 4 and 5 and is a result of optimal process conditions.

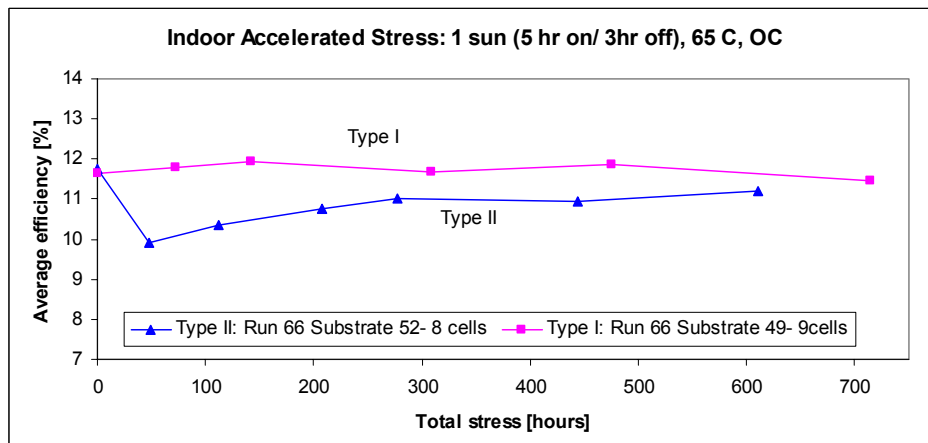


Figure 6: Comparison of Type I and Type II behavior for indoor accelerated stress testing

In Type II behavior, devices exhibit a decrease in efficiency in the early stages of both indoor accelerated and outdoor tests. The magnitude of the decrease is much higher outdoors

than indoors as shown in Figure 7. Type II device performance degradation is primarily due to a loss in J_{sc} for both indoors and outdoors. Tape peel tests demonstrated no loss of film or metallization adhesion in the stressed Type II devices. The loss of J_{sc} is due to a significant decrease in quantum efficiency at shorter wavelengths. Capacitance/voltage (C-V) analysis indicated that the doping in the CdTe has decreased significantly. In Type II behavior, the efficiency did recover in indoor stress testing, whereas such a recovery is not observed in outdoor conditions. It is important to note that the comparison of indoor to outdoor Type I and Type II behavior (Figures 6 and 7) show substrates from a single process run. These devices exhibiting Type II behavior had lower amounts of copper and lower substrate temperature during back contact formation. These variations were introduced intentionally during the processing.

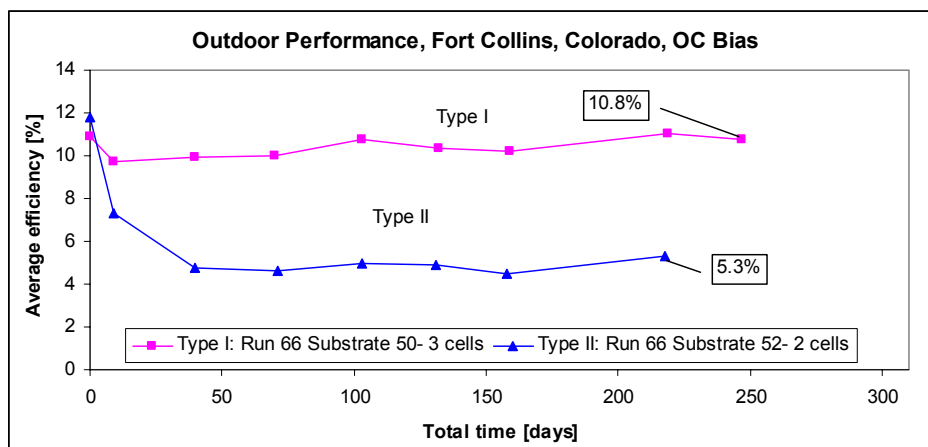


Figure 7: Type I and Type II behavior for outdoor exposure

For Type I behavior it maybe possible to obtain an empirical acceleration factor between indoor testing and outdoor performance. But at the present time, the change in efficiency outdoors is not large enough to determine such an empirical acceleration factor. The indoor tests are useful to identify process conditions that do not result in Type II behavior [Barth 2002].

4.2.4. Performance of Devices Subjected to 100° C Stress

Many devices processed at different conditions have also been subjected to 100° C, 1 sun and open circuit stress conditions. It was observed that processing devices at optimum conditions can lead to good stability at both 65° C and 100° C. Figure 8 is an overlay J-V plot which shows the stability achieved to date. Initial efficiency for this cell was 10.9% and the final efficiency after 964.5 hr of stress was 9.4%. Other cells from the same process run showed similar stability. Thinner cells had a higher incidence of shunting at 100° C than under 65° C or 77° C stress conditions. It was found that the Type II behavior was not observed during 100° C stress tests. Furthermore, the 100° C tests did not have the sensitivity to the differences in the CdCl₂ treatments and effects such as shown in Figure 2 were not seen. As a result, we have used 65 ° C, 1 sun illumination stress conditions to optimize the process. The optimum process parameters that will be obtained in this research program will produce devices which have good stability at both 65° C and 100° C, 1 sun illumination.

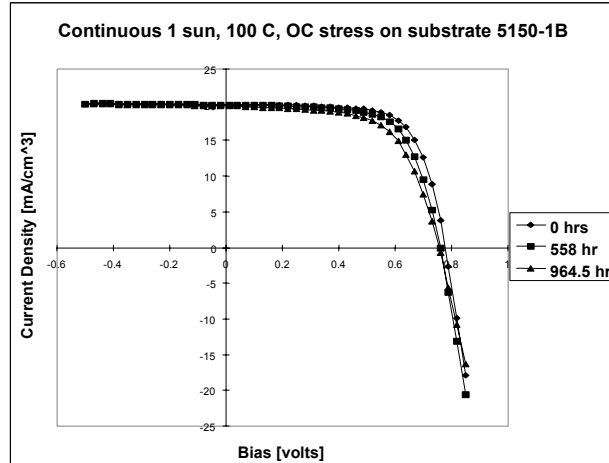


Figure 8: Overlay J-V plot of device performance under accelerated indoor stress

4.3. Analytical Studies to Better Understand Device Behavior

In order to develop a detailed understanding of the performance of our devices, the constituent films continue to be studied by X-ray diffraction (XRD), glancing angle XRD, XPS, and SEM SEM-EDS, ellipsometry, surface profilometry and UV-VIS-IR spectrometry at CSU. Devices have been studied by SIMS, CL and DLTS at NREL; DLTS at Lawrence Berkley Lab; and Glancing Incidence XRD at IEC.

The electrical properties of the devices are characterized through current/voltage (J-V), capacitance-voltage (C-V) and capacitance-frequency (C-F) techniques in our laboratory. A closed loop temperature controlled cryostat has been installed for measuring capacitance and other device properties in the dark at temperatures from 76K to 320K. This system has been used for measuring device capacitance as a function of temperature and applied voltage (C-V-T).

The most significant finding from these studies is that our back contact processing dopes the CdTe assisting in producing a low resistance back contact. Our back contact fabrication process utilizes no etching. Most other back contacts using copper have a separate p^+ layer, such as Cu_2Te or $ZnTe:Cu$. Analysis with GAXRD and XPS does not show the presence of a separate phase or a Cu_xTe layer at the back of our devices.

4.3.1. Copper Distribution Within the Device by SIMS

Secondary Ion Mass Spectrometry (SIMS) analysis of three of our devices was performed at NREL by Sally Asher. Two of the devices were fabricated during the same process run and fabricated under identical conditions including back contact copper processing. One of these devices was subjected to a significant amount of accelerated stress; the other saw no accelerated stress. The third device was from a different run but was processed similarly, except no copper was used in processing. The copper distribution of these three devices is shown in Figure 9. The SIMS analysis shows that there is copper in the CdS even when there is no intentional copper added during the processing. There is an increase in the Cu throughout the device with the intentional addition of copper. The largest increase is in the back approximately $0.4\mu m$. Furthermore, Figure 9 shows that there is a very small change in the distribution of the copper profile after stress.

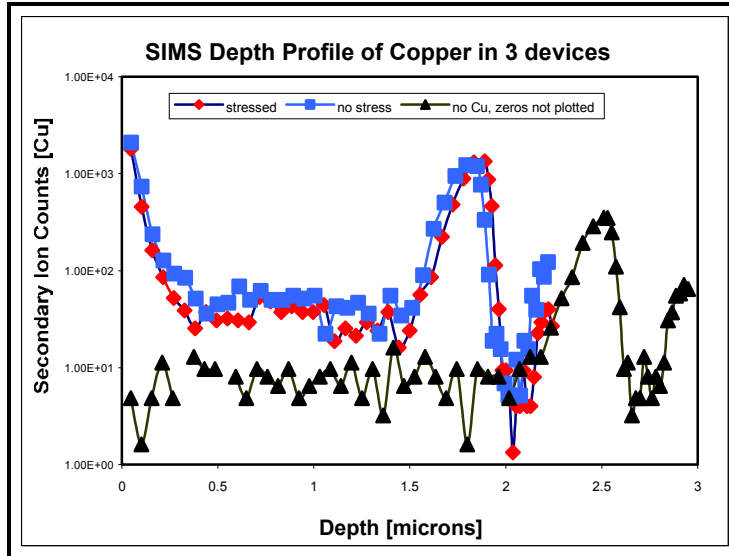
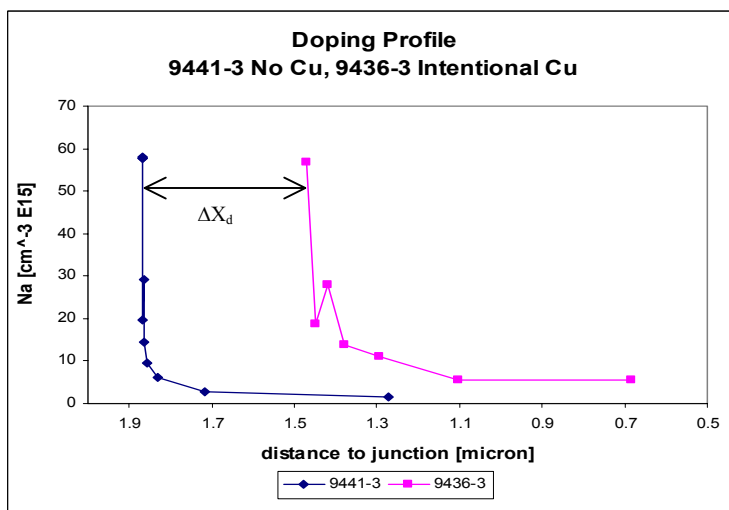


Figure 9: SIMS depth profile of nearly identical devices with and without stress. Stress condition: 3300 hours at 1000 W/m² illumination (5 hrs on out of 8 hr cycle), OC bias, 65 C temperature.

4.3.2. C-V Results for Devices With and Without the Intentional Addition of Copper

The doping profile from C-V analysis for devices with and without the intentional addition of copper is shown in Figure 10. The two devices were fabricated in the same process run. Surface profilometry measurements demonstrated that the samples within the run had the same thickness, within the error of measurement (0.05 μm). The decrease in the depletion width at reverse bias (ΔX_d) is a measure of the thickness of the doped region. This increase in dopant at the back of the CdTe is attributed to the large copper concentration near the back of the CdTe seen by SIMS analysis. The estimate of ΔX_d from Figure 10 is approximately 0.3 μm. This estimated thickness is similar to the thickness of the region with high copper concentration at the back of the device shown by SIMS in Figure 9. A similar variation in depletion width with the change in copper concentration for our devices has been reported previously [Sites 2002, Pudov 2002].

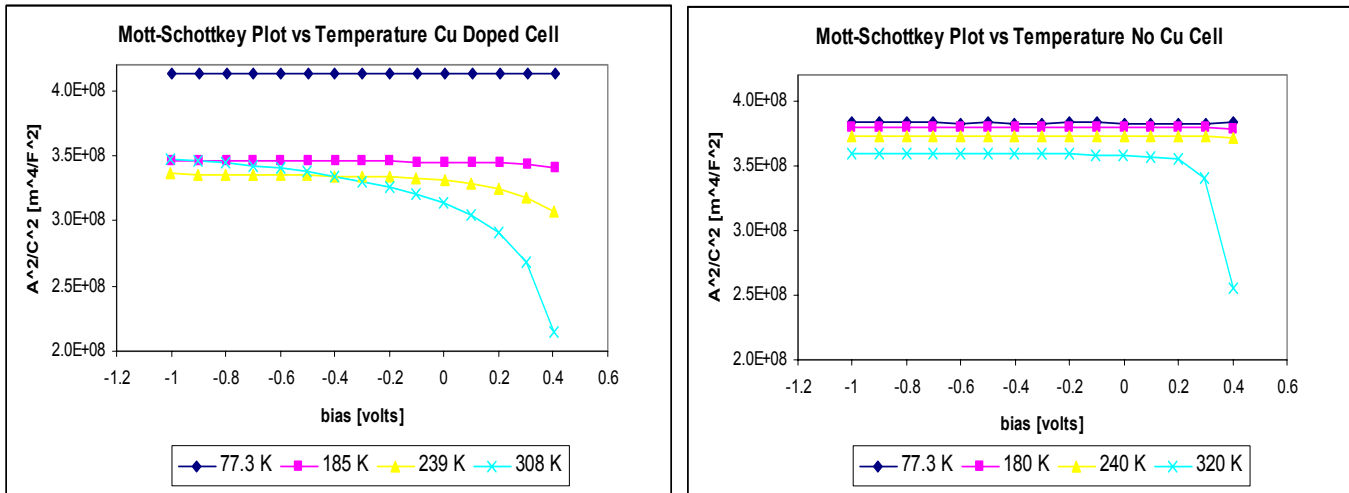


Figures 10: Doping profile of devices with and without copper

The total device capacitance is a combination of the junction and contact capacitance [Niemegeers 1997]. By assuming that the measured capacitance can be attributed only to the junction capacitance (assuming no contact capacitance), the thickness of the CdTe region doped with copper (ΔX_d) is an underestimation. All C-V measurements are performed at the highest frequency where minimal frequency dispersion is detected in order to minimize or eliminate the contribution of trapping states [Blood 1992, Mauk 1990].

4.3.3. C-V-T Results for Devices With and Without the Intentional Addition of Copper

In order to further understand the role of copper in our devices, capacitance -voltage (C-V) profiling as a function of temperature (C-V-T) was performed on our devices. The Mott-Schottky plots as a function of temperature is shown in Figures 11 and 12. The depletion width in reverse bias at 77 Kelvin matches the thickness of the CdTe film measured through profilometer measurements. The capacitance measurements were done at 100kHz. Higher frequencies could not be used due to inductance of the relatively long leads of the cryostat. However, when the device with copper was tested outside the cryostat with short leads attached directly to the device to minimize inductance, the difference in capacitance readings between 100kHz and 2.5MHz was only 6%, enabling the use of the lower frequency measurement. Capacitance vs. frequency measurements also show the device capacitance is not strongly dependent on frequency at the 100kHz range. This shows that the contribution of traps to the capacitance signal in Figures 11 and 12 is very small. The increase of capacitance with temperature for the device with copper at the back of the cell is due to the activation of copper based dopants.



Figures 11 and 12: Mott-Schottky plots showing activation of copper based dopants with temperature

4.3.4. C-V Profile after Stress

The doping profile obtained by C-V measurements on the same device after different amounts of accelerated stress is shown in Figure 13. The CdTe thickness in this device, estimated from profilometry measurements, is 1.8 μm . The thickness of the doped region is approximately 0.35 μm and it can be seen from Figure 13 that there is very little change in the copper doped region with stress. (The differences are within the limits of measurement

accuracy.) These results correlate with the SIMS result in Figure 9, which shows very little change in copper distribution with stress.

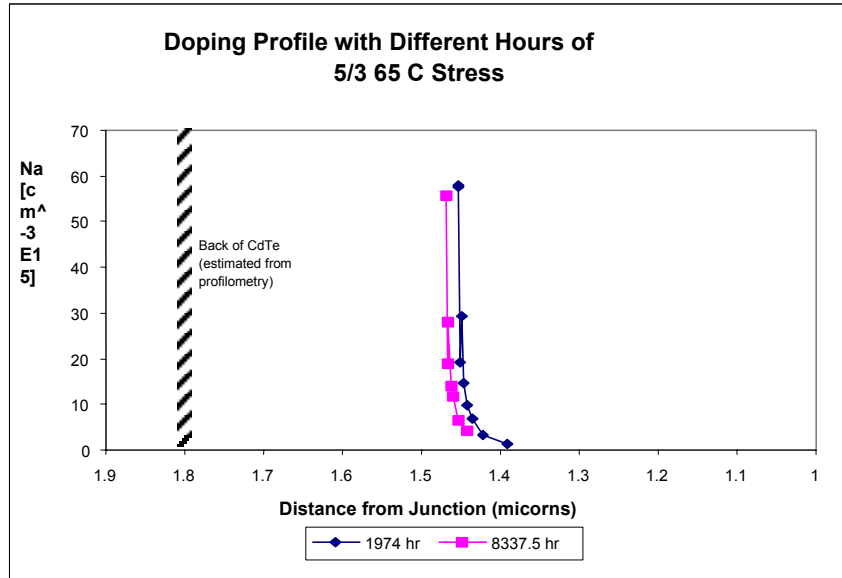


Figure 13: Acceptor density vs. distance from junction for a device with different hours of stress. . Stress condition: 1000 W/m² (5 hrs on out of 8 hr cycle) illumination, OC bias, 65 C temperature.

4.3.5. Other Results

Recent studies by Brian McCandless of IEC using GAXRD at slow scan rates indicate the possibility of trace amounts of Te and Cu_xTe at the back of our devices. More analysis is currently underway. XPS studies have been performed in collaboration with an expert who is currently a faculty member of the University of Missouri. The XPS studies show that the binding energy of Cu in CdTe is similar to the Cu of Cu_{1.9}Te. Measured copper quantities were below that needed for equivalent monolayer coverage.

Analysis of our devices with deep level transient spectroscopy (DLTS) and admittance spectroscopy indicates that at the optimum process conditions, the quantity of traps are very small. In the DLTS and optical DLTS (ODLTS) analysis performed at both NREL and Lawrence Berkeley Lab, only electron type traps were detected at levels below 3x10¹³ cm⁻³ as shown in Table 2. According to Steven Johnston [Johnston 2002] of NREL these levels are a lower bound estimate. This is due to the possible incomplete filling of all of the traps and to the limited temperature range explored (100-300 Kelvin). Concentrations of traps where the trap peak was outside of the measurement temperature range were unresolved. We are currently working to refine these estimates.

Substrate	Trap ID	Doping Density, Na [cm ⁻³]	Activation Energy, Ea [eV] Ec= energy of cond. band	Trap Density, Nt [cm ⁻³]	Technique
5151	E1	7.00E+13	Ec-0.39	3.00E+12	ODLTS
5151	E2	7.00E+13	Ec-1.5	8.00E+11	ODLTS
5151	Trap seen, peak beyond temp range studied		--	--	
7232	E3	1.00E+14	Ec-0.49	3.00E+10	DLTS
7232	E4	1.00E+14	Ec-0.75	6.00E+11	ODLTS
8734	Trap seen, peak beyond temp range studied		--	--	

Table 2: Trap density by DLTS and ODLTS

4.4. Improvement in Device Efficiency and Yields

Efforts aimed at improving overall cell efficiencies and reducing the standard deviation have resulted in improvements in both areas for one process run. The best to date efficiency distribution from one substrate are shown in Figure 14. The mean efficiency of the 14 cells is 12.6% with a standard deviation of 0.26%. The process modules in our pilot system are being improved further to demonstrate efficiency distributions similar to that shown in Figure 14 over 8 hour runs.

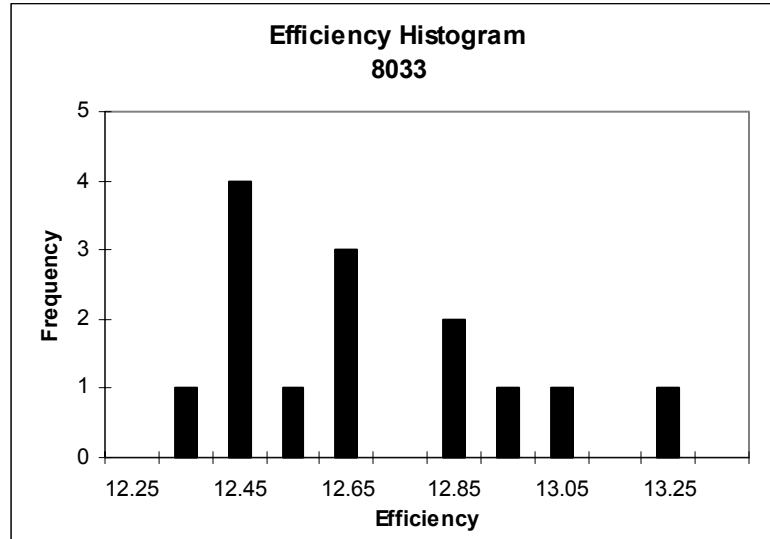


Figure 14: Efficiency histogram

5. PHASE II PLANS

As in Phase I, we will very closely adhere to the tasks outlined in the statement of work during Phase II. The focus of the efforts will be to further develop the understanding of stability, yield and efficiency of CdS/CdTe devices. We anticipate that further progress will be made towards demonstrating consistent stability. We will continue our collaborative activities with other research groups and provide assistance to industries as in Phase I.

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- Sites, J. R., A. O. Pudov, S. H. Demtsu, M. Gloeckler, K. L. Barth, R. A. Enzenroth, and W. S. Sampath, "Effect of Copper Concentration on CdTe Cell Operation", 29th IEEE PVSC, May 2002.

7. PUBLICATIONS, COMMUNICATIONS AND PRESENTATIONS

7.1. Publications and Presentations

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- Barth, K. L., R. A. Enzenroth, and W. S. Sampath, "Apparatus and Processes for the Mass Production of Photovoltaic Modules" US patent 6,423,565, July 23, 2002.
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7.2. Additional Reports, Communications

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Barth, K. L., S. Kohli, "X-Ray Diffraction Investigations of Film Stress on BP Solar CdS/CdTe Devices", Report to BP Solar, July 23, 2002.

Barth, K. L., R. A. Enzenroth, W. S. Sampath, "Investigations of Post Deposition Treatments using BP Solar CdS/CdTe Films", Report to BP Solar, February 2, 2002

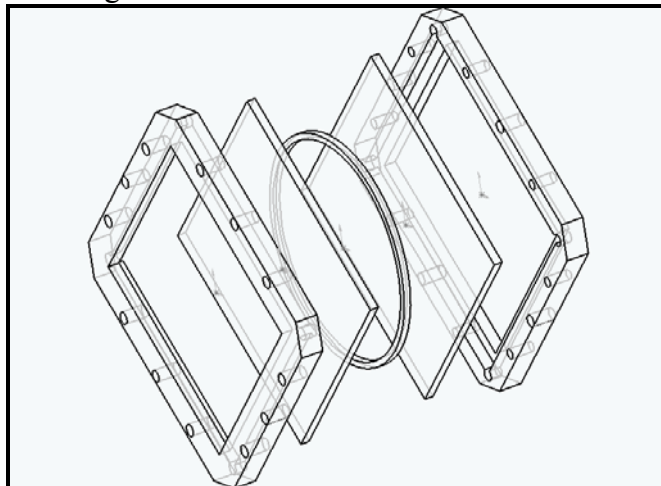
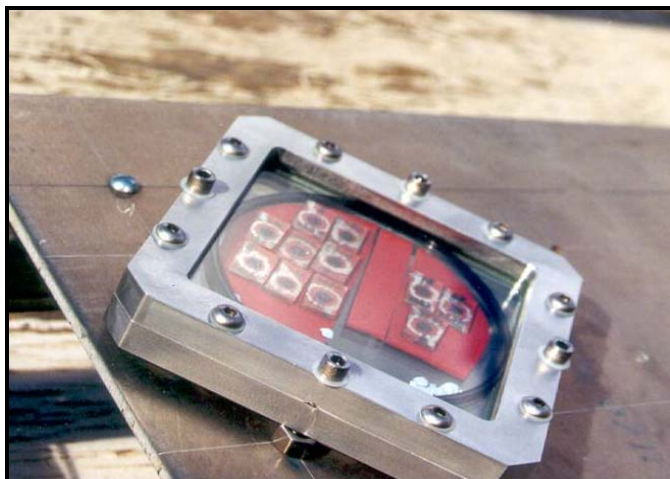
8. APPENDICES

8.1. Description of Improvements to Research Equipment

In this section, more details of our activities listed in section 3 are presented.

8.1.1. Outdoor Performance of Cells.

In order to develop an exact correlation between accelerated stress testing and outdoor performance, a unique fixture for exposing devices to outdoor conditions has been developed in our laboratory. This fixture utilizes a moisture tight, demountable arrangement. Non-encapsulated devices are inserted into the fixture which thermally emulates an encapsulated module. The devices can be removed for testing in the laboratory and then replaced for further exposure. The fixtures were tested for their ability to seal moisture by enclosing granules of indicating desiccant and submerging the fixture in water. After nine days, the desiccant in the fixture did not change color, demonstrating the ability of the fixture to seal against moisture. Five fixtures capable of testing 90 cells have been fabricated.



Figures 15 and 16: Photograph and schematic of the fixture for exposing un-encapsulated devices to outdoor conditions

Most of the published results of outdoor performance have been obtained from modules. Modules can have additional failure mechanisms such as interconnect degradation,

buss bar degradation and encapsulation failure [McMahon 1998]. The use of the outdoor fixture avoids these additional failure mechanisms. This enables accelerated indoor stress tests to be correlated to outdoor performance. Currently, 40 devices are being exposed to outdoor conditions in this fixture and device performance is being monitored periodically. Some of the results of the outdoor testing were given in Section 4.2.1.

8.1.2. Indoor Stress Testing of Cells.

We have significantly expanded and upgraded our capability for indoor stressing of cells to accommodate 250 cells in addition to the capacity that already existed. Our indoor light soakers enable independent control of illumination and cell temperature. Cell temperature is close loop controlled. A micro-thermocouple was used to confirm and calibrate the control thermocouple readings. The temperatures measured with the micro-thermocouples were within 0-2 degrees C of the control thermocouple readings. The new indoor stress fixtures have an additional control system incorporating redundant sensors. The additional control system has been wired to shut off of illumination (and heat) in case of primary controller failure, or excessive device temperatures.

8.1.3. Upgrading IV Measurement.

In order to keep records of device performance under indoor and outdoor stress the IV measurement system and the database for tracking results have been upgraded. The IV measurement in our laboratory was done with an HP 34401A for measuring voltage and a Fluke 8840A for measuring current and an HP 4145A for applying bias. All of this has been replaced by a Keithley 24203A sourcemeter. A Labview program was developed to run the Keithley 24203A using a GPIB interface. This has reduced the time for measuring IV by more than 50%. In addition to reducing the time for measurement, the newer setup allows for the IV measurement of modules. In addition to upgrading the current IV measurement, we have installed a Xantrex XRH 100-10 DC power supply to provide power to the ELH lamps and virtually eliminate variation in illumination due to fluctuations in the line voltage.

8.1.4. Upgrading the Database

All the results from our devices used to be tracked with a database that required manual entry of the data from IV measurement. This has been upgraded to enable the direct entry of cell performance data from IV measurement. The Labview program for IV measurement has been enhanced to allow direct export of data after IV measurement. The graphical processing of results from the database has been upgraded to allow better plotting and comparing of results. A student from our laboratory who is currently pursuing a Masters degree has completed a graduate level course in database design. As part of the course work he has developed a user-friendly interface to the database.

8.1.5. Residual Gas Analyzer (RGA) Installation

A Stanford Research System SRS 100 RGA has been installed on the system. Since our operating pressures are in the range of 40 mTorr, a bypass valve assembly was required to reduce the pressure at the inlet of the instrument. A turbopump has been installed to reduce the pressure at the RGA head. The RGA has been interfaced to a computer for data acquisition and control. The RGA system is functioning well. Experiments with the RGA have demonstrated that there is no increase in the partial pressure of oxygen when substrates

are transported into the vacuum chamber using our air-to-vacuum-to-air (AVA) transport system. The AVA seals were designed to accomplish this and the tests with the RGA validate the designs. Hardware was serviced as needed. Further servicing of the pumps, gages and controllers will be completed prior to the long duration runs.

8.1.6. Upgrading the process modules

Most of the vapor sources and substrate heaters in our system are graphite structures heated by quartz IR lamps and have a high degree of thermal uniformity ($\pm 2^\circ\text{C}$). However, three of the heaters in the system utilized "strip heaters" which did not provide the thermal uniformity of the other sources. These three heaters have been redesigned with the graphite/lamp configuration. Another heater associated with the CdCl_2 process has also been redesigned for increase uniformity and for easy removal of the unit for servicing and cleaning. This unit also includes a sensor to monitor the thermal stripping of the CdCl_2 film from the substrate during processing. These four heating units have been constructed, installed in the system and tested. They continue to function well.

8.2 Description of Activities with the National CdTe Team

Our group has been actively participating in National CdTe Team activities. It has had productive collaborations with Prof. Sites's group at Colorado State, as well as with researchers at BP Solar, National Renewable Energy Laboratory, Institute of Energy Conversion, Lawrence Berkley Labs, University of Missouri and others.

Collaborative research was being performed in conjunction with Photovoltaics Laboratory of CSU under the direction of Jim Sites and Alan Fahrenbruch of ALF. Devices have been fabricated at five different processing conditions incorporating various amounts of copper in the back contact. These devices were characterized through J-V as a function of temperature; capacitance vs. voltage and frequency and micro uniformity (LBIC) techniques. AMPS modeling of these devices was performed to gain further insight. These studies have helped in understanding how device performance changes as a function of the amount of copper introduced during processing. Results were reported [Pudov 2002, Sites 2002].

Many devices have been provided for the capacitance vs. voltage (CV) "round robin" study. The CV measurements performed in our laboratory on these devices closely matches the result obtained by Prof. Sites' group. This demonstrates that CV measurements can be reproduced in different laboratories.

Detailed investigations of the effect of water vapor on stability have been initiated. Stress tests are being performed in desiccated and un-desiccated conditions indoors and outdoors. The stability data on 4 sets of cells (at least 5 devices/set) which have undergone stress in the following conditions: 1) desiccated accelerated indoor 2) desiccated outdoor 3) un-desiccated accelerated indoor and 4) un-desiccated outdoors will be studied and reported. Devices have been provided for SIMS, CL studies and DLTS analysis to NREL. These included very similar devices which had been stressed and had seen no stress.

We have provided 51 devices for micrononuniformity studies. Devices were provided to Dr. Dhere of NREL and Moldova University for their collaborative studies with Jim Sites. Substrates processed with and without copper have been provided to B. McCandless of IEC for characterization of the films.

8.3 Description of Interaction with Industry

The activities of our group in helping industries are listed below:

At the suggestion of Doug Rose of First Solar, Doug Shultz of Ceramem was contacted and was provided many 3.6 x 3.2 inch glass substrates with CdS/CdTe films (CdCl₂ treated) to further their studies. Our group processed devices from CdS/CdTe material supplied by Canrom. The material was contacted and cells were defined and tested.

A joint study for better understanding the CdCl₂ treatment has been underway with BP solar. Many devices with efficiency values greater than 10% (highest 10.75%) have been fabricated on BP material utilizing our unique inline continuous processing technology. Results of this study were presented at the March CdTe Team meeting and presented to BP in a written report. These devices and ones which are being contacted by BP will be exposed to stress conditions.

A series of detailed XRD studies have been performed to characterize the residual stress in BP CdTe films, which have been subjected to different processing conditions. These studies are part of ongoing quality improvements efforts at BP Solar.

8.4. Additional Activities

We have made significant progress towards upgrading our continuous deposition system so that the process conditions (primarily vapor flux) can be precisely maintained over at least 8 hours and from run to run. We have made a few 3 in. X 3 in. minimodules using our scribing and interconnection technology. The results of the module fabrication efforts are very promising. In addition, numerical modeling of vapor sources for large (over 12 x 12 inch or greater) sources have been completed.

A model based on defects and dopants in the CdTe is being developed to understand the accelerated stress and outdoor stability results described in Section 4. Such a model is needed to develop procedures for quality control to assure that modules demonstrate consistent stability and performance in the field.

8.5. Graduate Student Activities

Two graduate students, Amit Bindal and Mukul Bhat, pursuing their M. S. degrees are supported through this project. They have assisted in the activities described in section 8.1.