562 CLASSES BEGIN **Tues. 27th August to Thursday, Dec 12th**

5:30 to 6:45 PM T R

- Divide yourselves into **FOUR** groups for doing group HW, Spice Labs, Pop Quizzes and Talks # 1 and #2. Do this ASAP and give the list of group members with full spelling and CSU ID #'s to both me and the grader.

- **Class Time:** Tuesday and Thursday 5:30 – 6:45 PM in B105 (Engineering B wing)

- **15 page syllabus will answer all your questions but is subject to in class updates.**

PROLOGUE to 562 Issues

Instructors teaching philosophy

- **ECE Students are the most important people at CSU.**
- **Not dependent on faculty.**
- **Faculty is dependent on them.**
- **Not an interruption of our work.**
- **They are the purpose of being at CSU.**
- **Students are doing us a favor when they come to our office.**
- **We are not doing them a favor by serving them.**
- **Students are part of our business, not outsiders.**
- **Not just a CSU ID number.**
- **They are flesh and blood human beings with feelings and emotions.**
- **Students come to us with their needs and wants.**
- **It is our job to address them with courteous and attentive treatment.**
- **Students are the life blood of this and every university.**
- **Without them we would close our doors.**
- **DON'T EVER FORGET THIS**

ECE562 Overview Grading

GRADING for 562 Power Electronics

Quick Overview: ALL efforts below are with a group from 1-6 people, so form a group ASAP.

1. **Pop Quizzes: 20%**
2. **Home Works: 5 %**
3. **Spice labs: 15%**
4. **Talk # 1: 20%**
5. **Talk # 2 40 % Special choice for those registered on ECE 461 as well as 562. A** talk on **DC to AC inverters** @ fixed phase but variable amplitude and frequency for transmission and gear free motor drives is accepted

Send REVISED PPT slides of talks 1 and 2 and associated WORD papers to Prof. Collins only and not to the grader.

TOTAL 100 %

I may or may not allow extra credit in 562 such as:

1. **Semester long special topic like right hand zeros effect of stability of buck-boost converters 7%**
2. **Class participation: 3 %**

A-F GRADING SUMMARY with plus minus fine tuning for 562

Letter grades are on an F to A + scale with plus minus fine tuning on all letter grades.

Score (X)	Letter Grade
X > 100	A+
X > 96	A
X > 93	A-
X > 91	B+
X > 86	B
X > 83	B-
X > 81	C+
X > 59	C
X < 59	F

No C minus grades allowed. Numerical grades are through CANVAS. Letter grades are via Aires Web

Instructor: Professor George Collins, Email: **gcollins@engr.colostate.edu**

Grader: TA: **TO BE ANNOUNCED**

Here are few guidelines regarding HW, Spice Labs and POP QUIZ submissions to the grader via CANVAS-

1) Preferably write your solutions in MS Powerpoint. Number of slides may vary depending upon the solution BUT always number your pages.
2) Please use the file name format as- "ECE xyz_HW/POP QUIZ#_Group#".
3) Only group leader will submit the final ppt of HW/POPQUIZ.
4) Please cc all the group members when submitting the final ppt for HW/POPQUIZ.

In summary, grading for 562 is in six parts as indicated above with opportunity for both group and individual efforts. Group efforts are encouraged in HW, Spice assignments and talks as well as associated papers. Groups of up to but not to exceed 6 students per group, are acceptable to encourage team efforts and provide the opportunity to learn team dynamics. Upon leaving CSU you will work in a company in teams—the Word and PowerPoint skills you learn in presenting technical materials in 562 will be to YOUR benefit. The practice and experience of living with the "psychodrama of technical group efforts" will also benefit you personally

To keep it all clear and fresh, the grader will send out a weekly memo usually a week in advance the prior Friday detailing:

1. **Last week's efforts**
2. **This week's efforts and what's due the coming week (e.g. Pop Quiz)**
3. **Next week's efforts and due dates for all new assignments**

Group efforts are one big emphasis in 562. Upon leaving CSU you will work in a company in teams—the Word and PowerPoint skills you learn in presenting technical materials in 562 will be to YOUR benefit. The practice and experience of living with the "psychodrama of technical group efforts" will also benefit you personally.

- SEND the grader (all of the following are group efforts—form a group ASAP for HW solutions, Spice labs, Pop Quiz solutions
- **Text Book**: Fundamentals of Power Electronic, by R. W. Erickson and D. Maksimovichttp://www.amazon.com/Fundamentals-Electronics-Second-Robert-Erickson/dp/0792372700/ref=ntt_at_ep_dpt_1
- **Class website:** http://www.engr.colostate.edu/ECE562/ and CSU calendar http://www.calendar.colostate.edu/
- Industry seminars are great—try this one from Arrow Electronicshttp://www.arrownac.com/offers/vision-2013/index.php

Introduction to 562

Disclaimer Notice:

All items in this memo are subject to change by Prof. Collins in LATER class announcements and items are considered only a preliminary guide to the student. For example, the ECE562 classes can cover high frequency magnetics/transformers/inductors rather than more details of PWM circuits or basics of resonant converters, if strong class interest exists—each semester is unique in its class preferences in this diverse field. In week # 9 we will have a mid-class review of past and future topics in which you are encouraged to input your desires for the remainder of the class lectures. This course requires a lot of extra work in the beginning of the semester and a lot LESS work at the end of the semester, so you have time for other courses, finals and job interviews.

The class notes are password protected
Username: Student
Password: Power!

Please forgive this lengthy syllabus, schedule and grading missive, but there are lots of issues to cover and keep it all clear and fresh.

Because of the breath of power electronics each year 562 is different. Perhaps the course should have a "under construction, pardon our appearance" sign. **All items in this memo are subject to change by Prof. Collins in LATER class announcements and items are considered only a preliminary guide to the student.** For example, the ECE562 classes can cover high frequency magnetics/transformers/inductors rather than more details of PWM circuits or basics of resonant converters, if strong class interest exists—each semester is unique in its class preferences in this diverse field.

During the semester I will talk several times about second mouse gets the cheese. Below I partially document that assertion in high tech.

"First Mouse a goner"	"Second Mouse a Winner"
1.QDOS and Wordstar	MICROSOFT
2. Books.com	AMAZON
3. Blackberry Phone	Apple Phone
4. Alta Vista Search	GOOGLE
5. Myspace Social media	FACEBOOK
6. Oldie but goodie is DC from Edison	AC from Westinghouse

ACADEMIC INTEGRITY

This course will adhere to Academic Integrity Policy of CSU General Catalog and Student Conduct code. It is expected in this course that all students will not give, receive or use any unauthorized or undocumented assistance in their group efforts as well as individual efforts. All appropriate sources need to be referenced and it's best to do so in IEEE format for references/sources. For details on CSU academic integrity policy goes to:
http://learning.colostate.edu/integrity/index.cfm

Problems will be solved according to CSU policies: http//tilt.colostate.edu/integrity/guides/what to do. cfm

562 COURSE OBJECTIVES

This course will teach students how to understand, analyze, design and better employ new commercial IC power supplies on a chip or on a board in any electronic system requiring powered DC levels different from the general DC system bus. Typically this is 6-12 additional DC levels. One illustrative commercial example is a remarkable **Dialog Semiconductor** product which provides, on ONE IC chip: 18 LDO(low drop out regulators) for low noise voltages needed for cell phone transceivers , two Buck converters for cell phone processors and semiconductor memory power supplies and one Boost converter for both driving LEDS for LCD screen backlighting or for the flash camera. ALL on one IC chip and driven by the on board batteries only!! Texas Instruments has similar products. This kind of chip allows for low cost cell phones employing various DC voltages all from one rail voltage. Cell phone sales are two billion per year and smart phones 600 million per year. This allows you to grasp why power management, at low cost, is on an IC chip or chips.

This course will cover the two major approaches to high efficiency DC-DC conversion in detail: Pulse width modulation and resonant converters. Both employ ideal lossless "L-C" networks and ideal lossless switches. The DC-DC PWM conversion is primarily an IC solution to point of load DC power requirement and the resonant DC-DC conversion is primarily for high performance DC power applications at kW levels, usually implemented on PC boards with discrete components, often called BRICKS. However, some attention will be given to linear power supplies like low drop out regulators and switched capacitor supplies for a comparison to our two circuit types. Moreover LDO's provide the lowest ripple rails for powering critical electronics devices, like transceivers and high speed serial interfaces to minimize the bit error rate (BER).

I hope by the end of the required talks in 562 or even sooner, all students appreciate the old saw " to read without reflecting is like eating without digesting". Or for the simple fools like me the shorter version "knowing the facts versus knowing the truth".

Cost "the four letter word' plays a key role in 562. This is just an economic word for the common good. So in a cell phone application the IC power chip has a potential market of 2 billion/ year—so cost and size drives all design.

Practice makes perfect
Kaizen is a Japanese word for" continual improvement and is common in manufacturing as pioneered by Toyota.

Presentation skills too can be honed through repetition, listening to talks and critique of our own talks

In DETAIL the ECE562 grading is scored as follows in 6 parts:

1. **(5 % of grade) Four HW Homework assignments** @1.5 pts each will comprise 6% of the grade. See page 4 of this document for details of assignments and due dates from Chapters 2,3,4and 5. In general HW assignments are due on Tuesdays the week after they are assigned. I will email each of you to remind you of HW problem changes and due date changes if any.

   Roughly speaking, HW due dates for the HW assignments are as follows UG is undergraduate and they do only a HW problems indicated, whereas graduate students do all assigned problems:

HW#1: Ch 2 of Erickson Pbms. 1(UG), 2(UG),3,4,6,: DUE week 4 day 1 (Tues. 17 Sept)

HW#2: Chapter 3 of Erickson Pbms. 8(UG),9,10 (UG).: Due Week 8 day 1 (Tues. 15 Oct)

HW#3: Chapter 4 of Erickson Pbms. 2(UG),4,5,7(UG): Due week 10 day 1 (Tues. 29 Oct)

HW#4: Chapter 5 of Erickson Pbms. 1(UG),4, 5(UG),14: Due Week 14 day 1 (Tues. 26 Nov.)

2. **(15% of grade) Five Spice assignments**@ 2 pts each are worth 10 % of the grade and are described in detail below where I give the schedule of SPICE due dates. In general Spice labs are due on Tuesdays too, usually when no HW is due. Use student versions of Cadence, NL5 or LT(linear technology website) SPICE ALL OF WHICH ARE FREE.

NL5 Spice Simulator vs. Cadence Virtuoso for Spice Labs of DC to DC converters

NL5 Spice Simulator and Cadence Virtuoso are programs that allow users to design circuits in a schematic view and then run various simulations on the designs. While they both have schematic capture and simulation capabilities, the extent of those capabilities are very different. Cadence Virtuoso is an industry standard software package that provides full IC design, from schematic design and simulation all the way up to physical chip layout. Cadence requires detailed parts libraries in order to simulate real components sold by different vendors, which is needed when designing real life chips. The main advantage Cadence has over NL5 is its extensive capabilities. Cadence offers every type of simulation, design check, and various tools a designer would ever need in a circuit-design package, and is regularly used in large-scale chip design in the IC industry. Some of the advanced simulations Cadence offers include simulating different design corners, Monte Carlos sweeps, and process variations. When used at its full potential, Cadence is a very powerful circuit-design program.
Cadence has two main disadvantages however, which are cost and complexity. It is a very expensive software package that typically costs companies and school thousands of dollars per license. For the most part, only large organizations can afford Cadence, so smaller companies or individuals must look elsewhere. In addition to its high cost, Cadence is also a very complicated program to master. It usually takes years just to learn to use a lot of the more common schematic simulation modes. Using layout and the more advanced simulation modes further increases the complexity of the program. In short, in order to use Cadence to its full potential and “get your money’s worth”, one must spend several years mastering the software. For students trying to use a circuits program for the purpose of learning circuit theory, Cadence is an ineffective option since it is so expensive and takes so long to learn how to use.

NL5 on the other hand is a very good candidate to use for educational purposes. To start, it is completely free to download and use. Unlike Cadence, it can be installed on Windows or Mac, and is a very small program (Cadence is typically run on Linux, and is a massive software package, memory-wise). In addition, NL5 is extremely simple to use compared to Cadence. It has a very straightforward GUI that is not overloaded with unnecessary content. The components in the somewhat limited library are all very basic and easy to assign values to. Simulations (AC, transient, and parametric sweeps) are pretty easy to master after going through a step-by-step tutorial of them. Another important point is that nearly all of NL5's functionality is always visible and available to the user on the schematic design screen. This means that it is not necessary to search through bloated drop-down menus for different parts of the program. Because of its simplicity, NL5 is relatively easy for students to pick up and use to build basic circuits and run basic simulations for the purpose of learning how different circuits work.
While the simulation capabilities of NL5 are much lower than Cadence, it is the better choice for educational settings because of its low cost (free!) and simplicity. Using a program like NL5 allows students to spend most of their time running simulations and analyzing circuits, and not troubleshooting the program itself or trying to learn how to use basic functionality.

Personally I prefer Linear Technologies LT SPICE available free.

FIVE Required SPICE Assignments@ 3 points each (15 Points total).

SPICE LABS due Tentatively each week tentative dates are subject to change by the grader on CANVAS as follows:
buck simulation assigned Tues 27 Aug. due Tues. 3 Sept.
boost simulation assigned Tues 3 Sep due Tues.10 Sept.
buck-boost assigned Tues.10 Sept. due Tues.17 Sept.
SEPIC assigned Tues.17 Sept due Tues.1 Oct. during TALK # 1
CUK assigned Tues.1 Oct. due Tues.8 oct. during TALK # 1
Optional L-C-C or L-L-C RESONANT converter Spice labs due BEFORE Tues. 27 Nov

Together the five labs will lead you through the major commercial DC to DC converter circuits: Buck, Boost, buck-boost, SEPIC and Cuk. Note that there is EXTRA CREDIT FOR THOSE who do Spice analysis for either the L-C-C or C-L-L resonant circuits, which can be found in the course website.

3. **TALK #1 20 % of final grade. We will have four talks: Tues.1 Oct to Thur.10 Oct.,** (20% of grade) Talk #1/Paper #1 given as a group effort will count for 20%. Talk # 1 will tentatively have each of 4 student groups are talking for the entire class period.

Sign up your group date ASAP

Talk #1 Dates (Week 6 & 7) assuming four student groups

Tuesday, Oct 1, 2019

Thursday, Oct 3, 2019

Tuesday, October 8, 2019

Thursday, October 10, 2019

Prior to your talk # 1, I will cover

"Multiphase buck converters to power microprocessors and FPGA's". This is the mother of all Buck applications and summarizes all we learned about BUCK CIRCUITS that operate below or near one Volt and can follow 100 A / micro second changes. INDEED 16 PHASE Buck converters can deliver >1000 A @ 0.7 V

REPEAT Talk # 1 is worth 20 points total 15 for PPT and 5 for word

PPT Presentation grades are as follows:
1. TECHNICAL ACCURACY 9/15
2. PPT Slide ORGANIZATION 3/5
3. CLARITY OF MATERIAL-SHORT LIST OF TOPICS IN DEPTH COVERAGE BETTER THAN MANY TOPICS VERY SHALLOW DOVERAGE 1/15
4. PROPER SPELLING GRAMMAR REFERENCES 1/15
5. FOLLOWING THE MEMOS ON TOPICS TO BE COVERED 1/15

WORD PAPER GRADE OUT OF 5 AS FOLLOWS:
1. TECHNICAL ACCURACY 2/5
2. PAPER ORGANIZATION 1/5
3. CLARITY OF MATERIAL-SHORT LIST OF TOPICS IN DEPTH COVERAGE BETTER THAN
MANY TOPICS VERY SHALLOW DOVERAGE 1/5
4. PROPER SPELLING GRAMMAR REFERENCES .5/5
5. FOLLOWING THE MEMOS ON TOPICS TO BE COVERED .5/5

After talk # 1 Collins 562 LECTURES RESUME covering losses in real converters and associated heat management as outlined in Chapter 3 of our text.

4. **TALK #2 (40 % of grade) has four talks on separate topics in power electronics chosen by the group interests:**

NO CLASS 15 NOV.

1. **Any topic in power electronics is acceptable. Suggested below is a talk on Boost converters for ideal rectifers. For students also in 461 variable anothjer choice is frequency drives for motors can be used in both classes. Again Special choice for those registered on ECE 461 as well as 562. A** talk on **DC to AC inverters** @ fixed phase but variable amplitude and frequency for transmission and gear free motor drives is accepted

Talk #2 Dates (Week 12 &13) assuming four student groups

Thursday, November 12, 2019

Tuesday, November 14, 2019

Thursday, NO CLASS Thur November 21, 2019 before thanksgiving break

TALK #2 is worth 40 points total: 35 for PPT and 5 for word as broken down below

Talk # 2 PPT Presentation grades total sum to 40 and are as follows:
1. TECHNICAL ACCURACY 20/35
2. PPT Slide ORGANIZATION 7/35
3. CLARITY OF MATERIAL-SHORT LIST OF TOPICS IN DEPTH COVERAGE BETTER THAN MANY TOPICS VERY SHALLOW DOVERAGE 4/35
4. PROPER SPELLING GRAMMAR REFERENCES 2/35
5. FOLLOWING THE MEMOS ON TOPICS TO BE COVERED 2/35

WORD PAPER GRADE OUT OF 5 AS FOLLOWS:
1. TECHNICAL ACCURACY 2/5
2. PAPER ORGANIZATION 1/5
3. CLARITY OF MATERIAL-SHORT LIST OF TOPICS IN DEPTH COVERAGE BETTER THAN
MANY TOPICS VERY SHALLOW DOVERAGE 1/5
4. PROPER SPELLING GRAMMAR REFERENCES .5/5
5. FOLLOWING THE MEMOS ON TOPICS TO BE COVERED .5/5

In general to learn boost circuits well I recommend:

Suggested TALK # 2: groups cover BOOST Converters for Ideal Rectifers. This is in our text as two chapters!

This is the mother of all boost applications and be sure to include the role of right half plane zeros in feedback instability of boost converters

Each group must sign up for a specific date and with the same topic for TALK # 1 " Trends in both prior art analog control of PF correction boost circuits as well as new digital control methods pioneered by Analog Devices.

To make this a learning experience and to insure "you get it" I expect you to cover the following issues for the % of the talk #1/paper grade indicated below by sub-topic for either synchronous Buck or synchronous Boost converters:

a. (15 %) Compare PF of a rectifier with a C load as regards: no PF correction, with passive PF correction, and with active boost circuit inserted to achieve PF

correction. Include GOVERNMENT grid harmonic regulations up to 39 harmonic.

b. (15 %) Describe the replacement of the BOOST diode with an actively driven FET (synchronous Boost) and compare to the diode version for heat losses and voltage drops.

c. (30 %) Paralleling many Boosts (multi-phase Boosts is best done with digital control) it is possible to achieve increased di /dt performance yet maintaining low ripple DC. Explain by circuit drawings and circuit equations how this is accomplished both via analog and digital means in the control loops by:
    1. Switching all FETs in unison
    2. Phasing the FET turn on's so ripple is reduced
    3. Comparing the performance of a versus b above

d. (20 %) Multi-phase boosts have increased ripple currents in each stage. To decrease this we use coupled inductors with each pair of boosts in parallel as discussed in class.
e. (20 %) Show how digital control of the proper duty cycle "D" to achieve PF = 1.0 and no harmonics is achieved both via both analog and digital means for both single and multiple boost converters.

Let me know if your group needs a specific talk date as early as possible. Email the PPT SLIDES to me as email attachments, only after taking into account the issues raised by myself for additional effort, at your talk. Word Paper is sent to the grader ONLY, as email attachments so we have a record of receipt date versus the due date.

I recommend Microsoft SkyDrive for student cooperative projects/talks/papers that many students in a group can share edits as they occur. It is deeply integrated with Microsoft Office on both Windows and Mac's

HOWEVER, in talk # 2 any other topic in power electronics is fine but I prefer the topic of DC to AC converters due to its importance to solar and wind energy as well as motor control in electric cars.

Second recommended TALK #2 on INVERTERS for students also in 461: DC to Ac converters for the AC Grid at fixed output frequency of 60 Hz

1. DC to Ac converters for the variable frequency motor drives

The details of synthesizing AC wave forms from DC with both variable amplitude and variable frequency

2. Discuss power factor requirements of the EU's 61000-3-2 which specifies acceptable levels of the first 32 harmonics of the AC mains (3%).
3. Describe in detail the electronic interface circuits for variable frequency motor drives using commercial examples

FINAL GRADES

YES the possible total is possibly >100 % because of possible ex credit and class participation and final grades will be determined as announced on class :

Our approach will be more traditional with both + and - letter grades to achieve a sliding curve and a distribution of grades. .In an ideal statistical world we would seek in a class grade distribution as follows:

Grading will be curved with students above the median receiving an “A”, students below the median and above one standard deviation below the median receiving a “B”. 1 to 2 standard deviations below the median will receive a “C”, 2 to 3 standard deviations below will receive a “D”, and anything lower will receive an “F”.

With plus minus grading this becomes:

A-F GRADING SUMMARY with plus minus fine tuning for 562

Letter grades are on an F to A scale with plus minus fine tuning on all letter grades.

Score (X)	Letter Grade
X > 100	A+
X > 96	A
X > 93	A-
X > 91	B+
X > 86	B
X > 83	B-
X > 81	C+
X > 59	C
X < 59	F

No C minus grades allowed. Numerical grades are through CANVAS. Letter grades are via Aires Web

In summary, grading for 562 is in six parts as indicated above with opportunity for both group and individual efforts. Group efforts are encouraged in HW, Spice assignments and talks as well as associated papers. Groups of up to but not to exceed 6 students per group, are acceptable to encourage team efforts and provide the opportunity to learn team dynamics. Upon leaving CSU you will work in a company in teams—the Word and

PowerPoint skills you learn in presenting technical materials in 562 will be to YOUR benefit. The practice and experience of living with the "psychodrama of technical group efforts" will also benefit you personally

Dates, are front loaded to the first HALF OF THE COURSE

Tentative Deadlines for Pop Quiz's, Lab's and Homework's

Final dates set by grader via CANVAS

Deadlines Dates	Pop Quiz	Labs	Homework's
28 August		**Buck Spice Lab**	----------
September 4		**Boost Spice Lab**	----------
September 6		----------	----------
September 7	**Pop Quiz #1**		
September 11		**Buck Boost Spice lab**	**HW #1 : Chapter 2 Problems** 1(UG), 2(UG),3,4,6
September 13		----------	
September 14	**Pop Quiz #2**		
September 18		**SEPIC Spice Lab Pop quiz # 3**	----------
September 20		----------	----------
September 21	**Pop quiz # 3**		
September 25		**Cuk Spice Lab**	----------
	----------	----------	----------
October 1st	----------	----------	----------
October 2		----------	----------
October 8th	----------	----------	----------
October 9th			**HW #2 : Chapter 3 Problems**8(UG),9,10 (UG)
October 11	----------	----------	
October 12	**Pop Quiz #4**		
October 19	**Pop Quiz #5**		----------
	----------	----------	----------
October 23	**Pop Quiz #6**		**HW #3 : Chapter 4 Problems** 2(UG),4,5,7(UG)

October 25	----------	----------	
October 30	**Pop Quiz #7**		----------
Nov 15	----------	----------	
November 13	**Pop Quiz #8**		----------
November 27			**HW #4 Chapter 5 Problems** 1(UG),4, 5(UG),14

Pop Quiz's, Homework's, SPICE Lab's to be sent to Grader via CANVAS.

Special Talk # 2 opportunity for students in BOTH 461 and 562 : VARIABLE FREQUENCY MOTOR DRIVES

Alternatively groups for talk # 2 may present on "Variable Frequency Motor Drives". Moreover, if group members are in 562 Power Electronics they can use the same talk in both courses. Each week we will hear from two groups for a total of four group talks/week. Due the importance of variable frequency motor drives student groups can choose this topic for both Talk/paper # 1 and later in the semester talk/paper # 2. Moreover students enrolled in BOTH 461 and 562 can use the same talk in both classes.

Motors and motor drives are key technologies for a variety of reasons. First >60% of grid energy goes to motors. Moreover, improvements in efficiency from input AC power to Torque- RPM mechanical energy at loads is an on-going green revolution as it creates "Negawatts" of saved energy that need not be generated. Electric cars will also be more competitive with these "variable frequency" motor drive improvements.
In short the goal of the new power electronics technologies is increased efficiency motor operation, smaller size and lighter weight electric motors and eliminating the need for mechanical gear trains to meet the applications specific T_{OUT} – N_{OUT} mechanical load requirements by variable frequency drive electrical means alone.
So a special opportunity is offered to students in both 461 and 562 courses to do talk # 2 on motors/motor drives. An emphasis list of items to cover is given below for 461 presentations and a different list of items for 562 student presentations. Students MUST add to this according to their group's interests.
For those students who will give the same talk in both classes both emphasis lists must be covered in the presentation that will give twice once in each class.

461/ 562 Joint INVERTER presentations: Required High Points:

1. Describe the Z_{IN}, V_{IN} and I_{IN} seen by the power electronics drives (e.g. the motor's electrical input characteristics) versus the varying T_{OUT} –N_{OUT} curves of the mechanical load for:
    a. Brushless DC Motor (BDCM)

b. Synchronous motor
c. Permanent magnet Synchronous motor (PMSM)
d. Induction motors

In short review the T_{OUT}-N_{OUT} vs V_{IN} - I_{IN} curves for the four most used motors.

2. Provide web links to manufacturers spec and application notes and their major arguments to justify the separate claims that “PMSM” technology is the best versus “BDCM” technology is best versus Synchronous or induction motors. This is easily resolved by distinguishing what mechanical loads each technology is best suited for. Do this for the four the chosen motors at the three mechanical load levels of :
    a. Low HP < 1 HP
    b. Medium HP < 10HP
    c. High HP > 100 HP
3. Commercial motor control systems consist of: sensors, command and control chips and power train drives.
    a. Describe in detail spatial location, type and output levels from the sensors for rotor position and other motor parameters needed for control decisions.
    b. Give three commercial motor control chips or board level hardware control systems.
    c. Compare and contrast the advantages and limitations as well as cost of high power switch hardware in the drive train employing :
        a. Thyristors
        b. IGBT’s
        c. IGCT’s and it’s varients of MOS control

        Go to manufacturer’s websites and get specs for the high power switches as well as application sheets for motor drive applications with these same switches and their control drive electronics.
        d. Provide two examples of commercial power train electronics from switch drives to variable 3 phase output V(f) from power switches.

562 Presentations Required High Points:

1. Explain the cost and reliability considerations for the motor centric items listed in 461 point #1 as well as the best of the breed for applications at the three HP levels for the four motor varieties:
    a. Brushless DC Motor (BDCM)
    b. Synchronous motor
    c. Permanent magnet Synchronous motor (PMSM)
    d. Induction motors

2. Explain in detail the differences and advantages as well as disadvantages of DSP vs FPGA vs microprocessor control methodologies and switch algorithm flexibility as well as cost.