ECE451/ECE450 Digital System Design and Experiments

Instructor: Tom Chen

1 Objectives

ECE451 is a senior level course on digital design techniques. The purpose of this course is to provide students with opportunities to learn different digital systems and their practical applications, and various design techniques for different types of digital systems. Because this is a course related to designing hardware, a great deal of emphasis will be paid to practical issues in designing digital systems which combines both the software and hardware skills in a top-down design flow. Practical design issues can be understood only by going through a set of extensive design experiments in ECE450 both in the form of software programming at a higher level of design hierarchy and in the form of hardware building and debugging at a lower level of design hierarchy. The behavioral level design of a digital system is often performed using hardware description languages (HDLs) such as Verilog. Students taking this course will learn how to use Verilog to describe behavior and functionalities of any complex digital systems. The gate level implementation of a digital system are mapped to an field programmable gate array device for verification. Therefore, students will go through the entire design process of describing hardware using software languages, mapping it into gates and simulating the gate level design, and finally load the schematic design on to a silicon chip to verify the functionality of the system in hardware.

2 Prerequisites and Corequisites

Students are required to have taken ECE102 and ECE202 and have a grade better than C in both classes. Having sufficient knowledge about high-level language programming in C, Java, or C++ will be a plus. Students MUST register ECE450 together with ECE451. ECE450 is the lab component of the ECE451.

3 Detailed Course Outline (Week-by-Week)

Following is a tentative course outline. It is subject to change depending on progress in class instruction and the design project.

Week	Topics and Lab Contents
1,2	Review of basic logic design, number systems, and basic logic families (Chaps. 1, 2, and 3)
3	Introduction to Verilog/VHDL and design tools
4,5	Design of combinational logic (Chap4 and 5)
6,7	Design and optimization of sequential logic state machines (Chap7 and 8)
8,9	Examples of some sequential logic curcuits and their implementation (Chap9, 10, and 11)
10,11	Introduction to programmable logic devices
12	Implementing combination logic with PLDs (Chap6)
13	Arithmetic logic
14	Design of data path logic
15	Design of control logic
16	Review and exam preparation

4 Textbook and Additional Readings

The textbook for ECE451 is "Contemporary Logic Design" by Randy H. Katz. There is a printed copy of the slides used in this course on sale in the bookstore. Students are strongly encouraged to have this set of slides since sufficient materials covered in this course cannot be found in the textbook. The reference books for additional reading are:

- "Digital Design, Principles and Practices" by John Wakerly.
- "Digital Design Fundamentals" by Kenneth J. Breeding, Prentice-Hall, 1992.
- "Computation Structures" by S.A. Ward and R.H. Halstead Jr., McGraw-Hill, 1990.
- "Logic Synthesis" by Srinivas Devadas et. al., McGraw-Hill, 1994.

5 Grading Policy

Homework	10%
Midterm	30%
Final Exam	35%
Labs and Design Project (ECE450)	25%

6 Office Hours

Instructor Office Hours: Wednesdays, 3-5pm, or by appointment. Office Location: Scott room 352. Office Telephone: 491 6574. Email: Thomas.Chen@colostate.edu

There are two Lab TAs for this class.

- Yusra Obeidat (yusraobeidat@yahoo.com). Office Hours: Tuesdays 10-11am and Thursdays 4-5pm.
- Devashish Vedre (drv11291@gmail.com). Office Hours: Fridays 10am-noon.

All TA office hours will be in Scott's atrium area. If you have time conflicts with office hours, you can also catch the TAs during the Lab hours, or email them to make appointments outside the office hours. The grader for this course is Devashish Vedre.