ECE102 Digital Circuit Logic FALL 2019

Objectives: To understand the concepts of digital logic and learn methods and tools for the design of digital circuits.

Prerequisites: Major in ECE or prior approval

Instructors: Professor Anura Jayasumana
Office/Phone: Engr C201D (970) 491-7855
Email: Anura.Jayasumana@Colostate.edu
Office Hrs: See Canvas for current hours.

URL: Students are expected to visit Canvas frequently for class handouts, homework assignments, lab assignments, and important announcements. Some of the information is also available at the public home page for ECE102 at http://www.engr.colostate.edu/ECE102/FALL19.

Grading Policy: The grade will be based on quizzes & homework (20%), labs (20%), midterm 1 (15%), midterm 2 (15%), midterm 3 (15%), and the final exam (15%).
The +/- grading scheme will be used, with the scale

>90% -- A, A+
>80% -- B, B+, A-
>70% -- C, C+, B-
>60% -- D

You must pass each lab assignment (score > 60%) in order to pass the course. A bonus not exceeding 5% will be awarded for neatness and clarity of presentation on some of your graded work.

Quizzes: On-line quizzes will posted on Canvas. They will demand a current familiarity with the course material. An integral part of this freshmen course is a professional development component and the associated quizzes and surveys.

Homework: Homework assignments are to be submitted via Canvas. Selected questions (announced in advance) from each homework assignment will be graded. However, turn in all of the assigned problems. All assigned problems are equally important for the development of your understanding of the subjects of digital logic. To receive full credit for your homework, show all reasonable steps in solving the problem. Written solutions will be available in the lab after the due date of the homework.

Late Policy: Labs, Quizzes, Homework and Exams must be taken as scheduled in order to receive credit. Late homework will not be accepted unless its lateness is due to circumstances beyond your control. To receive full credit, the lab reports must be turned in to the Graduate Teaching Assistant in the lab on the date due. Late lab reports will be accepted, but points will be deducted from the score.

Lab Assignments: Laboratory assignments are a very important component of this course. You will learn to design and develop digital logic circuits, and by the end of the semester will be able to design sophisticated digital circuits. We use a set of digital tools used by professional

engineers, which may appear a bit intimidating at first. After the first two to three labs, you will become comfortable with the tools and will be on your way to designing some interesting circuits.

Conduct and Nature of Exams: You will be allowed to use one double-sided page of notes, prepared by you, for the four exams. Exams will be straightforward, but will demand the kind of preparation only possible through continual, daily study.

Instructional Objectives: Given during class, these are the bases of all quiz and exam questions, and homework assignments. For this reason, consistent class attendance is very important.

Textbook and References: Fundamentals of Logic Design, by Charles H. Roth. The latest is the 7th Edition. However, fourth to sixth editions are also acceptable. Be aware that there are differences in chapter, page and problem numbers of the different editions. An electronic version of the text is available at coursesmart.com.

Tutoring: The course's Graduate Teaching Assistants will be available for drop-in consultation as well as help sessions at times and places listed on the website.

Topics:

Introduction to digital systems and number systems	Chapter 1
Boolean Algebra	Chapter 2
Algebraic simplification	Chapter 3
Minterm and maxterm expansions	Chapter 4
Karnaugh maps	Chapter 5
Multi-level gate networks	Chapter 7
Combinational network design	Chapter 8
Multiplexers, decoders and PLD's	Chapter 9
Latches and flip-flops	Chapter 11
Counters and sequential networks	Chapter 12
Analysis of synchronous sequential networks	Chapter 13
State graphs and tables	Chapter 14
Reduction of state tables/state assignment	Chapter 15
Sequential network design	Chapter 16

Academic Integrity: This course will adhere to the CSU Academic Integrity Policy as found in the General Catalog (https://resolutioncenter.colostate.edu/conduct-services/academic-integrity/) and the Student Conduct Code (https://resolutioncenter.colostate.edu/wpcontent/uploads/sites/32/2018/08/Student-Conduct-Code-v2018.pdf). At a minimum, violations will result in a grading penalty in this course and a report to the Office of Conflict Resolution and Student Conduct Services.

Inclusivity: ECE102 classroom is a place where you will be treated with respect. We welcome individuals of all ages, backgrounds, beliefs, ethnicities, genders, gender identities, gender expressions, national origins, religious affiliations, sexual orientations, ability – and other visible and nonvisible differences. All members of this class are expected to contribute to a respectful, welcoming and inclusive environment for every other member of the class.