

Contact is Jason Gentry: Jason.gentry@avagotech.com

VLSI Design Engineer

External Job Description

Member of a high powered World wide team responsible for designing high-

performance VLSI ASIC's for Storage, Networking, and Computing applications. Works closely with fellow team members to create high performance, high quality ASIC's working from specification, RTL, design, characterization, and release to production.

Responsible for all phases of development from specification through design, characterization and release to production. Specific duties could include, but are not limited to, writing RTL, Floor-planning, Physical design, timing convergence, simulation, verification, documentation, place and route, test vector generation, debug, and release to production of such devices in 130nm, 90nm, and 65nm process technologies. Duties could also include interfacing with Avago's internal and external partners/customers providing technical information and understanding integration requirements.

Strong command VSLI Physical design techniques are important to success in this position.

Committed to team success, customer satisfaction, first time right quality, and ease of use is also important.

External Qualifications:

- Bachelor's degree EE or CE
- 3-5 years relevant industry experience
- Experience with VSLI design techniques
- Proficiency with IC physical designs, tools, and flows from Synopsys and

Cadence

- Strong communication and teamwork skills

External Job Description :

PACKAGING ENGINEER

Avago Technologies is seeking a strong and versatile Packaging Engineer to be a major contributor to ASIC package design. The applicant would become a member of a high powered world wide team responsible for designing custom Enterprise ASIC packages. A primary focus is on high-speed / high density digital and SerDes signal routing in multi-layer organic laminate and ceramic technologies.

Responsibilities:

- Work closely with many different worldwide design teams to integrate package design into a total solution
 - o Multiple internal and external ASIC design teams
 - o Signal integrity design teams
 - o Thermal, reliability and qualification design teams
 - o Test characterization teams
 - o Package suppliers
 - o Assembly houses
- Point contact for customer communication on packaging
 - o Available to attend regular customer meetings
 - o Deliver SI models and layout database to customer
 - o Compile and deliver various documents from partners and vendors to customer
- Point contact for the layout of packaging
 - o Document, explain, and check design requirements
- Managing multiple independent projects on different schedules
- Effective communication in conversations, presentations and written documents

External Qualifications :

Qualifications:

BS or MS in computer or electrical engineering with strong theoretical knowledge and minimum of 5 years in one or more of the following areas:

- IC package design (Package technology, assembly is a plus)
- PCB Design Engineer (motivated to learn package design)
- Signal integrity for high speed digital applications
- Power integrity and delivery
- Microwave theory and/or Electromagnetic transmission line theory

Tools:

Knowledge in the following tools is suggested

Cadence Layout tools (APD)-
Windows and Linux-
- Microsoft office (open office)
SKILL and perl-
2-D simulators-
- Ansoft TPA/HFSS/SIWave
Agilent ADS-
Flomerics-Flotherm-

Published Job Title :

Mixed Signal Designer

External Job Description :

Avago Technologies, a leading supplier of ASIC embedded gigabit SERDES (PHY) ranging in operation from 1Gbps to beyond 17Gbps, is looking for a qualified individual to join the SERDES team.

The candidate will be joining a global, high powered mixed-signal design team responsible for state of the art Gigahertz SerDes design, signal integrity modeling, and electrical characterization. Avago Technologies

state of the art SerDes supports networking, storage, and computing applications covering 3Gbps to >17.0Gbps data rates.

Each designer is responsible for the functionality and quality of their designs and insuring that they work correctly in the overall system.

The candidate should have expertise in some of the following areas:

1. Very high speed custom digital design
2. Very high speed analog design
3. Digital communication theory
4. SerDes architectures

Committed to team success, customer satisfaction, first time right quality, and ease of use is also important.

Specific duties could include, but are not limited to, designing

complex,

high performance custom & semi-custom mixed-signal circuits, modeling (verilog), simulation (verilog, spice, and mixed-mode), validation, optimization, documentation, layout and debug of such devices in 90nm, 65nm, and 40nm process technologies. Duties could also include interfacing with Avago Technologies' internal and external partners/customers providing technical information and understanding integration requirements.

Become a member of Avago Technologies' SerDes team, and join the world leader in embedded SerDes solutions.

External Qualifications :

- Bachelor's degree EE or CE
- 3-5 years relevant industry experience
- Experience with high performance FET-level analog or mixed-signal design.
- Experience with IC physical mixed-signal design tools and flows
- Strong communication and teamwork skills
- Must have legal authorization to work in the US

Preferred:

- Master's degree in EE or CE
- 5-8 years relevant industry experience
- Experience with state of the art CMOS SerDes design techniques, circuits

and approaches

- Familiarity with overall chip design methodologies and tools