Smart Pixels Using the Light Amplifying Optical Switch (LAOS)

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Abstract—The light amplifying optical switch (LAOS) is a vertically integrated heterojunction phototransistor (HPT) and light emitting diode (LED) which has latching thyristor type current–voltage characteristics. Since the HPT is designed to have high optical gain, it can be incorporated in a circuit with the LAOS to fabricate high performance optical logic gates such as a NOR, NAND, AND, or a gated latch. This paper describes methods of implementing these gates, reports experimental results for large mesa devices, and analyzes the performance of the gates. Logic gates that utilize either one or two wavelengths of input light are demonstrated. The present logic gates are shown to have output contrast ratios from 4 to 30 and operate at frequencies up to 300 kHz. Increasing this performance by improving processing techniques and reducing mesa size is discussed.

I. INTRODUCTION

PARALLEL digital processing of images or two dimensional data sets requires pixels that can perform a logical function such as inversion, AND, NOR, etc. It is desirable that these “smart pixels” be small, fast, cascadable, energy efficient and have the potential for compact, rugged packaging. It is also desirable that the pixels not require a narrow linewidth laser. In order to develop such a pixel, we have investigated an optically latching device that we call the light amplifying optical switch (LAOS). This paper demonstrates that the LAOS can be configured to perform many optical logic functions at moderately high frequencies. The LAOS has previously been shown to respond to a broad spectrum of input light [1] and can be fabricated with small mesa structures that can be densely packed [2].

The light amplifying optical switch (LAOS) is composed of a heterojunction phototransistor (HPT) vertically integrated with a light emitting diode (LED). The structure and simplified equivalent circuit of the device are shown in Fig. 1. It has been shown [1] that for small applied voltages, the current–voltage characteristics of the LAOS are very similar to those of the series connected HPT and LED, i.e., they resemble HPT characteristics shifted by the voltage drop across the LED [1]. For large applied voltage, the electrical and optical feedback from the LED to the HPT, coupled with the nonlinearities of the HPT, cause the LAOS to switch from a low-current OFF state to a high current ON state via a region of negative differential resistance. These thyristor-type characteristics are similar to those of a pnpn switch [3], [4] or DOES device [5], [6]. The first devices of the LAOS type were reported by Beneking [7] and Sasaki [8] in 1981. Since that time, several other research groups have reported results from devices with this same general configuration using either the GaAs–AlGaAs or InGaAsP–InP materials systems [2], [9]–[11]. Some of these devices replaced the LED with a laser diode [9], [11].

The LAOS is an optical detector-regenerator type of device as opposed to a detector-modulator device such as the SEED [12] or EARS [13]. And, since the LAOS uses an HPT as the detector, it has a broad spectral response and does not require a highly wavelength stable laser input as required by the modulator type devices. There is also no need for strict temperature control or single-mode polarized input light. In addition, the LAOS structure provides a high gain phototransistor on the chip which makes the realization of optical logic relatively easy and straightforward, as we will show later. The LAOS can switch at relatively high speed (<10 ns) [2] although it does not have the high pass through bandwidth of the modulator type devices. Thus, the LAOS type device has many advantages for smart pixel computing and image processing applications but is best suited for applications which require fast switching (i.e., high frame rates) and easily implemented logic functions. This paper examines optical NOR, NAND, and AND gates, as well as a gated latch, all implemented with the LAOS. Logic gates which uses

Fig. 1. Structure and equivalent circuit of a LAOS device.
either one wavelength of light for the two inputs or two different wavelengths are demonstrated.

II. OPTICAL LOGIC WITH THE LAOS

The LAOS can be switched on by biasing the device near the critical voltage and then applying a short pulse of light that momentarily increases the photocurrent above the critical current. When the optical pulse is removed, the LAOS remains in this on condition [1]. In order to turn the LAOS off, we have incorporated additional light sensitive circuitry which can be configured to perform a variety of logic functions. All of the logic functions are performed optically without changing the electrical bias level, as is often required when a pn-pn switch is employed [3], [4]. When the LAOS is in the on state, the LED current and light output is high. In the off state the LED current is low and there is very little output light.

Two-dimensional (2-D) arrays of the logic gates discussed here can be used in image processing systems, e.g., an AND gate array can operate as a spatial light modulator and the NOR gate can be used as part of an image or data comparator system [14]. Integrating the LAOS gates into arrays appears to be straightforward and indeed our preliminary fabrication work has not uncovered any unforeseen problems. At present we believe that there are no inherent reasons that large arrays cannot be successfully fabricated. Problems that may arise with the LAOS arrays relate to optical interaction between pixels and uniformity across the array. We have found that there is very little pixel to pixel interaction for larger mesa which are separated by 120 μm. Work is under way to determine if optical cross talk problems will arise at smaller separation. Uniformity of device characteristics has not been a problem for the present size die of 3 × 3 mm. Larger size die should not be a problem since HPT and LAOS characteristics are not strongly dependent upon layer thickness and doping. Fabricating arrays will require additional processing, e.g., some of the logic gates require an integrated resistor for each pixel and we are planning to use electron beam deposited NiCr thin film resistors. The LAOS logic arrays should be quite versatile since the same or different types of logic gate can be produced at each pixel location by simply changing the metallization mask interconnect pattern. This is much simpler than some other types of optical logic gates which require electrical pulses [4].

A. Inverter and NOR Gate

The basic building block of a logic set is the inverter. A technique for implementing an optical inverter and NOR gate using the LAOS is illustrated in Fig. 2 [10]. Optical inversion is achieved by electrically biasing the LAOS device into the on state and then turning it off with an input light signal to the parallel connected HPT. Applying a light input to the HPT increases the current through the load resistor and decreases the voltage drop across the LAOS. When the input to the HPT is large enough, the LAOS voltage drops below the holding voltage $V_H$ (see Fig. 4) and the LAOS turns off. The NOR operation is accomplished by providing the inverter with multiple inputs. Fig. 3 shows the input-output oscilloscope traces of a two-input NOR gate fabricated with layers of InP and InGaAs grown by gas source molecular beam epitaxy [15]. The light from two synchronously driven 1.3 μm lasers was applied through optical fibers to the A and B HPT mesas. Note that the output is low when both A or B is high and that the output is high only when both A and B are low. Thus, the NOR function is realized. Note also that the bias voltage is held constant and does not need to be pulsed in order to cause the NOR gate to function.

The input-output characteristics of the optical NOR gate can be explained by examining the current-voltage curve of the LAOS with a superimposed resistive load line and the characteristics of the parallel connected phototransistor. Fig. 4(a) plots the LAOS $I$-$V$ curve along with the loadline for a fixed load resistor of value $R$. The equation for the load line is given by

$$V_L = V_{bias} - R(I_L + I_{HPT})$$

(1)

where $I_L$ and $V_L$ correspond to the LAOS current and voltage, respectively, and $I_{HPT}$ is the current through the HPT. The load line intersects the LAOS curve at point A; this is the only stable operating point for zero input into the HPT. The light output from the LAOS is proportional to the current defined by point A. This zero input current can be increased by either reducing the load resistance or by increasing the bias voltage.

Fig. 4(b) superimposes the HPT characteristics on the LAOS-resistor curve of Fig. 4(a). The HPT curves fit on the zero input load line to form a variable load that depends on the optical input to the HPT. For simplicity, it is assumed that the phototransistor has linear gain and no early effect or avalanching. The operating points of the nor gate circuit are the intersection points of the LAOS characteristic curves and the family of curves associated with increasing optical input power to the HPT [points A–F on Fig. 4(b)]. It can be seen that the operating point moves down the on region of the LAOS $I$-$V$ characteristics as the optical input power is increased [points A–C on Fig. 4(b)]. When the input power reaches the threshold power $P_{th}$ the operating point is at the holding voltage.
$V_H$ and $I_L = I_H$, the value of the input power required to switch the LAOS from the on state to the off state is given by

$$P_{th} = \frac{1}{G_{opt}} \left( \frac{V_{bias} - V_H}{R} - I_H \right) \quad (3)$$

Fig. 5 shows how the minimum required input power varies with the value of the load resistance with the applied bias voltage and optical gain as parameters. From these curves it is seen that $R$ must be in the range 250–750 $\Omega$ in order that $P_{th} < 100 \mu W$. The magnitude of $P_{th}$ will decrease with the mesa area.

The output on–off contrast ratio can also be determined from Fig. 4(b) since point A sets the maximum output and the leakage current, e.g., point E, sets the minimum output. For low leakage devices, the contrast ratio can be large. For the $\text{NOR}$ gates presented here, the low frequency contrast ratio is about 30. Measurements at higher frequencies show that the contrast ratio remains constant up to 300 kHz. Above this frequency the output waveform becomes distorted and the contrast ratio begins to drop rapidly. Fig. 6 shows that the output fall time is much faster than the rise time and that the rise time has two or three different "time constants." Our measurements indicate that the fall time is limited by the turn on time of the HPT and the test setup. The complex rise time is thought to be caused by the highly nonlinear dynamic resistance of the LAOS device and nonlinearities of the junction capacitances; however, the physics/equivalent circuit are not understood at this time. However, since RC time constants are involved, the maximum operating frequency should scale with the area of the junction until the recombination lifetime (approximately 1 ns) in the HPT base and the active region of the LED dominates the transient response. Thus, reducing the mesa area from the present (250 $\mu m)^2$ to (20 $\mu m)^2$ should increase the maximum operating frequency to about 50 MHz, i.e., a total rise and fall time of 20 ns. This corresponds closely to the 10 ns response time reported by Matsuda et al. [2] for a set–reset memory cell that was fabricated with (20 $\mu m)^2$ LAOS type devices. Thus, the linear scaling of the transient response with mesa area, appears to hold and high frequency operation of the $\text{NOR}$ gate should be realizable. However, this simple analysis assumes that the load resistance remains constant. In practice the value of the load resistance is chosen as a compromise between the required output light, the allowable electrical power dissipation and the optimum input optical power. Thus, the operating frequency is also a function of these parameters and simple scaling may not hold.

B. And Gate and Gated Latch

The $\text{NOR}$ gate, discussed above, is an example of a LAOS optical logic gate that uses the same wavelength of light for each of the two inputs. We have also demonstrated two wavelength smart pixel devices using the LAOS [16], [17]. This type of device is composed of an HPT vertically integrated on top of the LAOS as shown
Fig. 5. Minimum input optical power to the HPT required to turn the LAOS off as a function of load resistance for different values of bias voltage and optical gain. $I_H = 2.5$ mA, $V_H = 1.75$ V.

Fig. 6. High frequency output wave shape of an optical NOR gate.

in Fig. 7. The base collector layers of this HPT and the LAOS device are fabricated with different InGaAsP compositions and therefore they respond to different wavelengths of input light. Only a single mesa is required for this device structure and thus higher packing density than with the three mesa NOR gate can be achieved. In addition, the two input signals are both focused on the same spot on the pixel, thereby reducing the alignment problems. This integrated 2λ device can function either as an optical AND gate or an optically controlled latch; the function depends upon the applied bias.

Proper operation of the 2λ device requires that most of the light of wavelength $\lambda_1$ must be absorbed in the base-collector region of the top HPT, as indicated in Fig. 7, since the $\lambda_1$ light that penetrates into the LAOS could latch the device into the ON state if the $\lambda_1$ light leakage exceeds the switching threshold of the LAOS. On the other hand, the top HPT must be transparent to the $\lambda_2$ input light since it is used to switch the LAOS. This optical isolation is accomplished by fabricating the base collector regions of the two HPT’s from materials of different bandgaps. For our devices, the composition of the base collector layers corresponds to a band-gap emission wavelength of 1.15 $\mu$m and 1.7 $\mu$m for the HPT and LAOS, respectively. These single mesa devices were formed by chemically etching the molecular beam epitaxially grown layers and depositing gold contacts on the top and bottom layers of the mesa. The devices were tested by applying a dc bias to the contacts and directing light from 0.83 $\mu$m ($\lambda_2$) and 1.3 $\mu$m ($\lambda_3$) lasers through optical fibers to the top of the mesa. The lasers were driven with square waves at different frequencies in order to observe the output with different input combinations. Oscilloscope traces, proportional to the input and output signals for the AND gate and the gated latch, are shown in Fig. 8. Note that the output of the AND gate, Fig. 8(a), is high only when both the 0.83 $\mu$m and the 1.3 $\mu$m are high and thus, the AND function is realized. The output of the gated latch is also switched to the high state when both of the laser inputs are high, however the output only returns to the low state when the 0.83 $\mu$m laser turns off, independent of the state of the 1.3 $\mu$m laser input. This type of functionality can be used to synchronize an array of gates or to act as an optical pass transistor.

The operation and contrast ratio of the AND gate and gated latch can be analyzed with the aid of the current-voltage curves of Fig. 9 which are similar to the NOR gate $I-V$ curves of Fig. 4, except the HPT is now in series with the LAOS and there is no load resistor. In fact, the HPT serves as an optically controlled nonlinear resistor which controls the current, eliminating the need for a fixed load resistor. In the NOR gate circuit, the input HPT optically controls the voltage across the LAOS and the load resistor is needed to limit the current and drop part of the bias voltage.

As shown in both Fig. 9(a) and (b) the LAOS has three different $I-V$ curves representing the three operating conditions of the vertically integrated 2λ device. These illustrate the LAOS $I-V$ characteristics with, 1) no input light, 2) a small amount of input light, i.e., a small amount of unwanted $\lambda_1$ penetrating down to the LAOS device, and 3) a large amount of $\lambda_2$ input.

The light output of the 2λ logic device is proportional to the LAOS current which is controlled by the top HPT to be at one of four stable operating points A–D. These points are shown both in Figs. 8 and 9. Note the contrast ratio is determined by the maximum output, point D, and the minimum output, point C or A. Point A is determined by the current leakage of the LAOS and point C is determined by the light leakage of $\lambda_1$ (0.83 $\mu$m) into the LAOS. For the data shown in Fig. 8, the contrast ratio of the AND gate is about 4 and the gated latch is about 12. Note that, for the gated latch, point D is above the holding current $I_H$, and for the AND gate it is below $I_H$. 
C. NAND Gate

The same three mesa structures used to fabricate the NOR gate can also be used to implement a two input NAND gate. This is accomplished by connecting the two HPT’s in series instead of in parallel as shown in Fig. 10(a). This type of arrangement requires the same input intensity as the NOR gate since this will yield the same current through the parallel connect circuit. Another approach to implementing the NAND gate is shown in Fig. 10(b) in which the A and B inputs are of subthreshold intensity. While this technique lowers the required light input intensity it also sets strict limits on the intensity and thus makes the device more difficult to incorporate into a system.

Still another technique for implementing the NAND gate uses the 2λ structure of the AND gate and the equivalent circuit of Fig. 10(a). Now a single input mesa replaces the two HPT mesas of the first approach discussed here, and each input is of different wavelengths.

III. DISCUSSION AND SUMMARY

The LAOS has been shown to be a versatile device that can be easily configured to perform optical logic. This is, in large part, due to the fact that the HPT and LED are designed as separate components. Thus, the HPT is designed to have high optical gain and can be effectively used as a parallel or series connected nonlatching optically sensitive circuit component. The LED can be designed for maximum surface emission [18] and has a spectral output independent of the responsivity of the

HPT. Previous analysis [1] shows that optical and electrical feedback from the LED to the HPT coupled with the nonlinearities of the HPT, cause the thyristor type switching of the LAOS. Therefore the coupling between the two components must be considered in the LAOS design.

Several different logic gates using the LAOS have been demonstrated as examples. Other gates and combinations of gates can also be implemented by changing the metallization and etch masks. We expect to demonstrate more complex logic pixels in the near future.

For the present LAOS devices, an LED is used as the output device, however, a laser diode or VCSEL could also be used. The use of a laser greatly increases the optical output and has a narrower divergence beam angle. Unfortunately, a laser requires significantly more difficult epitaxial growth and wafer processing. The lasers also have relatively high threshold currents which increases the power dissipation per pixel which could limit the pixel
density. Our simplified calculations [19] indicate that an LED can provide sufficient light output, with acceptable optical cross talk, if micro lenses are used along with an optical coupling medium and high gain HPT's. Our present research is directed toward experimentally demonstrating that LED's can be used to cascade two LAOS arrays, however we are also considering VCSEL's.

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REFERENCES


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