Optoelectronic Exclusive-OR Using Hybrid Integration of Phototransistors and Vertical Cavity Surface Emitting Lasers

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Abstract—Heterojunction phototransistors and surface-emitting lasers were used to demonstrate two new optoelectronic circuits that implement the exclusive-OR (XOR) function. One of the circuits also determines which of the two inputs is greater than the other. The XOR gates have high ON/OFF contrast ratios (i.e., > 28:1) and optical gate gain $\approx 3$.

I. INTRODUCTION

THE DEVELOPMENT of vertical cavity surface-emitting lasers (VCSEL's) is advancing rapidly, and many applications, such as laser printing, free space interconnects, and optical computing are envisioned [1]. Incorporating the VCSEL's into smart pixel arrays will increase the applicability of these lasers even further and accelerate the development of optical processing and computing systems.

This letter presents experimental demonstration of two exclusive-OR (XOR) optoelectronic circuits that use VCSEL's as the output devices and heterojunction phototransistors (HPT's) as input detectors. One of the circuits realizes the XOR function $Q = A\overline{B} + \overline{A}B$ using only one VCSEL. The other circuit uses two VCSEL's, but in addition to the XOR function, the circuit also determines if $A$ is greater than $B$. This later function is essential in many sorting and data-filtering systems and thus increases the usefulness of this circuit [2]. The differences between the operating characteristics and device requirements for the two circuits are discussed.

II. XOR GATE CIRCUITS

Recently, we demonstrated an optoelectronic XOR gate fabricated with HPT's and an HPT-LED combination [3] that we call the light-amplifying optical switch (LAOS) [4]. The current-voltage characteristics of the LAOS exhibit an S-shaped nonlinearity that provides well-defined ON and OFF states. This leads to a high ON/OFF contrast ratio (> 50) for the XOR gate. The XOR circuits of the present paper use the nonlinearity in the current-light characteristics of a VCSEL introduced by the lasing threshold.

Previously, Cheng et al. [5] reported implementing the XOR function by the hybrid integration of two VCSEL's and two HPT's in a balanced push-pull-type circuit. For this circuit to operate properly, the gain and leakage currents of the two HPT's had to be closely matched in order to prevent an unbalanced circuit. No such matching is required for the XOR circuits presented here.

Fig. 1 illustrates the two HPT-VCSEL XOR circuits. The XOR gate of Fig. 1(a) can be viewed as two circuits, each composed of two HPT's and one VCSEL. The HPT's (M2 or M3) are arranged such that one is connected in parallel with the VCSEL (V1 or V2) and the other HPT (M1 or M4) is serially connected to the parallel VCSEL-HPT combination. This circuit is similar to the HPT-VCSEL NOR gate presented by Lee et al., [6] except that the resistor is replaced by an HPT (M1 or M4) that is used to optically enable the circuit. When the input to HPT M1 is ON, a current is allowed to flow into the VCSEL V1-HPT M2 combination. If the input to HPT M2 is OFF, then the current provided by HPT M1 flows through VCSEL V1. When sufficient input optical power is incident on HPT M1, the current provided to VCSEL V1 is greater than the lasing threshold current, and an optical output signal is generated. If the input to HPT M2 is also ON, then a portion of the current provided by HPT M1 is shunted. With sufficient input to HPT M2, the current through VCSEL V1 can be reduced to below the lasing threshold and the output signal turns OFF. Thus, the output of VCSEL V1 is analogous to the output of an inhibition gate (i.e., the output is equal to $\overline{A}\overline{B}$). Since the inputs are reversed on the second half of the XOR gate, the output of VCSEL V2 is equivalent to $\overline{A}\overline{B}$. To realize an XOR function, each of the VCSEL outputs must be directed onto a single detector as in the present demonstration. This is equivalent to a "wired OR" of the two optical outputs. If each of the VCSEL outputs is detected separately, then this circuit determines which of the two input signals is larger. The first VCSEL produces an optical output only when $A > B$, whereas the second VCSEL produces an output only when $B > A$.

For systems applications requiring only the XOR functionality (as in the case of binary addition) [6], then an
XOR gate with a single VCSEL is preferred, because the detector can be smaller. The second XOR circuit presented in this paper, Fig. 1(b), realizes such a single VCSEL XOR. Four HPT’s are again used as inputs. Two of the input HPT’s (Q1 and Q2) are connected in parallel and placed in series with the VCSEL. The other two HPT’s (Q3 and Q4) are connected in series and then placed in parallel with the VCSEL. The operation of this XOR gate is similar to the operation of the inhibition circuit described above. When one of the two input signals is ON and the other is OFF, current will flow through the VCSEL, and there is an optical output. When both of the input signals are ON, the current provided to the VCSEL is shunted through HPT’s Q3 and Q4. This drops the VCSEL current below the laser threshold, and there is no optical output. When both inputs A and B are OFF, no current flows through the circuit, and again there is no optical output.

III. RESULTS AND DISCUSSION

In order to test the functionality of the XOR gates, the HPT’s and VCSEL’s were mounted in DIP packages. The XOR gates were then created by electrically connecting the HPT’s and VCSEL’s on a breadboard. The optical inputs were generated with two pigtailed 830 nm semiconducting lasers driven with offset square waves of the same frequency. The light from each input fiber was simultaneously directed onto two adjacent HPT’s. The HPT’s used in this demonstration were fabricated from InGaP/GaAs layers grown by gas source molecular beam epitaxy (MBE) as described previously [7]. The VCSEL were MBE-grown with AlGaAs superlattice mirrors and were operated at a wavelength of 980 nm. The operation of the circuits is independent of the output wavelength, however.

Fig. 2(a) shows a timing diagram for the first XOR gate. The input waveforms are those of the function generator signals used to drive the 830 nm semiconducting lasers. The output waveform was measured by directing both VCSEL output signals onto a single, broad-area silicon photodiode. Fig. 2(b) shows the timing diagram for the second XOR gate. It is seen for both circuits that the output is “1” only when one of the inputs is ON and the other is OFF. Thus, the XOR functionality is realized.

The ON/OFF contrast ratio (CR) was found for these XOR gates by taking the minimum ON value divided by the maximum OFF value in the output waveform. The first circuit has a CR of 35:1, and the second circuit has a CR of 28:1.

As described above, proper operation of the XOR gates depends on shunting a portion of the VCSEL current. When only one input is ON, the current provided by the corresponding input HPT (I_{HPT}) must be greater than the threshold current of the VCSEL (I_t). For the first circuit, Fig. 1(a), each VCSEL has one HPT (M1 or M4) in series and one HPT (M2 or M3) in parallel. Thus, for HPT M2 to turn off VCSEL V1, it must shunt a current greater than I_{HPT} - I_t. Since the VCSEL’s are operated slightly above threshold, the current shunted through HPT M2 is a fraction of the current provided by HPT M1. Thus, variation in input power or HPT gain is not critical to the circuit operation. This leads to an XOR gate that can easily be integrated into arrays of smart pixels suitable for optical computing and processing applications.

For the second circuit, each of the HPT’s connected in series (Q1 and Q2) with the VCSEL produces a current I_{HPT} > I_t. Thus, when both inputs are ON, a current I = 2I_{HPT} is provided to the VCSEL. In order to turn the VCSEL OFF, a current greater than 2I_{HPT} - I_t must be shunted. This requires HPT’s Q3 and Q4 to conduct more current than either HPT Q1 or Q2 provides. Thus, the HPT’s Q3 and Q4 must have either a larger input power.
or larger gain than HPT's Q1 and Q2. This is most easily achieved by scaling the size of the input windows for the HPT's such that the series HPT's have a smaller input power than the parallel HPT's. By designing the HPT input power characteristics in this way, it is also possible to overcome the sensitivity to gain and input power variation and thus yield a gate suitable for array applications.

The input power versus output power characteristics of the XOR circuits are plotted in Fig. 3. Since the maximum output power from either XOR gate is limited by the series HPT's (Fig. 1) driving the VCSEL, the circuit shown in the inset could be used to generate these input-output characteristics. Fig. 3 indicates that the VCSEL's used in our demonstration begin producing significant optical output at approximately $P_{in} = 350 \mu W$. At $P_{in} = 825 \mu W$, the HPT saturates, holding the VCSEL current (and output power) constant for input powers above this value. For input powers between 400 $\mu W$ and 800 $\mu W$, the output power generated by the VCSEL is greater than the input power, indicating that the XOR gates exhibit gain in this region. For the present components, the output power-input power ratio yields a maximum gate gain of approximately 3. Applying an antireflection coating to these same components should increase the maximum gate gain to approximately 4.

IV. SUMMARY

Two new optoelectronic XOR gates circuits based on the hybrid integration of HPT's and VCSEL's have been demonstrated with contrast ratios of 28.1 and 35.1 and optical gains of 3. By controlling the size of the HPT input windows, it is possible to control the operating characteristics of the XOR gates. This minimizes the changes in gate performance due to variations in input power and HPT gain. Thus, both circuits are suitable for monolithic integration into two-dimensional arrays.

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REFERENCES