

A Neural Network based Approach for Testing Analog Circuits with Frequency Domain Classification and Time Domain Testing

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Abstract

A new analog circuit testing technique based on neural networks is proposed. It is based on utilizing the domain knowledge in order to design a training set for a neural network which characterizes the circuit's response under faulty and fault free conditions. The training set is a general set representation of the entire response space of the circuit under both the faulty and fault free conditions. The results show that the neural network approach is capable of detecting response variation due to acceptable parameter variations from that due to faults. Effectiveness of the approach in detecting hard faults (shorts and opens) and soft faults (out-of-specification) for both single and multiple faults are presented.

Introduction

Despite the many recent advances in design of analog and mixed signal integrated circuits, testing of these circuits remains a major problem. This is mainly because there is limited access to the internal nodes, the outputs are mostly non-linear, include noise and are affected by variations in the component values. The statistical distribution of faults in analog circuits is also not known with enough precision. The usual method used for testing is functional testing where the specifications of the circuit are tested. An analog circuit is faulty if any of the specifications are not satisfied. A fault in an analog circuit is any change in the value of an element with respect to its nominal value outside the tolerance limits that causes the failure of the circuit. The effective method to detect faults is to select an input stimulus that will propagate the error to the output and produce different responses for a faulty and fault free circuit. This paper proposes a new method for testing analog circuits using artificial neural networks.

Artificial neural networks have been put to use in a wide range of applications in analog circuit parameter

estimation and also for fault diagnosis and isolation of faulty components [5], [3]. In testing of circuits it has been applied for testing of small analog circuits taking into consideration the nodal voltages, etc [1-4].

Analog circuit testing was done by checking the functionality of the individual components in a circuit [9], which requires the access to the internal components or additional built-in circuitry for testing. Testing with limited nodal access has been addressed in [12]. Testing of analog circuits has also been done by monitoring the power supply current and it has also been done using the fussy logic paradigm named FLAMES [7].

A neural network based technique for analog testing is proposed and evaluated with several analog filter circuits. The learning capability of the neural network along with its capability to generalize based on small sets for the entire space is used for the purpose of testing analog circuits. An artificial neural network is trained with a small training set which is a general representation of the entire response space of the circuit. The training inputs corresponding to the fault free circuit include effects due to component tolerances within specified limits. The training inputs for faulty circuit are obtained by injecting hard and soft faults to the circuit. The selection of an input pattern(s) that captures as much of system response characteristics is critical for keeping the neural network complexity low. In case of a biquadratic filter for example, a saturated ramp or continuous pulse input can capture the circuit characteristics very effectively. Also the input is so chosen that there is maximum deviation between the nominal response and the faulty response. This ensures minimum overlap of the faulty and fault free responses. Generating training patterns for faulty circuits is challenging as the sensitivity of circuit characteristics to different components can widely differ. Thus, even when a certain component is outside the tolerance

level of the manufacturing process, its impact on the circuit characteristic may be negligible. On the other hand, the circuit response to another component may be so sensitive, that manufacturing tolerances impose a strict bound on the acceptable circuit behavior. We will discuss these issues in detail using two analog filters as examples. The proposed technique uses frequency domain information to classify the test patterns into fault and fault free responses, but the training of the neural network and testing uses time domain waveforms. The approach was evaluated by testing for a large number of single and multiple faults that are not related to the training set. The classification is done automatically in real time. The proposed approach can effectively distinguish between the variation of the system response due to component variation within acceptable manufacturing tolerances and that due to faulty components that cause system response to lie outside the design specifications.

The flexibility of this method is demonstrated by the fault detection achieved with different filters and also with different input stimuli. Only the input-output or the power supply pins are needed. This accounts for the simplicity, as there is only limited access to the internal nodes in case of integrated circuits. Complex analog circuits can be divided into different macro blocks like filters, DAC, ADC, oscillators, phase locked loops and a testing method for each of these macro models can be formed. In this paper a testing strategy for testing filters is proposed and also the results obtained for a biquadratic filter [Figure 1], and a 1KHz narrow bandpass filter are included.

Training set design

The selection of the features for testing analog circuit is of great importance. These are the inputs-outputs specified to the neural network. In the case of a bandpass filter a sampled pulse response is the input to the neural network. For a biquadratic filter the sampled pulse response or the sampled response for a saturated ramp input will be considered as the input to the neural network. The two-bit output (target) of the neural network is either 10 or 01 depending on whether the circuit is faulty or fault free. The data for the training and testing set is collected from the PSpice simulator and the transient response of the circuit is used for this purpose. The frequency responses of the circuits are used for classification. The Monte Carlo approach is used to generate responses with changes in the component values. Using this method, responses that include multiple faults can be generated easily. Also various single

and double faults are induced in the circuit and their transient response is obtained.

Classification of faulty and fault free circuits

Classification is done using the frequency response. Variations in the component values affect the peak amplitude or central frequency of the filter. So the two parameters taken into consideration for the classification are the peak amplitude and the shift in the central frequency. The tolerance for the amplitude and central frequency shift is 10% of the nominal value. The correct circuits are those which have a tolerance within 110% and 90% of the nominal value for both the amplitude shift and the central frequency shift of the frequency response. The faulty circuits are those which have tolerances above 120% or below 80% of the nominal value for both amplitude shift and central frequency shift. Figure 2 shows the frequency response of a biquadratic filter. It also shows the tolerance bands for the peak amplitude and the central frequency. In case of biquadratic filter 100 samples were taken between .5MHz and 1.5MHz. Figure 3 shows the transient responses of the biquadratic filter (saturated ramp input). In the case of biquadratic filter 50 samples are taken from 0 to 4.9microseconds in case of continuous pulse and 50 samples from 0 to 3 microseconds in case of saturated ramp input. The input in case of the biquadratic filter is 1V. The Flow chart in Figure 4 explains the process of neural network training.

A Biquadratic filter

In case of the biquadratic filter the frequency response is first considered. The classification is done based on the frequency response of the filter circuit. The circuit is tested with different types of input stimuli. The continuous pulse is found to be the best input stimuli for the filter. This is well explained in [11]. A continuous pulse and a saturated ramp input is given to the circuit and its response is used for the training of the neural network. The circuit response to saturated ramp is an output that rises gradually and overshoots the DC saturation value and finally settles down at the DC saturation value [6]. The main features of this response are the delay, rise time, DC saturation value and the initial overshoot above the saturation value. The 20% deviation in the component values is considered to compare our results with the results of [6].

In Case of Biquadratic filters two input stimuli are used Continuous Pulse and Saturated Ramp

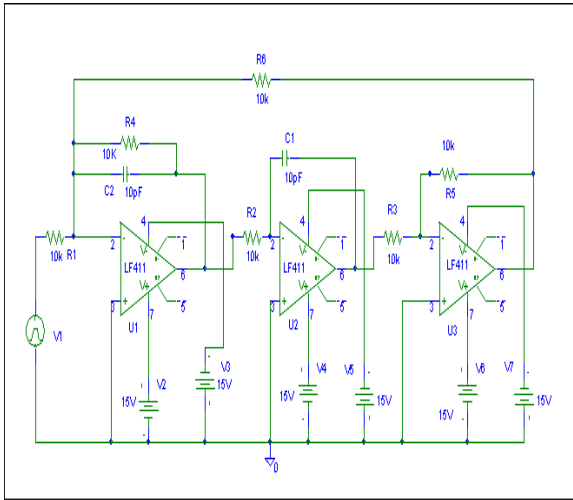


Figure 1. A Biquadratic Filter.

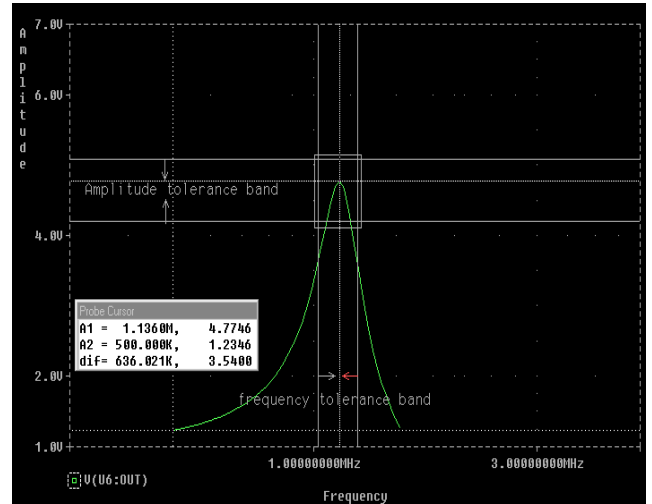


Figure 2. Frequency Response of the Biquadratic Filter

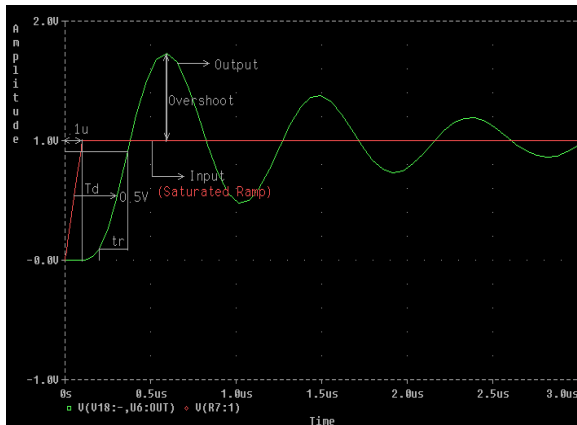


Figure 3. Transient Response of Biquadratic Filer for a Saturated Ramp input.

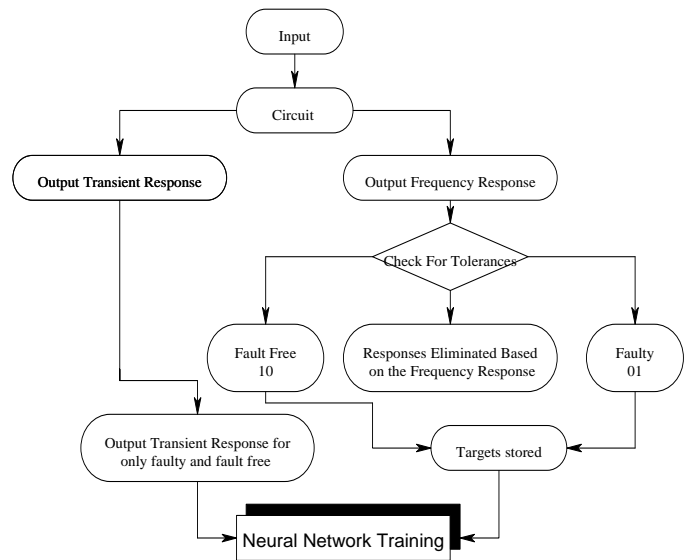


Figure 4. Flow Chart showing the process of Training of the Neural Network.

Continuous Pulse (0V 1V 0 .01u .01u .5u 1u) Testing of the circuit:

Input given to the circuit: 1V Sinusoidal input.
Output from the Circuit: Frequency response for a frequency sweep of .5MHz to 1.5MHz.
Transient Input: 1V rectangular pulse input, rise time=. 01us fall time=. 01us period=1us.
Transient Output: Transient response from 0 to 4.9us.

The input to the Neural Network: Transient response of the circuit.

Output defined to the network under supervised learning: 10-Faultfree, 01-Faulty.

The network is tested with transient responses obtained by inducing single faults to the circuits with 5%, 10%, 50%, and 75% deviations in the component value from the nominal value. The results are then used to determine the fault coverage. Note that majority of the 5% and 10% variations correspond to fault free condition and for the 50% and 75% majority would correspond to faulty circuits.

Training set:

1. Number of fault free transient responses based on the classification (includes tolerance percentages for both peak amplitude and peak frequency) which fall within 10% of the nominal value for 60 simulations: the correct responses : 36 out of 60
2. Number of fault free transient responses based on the classification (includes tolerance percentages for both peak amplitude and peak frequency) which fall above 20% of the nominal value for 60 responses : 56 out of 60
3. Shorts and opens : 16

Testing set:

1. Number of transient output responses used for training set Training set : 108
2. Number of transient output responses with changes in the component values 5%, 10%, 20%, 50%, 75% : 80
3. Correct classification : 170
4. Misclassification : 18

In case of shorts in component, .001 times the nominal value is used and in case of opens, 1000 times the nominal value is used.

In case of saturated ramp input the results showed that the performance of the neural network increased with an increase in the training set. This is shown in table 1.

Table 1 Performance of Neural Network with increase in the Training Set for Biquadratic Filter in case of a Saturated Ramp Input.

Training Set	Evaluation For Training Set (Testing set for Shorts opens and 5%, 10%, 25%, 50%, 80%)	Misclassification
108	96	21
120	96	13
188	96	2

Advantages

The advantages of our method include the fact that no DC node voltages are needed for detecting the shorts and opens in the circuit and also multiple faults can be detected. Also the changes in phase are not considered thus simplifying the process. Only one test-input signal is used. The training of the neural network and the selection of the training set take time and effort but once that is done, the classification is done automatically in real time. In cases where there is less fault coverage it is possible to increase the fault coverage by including the misclassified responses in the training set and retraining the neural network with the new training set as seen from the results shown in Table 1. Main advantage of this type of testing is that the proposed approach can distinguish between parameter variation faults very effectively. It is also effective for detecting multiple faults as well as faults not covered by the training set. The flexibility of this method is demonstrated by the fault detection achieved with different filters and also with different input stimuli.

Conclusions

The percentage fault detection achieved was greater than 90% in most cases. The effectiveness of this method is demonstrated by the excellent fault detection achieved with this method for detecting hard and soft faults for both single and multiple faults for the circuit being tested. The domain knowledge is exploited to describe and also exploit the nonlinear relationship between the input measurement space and the outputs. The training of the network forms a mapping between the inputs and the outputs. Experimental results demonstrate the effectiveness of the proposed approach in terms of testing analog circuits. The misclassifications in the few cases of single faults may be attributed to the fact that they affect the circuit response to a much larger extent or much lower extent than expected. The misclassification for multiple or double faults may be attributed to the fact that changes caused by variations in two or more components may result in characteristics that does not affect the overall response of the circuit. The training set can be formed from responses got from faults that most

commonly occur in a particular circuit and in case of undetected or misclassified faults the neural network can be retrained including the undetected or misclassified faulty response and the new network can be used. This testing process can be extended to fault isolation process where the faulty component can be isolated by the way it affects the output response. This method can also be extended to complex analog circuits which can be divided into different macro blocks such as filters, DAC, ADC, etc and a testing method for each of the macro blocks formed.

Table 2 Single Faults

Circuit (Input)	Training Set	Testing set	Correct Classification	Fault Detection
Bandpass (Pulse)	113	153	151	98.7%
Biquadratic (Pulse)	108	188	170	90.4%
Biquadratic (Saturated Ramp)	108	188	167	88.8%
Biquadratic (Saturated Ramp)	188	188	186	98.9%

Table 3 Double Faults (Same Neural Network is used)

Circuit	Testing Set	Correct Classification	Fault Detection
Bandpass (Pulse)	78	77	98.7%
Biquadratic (Saturated Ramp)	120	109	90.8%

Table 4 Multiple Faults (Same Neural Network is used)

Circuit	Testing Set	Correct Classification	Fault Detection
Bandpass (Pulse)	108	104	96.3%
Biquadratic (Saturated Ramp)	102	2	98%

References

1. Juraj Povazanec, Vladislav Musil and Jiri Kaderka, "Simulation of the Test Process for Analog Integrated Circuits", International Symposium on Circuits and Systems, ISCAS, 1996 pp. 711-714.
2. Juraj Povazanec, Vladislav Musil, Petr Simek and Jiri Kaderka, "Neural Network Based System for Testing and Diagnostics of Analog Integrated Circuits", Proceedings of the International Conference on Electronics, Circuits and Systems", 1996 pp. 1198-1201.
3. Mohamed A.El-Gamal, "A Knowledge-Based Approach For Fault Detection and Isolation in Analog circuits", IEEE Transactions on Neural Networks 1997 pp. 1581-1583
4. A. Materka, "Neural Network Technique For Parametric Testing of Mixed-Signal Circuits", IEEE Electronic Letters 1994.
5. Jingfan Zhang, Junren Gan and Linsheng Yao, " Analog Integrated Circuit Parameter Fault Diagnosis Using Artificial Neural Network", International Conference on ASIC, 1996 pp. 40-43.
6. Ashok Balivada, Jin Chen and Jacob A. Abraham, "Analog Testing With Time Response Parameters", IEEE Design and Test of Computers, 1996 pp. 18-25.
7. Mani Soma, "Challenges in Analog and Mixed-Signal Fault Models", Circuits and Devices, 1996 pp. 16-19.
8. F. Mohamed, M. Marzouki, A. Biassizo and F. Novak, "Testing and Diagnosis of Analog Devices with Flames", IEEE VLSI Test Symposium.
9. Mustapha Slamani and Bozena Kaminska, "Analog Circuit Fault Diagnosis", IEEE Design and Test of Computers, 1992 pp. 30-39.
10. Hong Dai and T. Michael Saunders, "Time-Domain Testing Strategies and Fault Diagnosis for Analog Systems", IEEE Transactions on Instrumentation and Measurement, Vol. 39 No. 1, Feb 1990.
11. Sheng-Jen Tsai, "Test Vector-Generation for Linear analog Devices", ITC 1991, pp. 592-597.
12. Kenneth R. Chin, "Functional Testing of Circuits and SMD Boards with Limited Nodal Access", ITC 1989 pp. 129-1.
13. Chen-Yang Pan and Kwang-Ting Cheng, "Implicit Functional testing for Analog Circuits", 14th VLSI test Symposium pp. 489-495 1996.
14. Arun Palaniswamy, "Analog Circuit Testing Using Neural Networks", M.S. Thesis, Dept. of Electrical and Computer Engineering, Colorado State University, Spring 1998.