Input Pattern Classification for Detection of Stuck-ON and Bridging faults using I_{DDQ} Testing in BiCMOS and CMOS Circuits

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ABSTRACT

Quiescent power supply current monitoring (I_{DDQ}) has been shown to be effective for testing CMOS devices. BiCMOS is emerging as a major technology for high speed, high performance, digital and mixed signal applications. Stuck-ON faults as well as bridging faults in BiCMOS circuits cause enhanced I_{DDQ}. An input pattern classification scheme is presented for detection of stuck-ON/bridging faults causing enhanced I_{DDQ}. This technique can also be used for detecting I_{DDQ} related faults in CMOS circuits.

1 Introduction

Quiescent power supply current monitoring (I_{DDQ}) has been identified as an effective technique for testing CMOS circuits [1,2,3]. I_{DDQ} testing is performed using either an external or a Built-In Current Sensor (BICS) Several schemes for current measurement are given in [4].

Various methods of test generation for I_{DDQ} testing have been described in [5-7] for CMOS circuits. In this paper, we describe an input pattern classification technique to generate test sets for detection of stuck-ON faults and bridging faults in BiCMOS circuits. This technique can also be used to generate test sets for detection of I_{DDQ} related faults in CMOS circuits.

This paper is organized as follows. Classification of input patterns is described in section 2. Section 3 deals with test sets for fault detection. Applicability of this technique for detection of I_{DDQ} related faults in BiCMOS and CMOS circuits is given in section 4. Finally, conclusions drawn from the study are given in section 5.

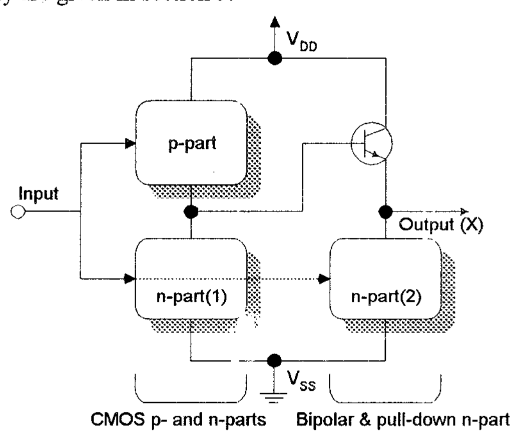

Figure 1: A general S-BJT BiCMOS device

2 Input Pattern Classification

In this section, we classify the input patterns according to the effect on the output in the presence of a fault. Block diagram of a general S-BJT BiCMOS device is shown in Figure 1. An S-BJT BiCMOS gate consists of CMOS p- and n-parts to perform logic function, a BJT and a pull-down n-part for driving the output node. Analysis of stuck-ON failures and various bridging faults is described in [8]. A section of the BiCMOS gate [p-part, n-part(1) or n-part(2)] is either conducting or not conducting for a given vector. Venn diagram for a fault-free BiCMOS device is shown in Figure 2(a). Let $\mathbf{P_t}$ denote the set of vectors which turn ON the p-part. Similarly, let $\mathbf{N_{1t}}$ and $\mathbf{N_{2t}}$ denote the set of vectors which turn ON the n-part(1) and n-part(2) respectively. $\mathbf{N_{1t}}$ and $\mathbf{N_{2t}}$ are equivalent, and equal to the complement of $\mathbf{P_t}$ as shown in Figure 2(a). $\mathbf{P_t^f}$, $\mathbf{N_{1t}^f}$ and $\mathbf{N_{2t}^f}$ are the set of vectors which turn ON the p-part, n-part(1) and n-part(2) respectively in the presence of fault f in that part. An input vector, when applied to a fault-free BiCMOS gate causes a conduction path in the p-part[V_{DD} to output and base of bipolar] or in n-part(1)[base of bipolar to Ground] and n-part(2)[Output to Ground].

Below we give a lemma that summarizes the impact on the sets $\mathbf{P_t}$, $\mathbf{N_{1t}}$, $\mathbf{N_{2t}}$ due to the different stuck-ON/bridging faults. Under the single stuck-ON/bridging fault in the n-part(1), the following lemma applies.

Lemma 1: The set of vectors $\mathbf{N_{1t}}$ that cause the n-part(1) to turn ON in a BiCMOS gate is a proper subset of the set of vectors ($\mathbf{N_{1t}}$) that turn ON the n-part(1) in the presence of the stuck-ON/bridging fault, i.e., $\mathbf{N_{1t}} \subset \mathbf{N_{1t}^f}$.

Proof: Consider an input pattern $\underline{t} \in \mathbf{N_{1t}}$. As $\mathbf{N_{1t}}$ is the set of vectors which makes the n-part(1) conduct, there is at least one conduction path through the n-part(1) for this vector. Consider an input patter $\underline{t} \in \mathbf{N_{1t}^f}$. As f is a stuck-ON/bridging fault causing an additional conduction path, the vector $\underline{t} \in \mathbf{N_{1t}}$ will also be a vector $\underline{t} \in \mathbf{N_{1t}^f}$. Thus, if $\underline{t} \in \mathbf{N_{1t}}$, then $\underline{t} \in \mathbf{N_{1t}^f}$.

Now, consider a vector $\underline{t'} \in \mathbf{N_{1t}^f}$ which causes n-part(1) to provide a single conduction path through the transistor T containing the stuck-ON fault due to the bridging fault. As T is stuck-ON or in the presence of bridging fault, there will be a vector $\underline{t'}$ such that the gate voltage applied to transistor T is logic '0' such that an additional conduction path is created. This vector when applied to fault-free circuit will not cause the additional conduction path. Thus $\underline{t'} \notin \mathbf{N_{1t}}$. This completes the proof that $\mathbf{N_{1t}} \subset \mathbf{N_{1t}^f}$. The resulting $\mathbf{N_{1t}}$ region in the Venn diagram is shown in Figure 2(b).

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Similarly, the proof given for Lemma 1 can be easily extended for n-part(2) and p-part [8]. The theorem given below follows from the above lemma [8].

Theorem: The set of vectors that cause the transistors in any part [n-part(1), n-part(2) or p-part] to turn ON in a BiCMOS gate under fault-free condition is a proper subset of the set of vectors that turn ON the corresponding part in the presence of a stuck-ON/bridging fault.

The proof of this theorem follows from the above lemma and can be found in [8].

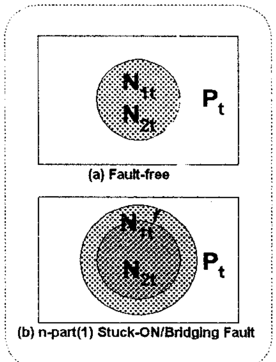

Figure 2: Venn diagrams for S-BJT BiCMOS stuck-ON/Bridging faults

3 Test Sets for Fault Detection

In the presence of a stuck-ON/Bridging fault, the sub-set of the vectors turning the corresponding conduction paths ON increase, resulting in the expansion of the corresponding regions in the Venn diagram. Based on this, test-sets to facilitate I_{DDQ} testing for the various stuck-ON/Bridging faults in a BiCMOS gate can be generated as given below:

The test-set to detect faults in p-part: $\{P_f \cap (N_{1t} \cap N_{2t})\}$.

The test-set to detect faults in n-part(1): $\{N_{1f} \cap P_t\}$.

The test-set to detect faults in n-part(2): $\{N_{2f} \cap P_t\}$.

The test-set to detect faults in bipolar transistor: $\{N_{1t} = (N_{2t})\}$.

4 Applicability to CMOS Circuits

Whenever a test vector is applied to test for a particular stuck-ON or bridging fault from the test sets obtained, results in enhanced I_{DDQ} to be drawn by the circuit partition. Thus, monitoring I_{DDQ} in conjunction with the test sets generated using the technique mentioned in this paper would detect the I_{DDQ} related fault.

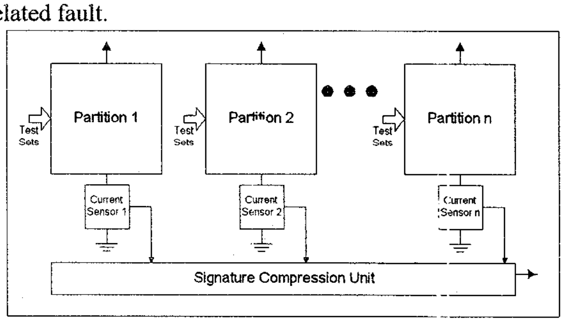

Figure 3: An example IDDQ testing implementation

Figure 3 shows the implementation of I_{DDQ} testing for a large circuit partitioned into smaller partitions and each partition using independent external or built-in current sensors. The test sets are generated and applied to each of the circuit partitions independently. Since each module or partition has its own current sensor, it is impractical to observe the output of every current sensor. One solution to this problem is to propagate the outputs of all the sensors to one observable output pin which is designed solely for the signature extractor or information compression unit. When any of the partitions in the circuit causes enhanced I_{DDQ} to be drawn, the signature compression unit output flags the condition.

The above methodology of generating test sets for BiCMOS circuits can be used for generating test sets for CMOS circuits. CMOS circuits have only a p-part and an n-part as opposed to a p-part, two n-parts and the bipolar transistor in case of S-BJT BiCMOS devices. Hence, the test sets need to be found only for p-part (**P_f**) and for the n-part (**N_f**).

5 Conclusions

Pattern classification scheme was shown for BiCMOS gates under stuck-ON/bridging faults. A methodology for generation of test sets in BiCMOS circuits using the above scheme was presented. Implementation of an I_{DDQ} testing scheme by partitioning large circuit into smaller partitions and applying the generated test sets was presented. The test sets obtained can be used for detecting the stuck-ON faults as well as bridging faults that occur in BiCMOS as well as CMOS devices using I_{DDQ} monitoring techniques, by way of external I_{DDQ} sensors or Built-in current sensors (BICS).

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