

A Proper Deep Submicron MOSFET Model (PDSMM) and Its Applications for Delay Modeling of CMOS Inverters

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Abstract

A new and simple proper deep submicron MOSFET model (PDSMM) is proposed to accurately describe deep submicron MOSFET I-V characteristics. The second-order effects of deep submicron metal-oxide semiconductor field effect transistors (MOSFETs) such as charge carrier velocity saturation and channel length modulation are included in the PDSMM. The PDSMM is the extension of Shockley-Sah MOSFET model and Shichman-Hodges MOSFET model taking the second-order effects into account. Propagation delays of a complementary metal-oxide semiconductor (CMOS) inverter are obtained by using the PDSMM and by considering input transition time, drain diffusion capacitance, output load capacitance and gate-drain coupling capacitance. Even in the extreme conditions, the calculated results of propagation delays of deep submicron CMOS inverters are accurate compared with SPICE results of BSIM3 model. This shows that the proposed PDSMM is suitable to accurately simulate deep submicron MOSFET I-V behaviors.

Introduction

Propagation delay of deep submicron CMOS digital circuits is one of the most critical parameters in CMOS digital designs. Simple, fast and accurate methods to calculate the propagation delay are needed for very large scale integrated circuit (VLSI) digital designers to verify and optimize their designs. One of approaches is to analytically derive timing models for CMOS digital circuits from various MOSFET models [3-11]. In order to accurately predict the propagation delay of CMOS digital circuits, the MOSFET models used for propagation delay calculations have to be simple and accurate to describe deep submicron MOSFET I-V characteristics. Several MOSFET models are widely used in the analytical time delay analysis [1][2][6][8-9].

The existing MOSFET models, however, are either not accurate enough to model deep submicron MOSFET characteristics or too complex to be directly used in the analytical timing models. Based on the discussion of the second-order effects of deep submicron MOSFETs, we propose a proper deep submicron MOSFET model (PDSMM) in this paper. The propagation delays of a 0.18 μ m CMOS inverter are calculated for a broad combination of input transition times and connected output load capacitances. The result shows that the PDSMM and timing analysis model are accurate.

Shockley-Sah MOSFET model

The first proposed MOSFET model is Shockley-Sah MOSFET model [1-2]. In Shockley-Sah MOSFET model, the drain-source current I_{ds} is expressed as:

$$I_{ds} = \begin{cases} 0 & V_{gs} \leq V_{th} \\ k \left(V_{sat} - \frac{V_{ds}}{2} \right) V_{ds} & \begin{matrix} V_{gs} \geq V_{th} \\ V_{ds} \leq V_{sat} \end{matrix} \\ \frac{1}{2} k V_{sat}^2 & \begin{matrix} V_{gs} \geq V_{th} \\ V_{ds} > V_{sat} \end{matrix} \end{cases} \quad (1)$$

In (1), V_{gs} is the gate-source voltage, V_{ds} the drain-source voltage, V_{th} the threshold voltage, k the transconductance parameter, and V_{sat} the drain-source saturation voltage of MOSFET which is

$$V_{sat} = V_{gs} - V_{th} \quad (2)$$

Shockley-Sah MOSFET model was developed for long channel MOSFETs. This simple model is widely used in treating long channel MOSFET circuits analytically [3-4]. However, Shockley-Sah MOSFET model cannot reproduce the I-V characteristics of deep submicron MOSFETs since the second-order effects of deep submicron MOSFETs are ignored. The four main discrepancies for deep submicron MOSFET behaviors are shown in Fig. 1. The first is that drain-source current

I_{ds} in the saturation region of deep submicron MOSFET does not show square-law dependence on gate-source voltage V_{gs} as in (1) and (2). The second discrepancy is that the drain saturation voltage V_{sat} of deep submicron MOSFET is quite less than that from the linear relation with gate-source voltage predicted in (2).

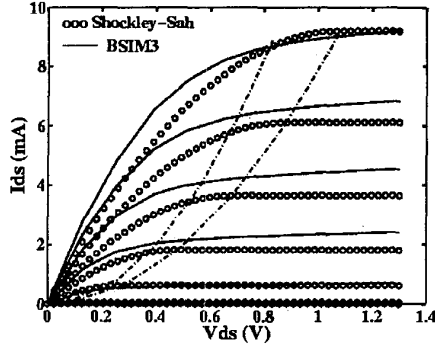


Fig. 1. Shockley-Sah MOSFET model and BSIM3 MOSFET model

The third one is that drain-source saturation current I_{ds} of deep submicron MOSFET with a given V_{gs} , is much less than the predicted value of the Shockley-Sah MOSFET model where the carrier mobility is constant. The fourth deficiency is that the effect of channel length modulation is not taken into account in Shockley-Sah MOSFET model. The lack of the effect of charge carrier velocity saturation in Shockley-Sah MOSFET model gives rise to the above three discrepancies in deep submicron MOSFETs. In other words, the effect of charge carrier velocity saturation in a high electric field has to be considered in the deep submicron area. Besides that, the channel length modulation also has to be included in the deep submicron MOSFET model.

Second-order effects of deep submicron MOSFETs
Effect of charge carrier velocity saturation

When gate-source voltage V_{gs} of an n-MOSFET is greater than the threshold voltage V_{th} ($V_{gs} > V_{th}$), electrons move from the source to the drain along the n-channel, under the influence of electric field E . Fig. 2 shows the effect of charge carrier velocity saturation along the channel. It can be modeled by the simplified expression [12]:

$$v = \frac{\mu_0 \cdot E}{1 + |E/E_C|} \quad (3)$$

where v represents the velocity magnitude along the channel, μ_0 the low-field carrier mobility, E the applied electric field, and E_C the critical electric field.

Effect of channel length modulation (Shichman-Hodges MOSFET model)

The space-charge region at the drain end of the channel for saturation operation region ($V_{ds} > V_{sat}$) varies with the drain voltage V_{ds} . The channel shortening can be

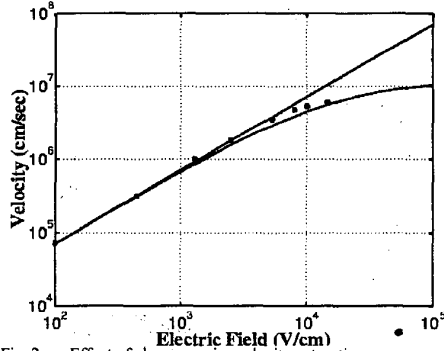


Fig. 2. Effect of charge carrier velocity saturation

modeled as being linearly proportional to V_{ds} with a channel length modulation parameter λ . Taking it into account, Shichman and Hodges proposed the following MOSFET model [13]:

$$I_{ds} = \begin{cases} 0 & V_{gs} \leq V_{th} \\ k \left(V_{sat} - \frac{V_{ds}}{2} \right) V_{ds} (1 + \lambda V_{ds}) & V_{gs} \geq V_{th} \\ & V_{ds} \leq V_{sat} \\ \frac{1}{2} k V_{sat}^2 (1 + \lambda V_{ds}) & V_{gs} \geq V_{th} \\ & V_{ds} > V_{sat} \end{cases} \quad (4)$$

All the other parameters and variables of (4) have the same meanings as Shockley-Sah MOSFET model except for λ . The improvement of Shichman-Hodges model over Shockley-Sah model is the term of $(1 + \lambda V_{ds})$ in the equation of saturation region. The term of $(1 + \lambda V_{ds})$ in the equation of linear region is used to meet the continuity of the above equations at $V_{ds} = V_{sat}$. There is no physical justification to do so. The channel length modulation coefficient λ is quite small for long channel MOSFETs, but increases considerably for deep submicron MOSFETs.

Proposed MOSFET models

Deep submicron MOSFET model (DSMM)

Combining the effects of charge carrier velocity saturation in (3) and channel length modulation in (4), we can derive a general MOSFET model. It is termed as the deep submicron MOSFET model (DSMM) since the second-order effects of deep submicron MOSFETs are

included. The drain-source current I_{ds} in DSMM is expressed as

$$I_{ds} = \begin{cases} 0 & V_{gs} \leq V_{th} \\ k \left(V_{gs} - V_{th} - \frac{V_{ds}}{2} \right) \frac{V_{ds}(1 + \lambda V_{ds})}{1 + V_{ds}/V_c} & V_{gs} \geq V_{th} \\ & V_{ds} \leq V_{sat} \\ \frac{1}{2} k V_{sat}^2 (1 + \lambda V_{ds}) & V_{gs} \geq V_{th} \\ & V_{ds} > V_{sat} \end{cases} \quad (5)$$

In (5), all the other parameters and variables have the same meanings as in (1) or (4) except for V_c and V_{sat} . V_c is the critical voltage of the MOSFET defined as the product of the critical electric field of (3) and effective channel length and V_{sat} , the saturation voltage in DSMM, instead of (2), is

$$V_{sat} = V_c \cdot \left(\sqrt{1 + 2 \cdot \frac{V_{gs} - V_{th}}{V_c}} - 1 \right) \quad (6)$$

The additional term $(1 + V_{ds}/V_c)$ in the linear region of (5) and V_{sat} shift from (2) are caused by the effect of charge carrier velocity saturation. Obviously, the DSMM model in (5) and (6) is the extension of Shockley-Sah model and Shichman-Hodges model with strong physical meanings. The DSMM model substantially improves the accuracy to describe deep submicron MOSFET behaviors as the second-order effects of deep submicron MOSFETs are include in DSMM.

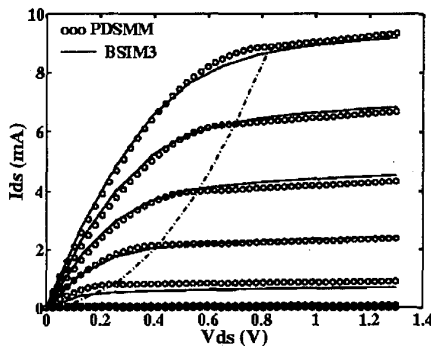


Fig. 3. Proper deep submicron MOSFET model (PDSMM) and BSIM3 model

Proper deep submicron MOSFET model (PDSMM)

DSMM is easily used in numerical calculation of VLSI circuit analysis. However the differential equation to describe CMOS inverters in timing analysis cannot be solved analytically due to the term $(1 + V_{ds}/V_c)$ in the denominator of (5). In order to solve the issue, we propose the proper deep submicron MOSFET model (PDSMM). The main ideas are that the equations to describe saturation region $I_{ds}(sat)$ and drain saturation

voltage V_{sat} are kept the same as that of DSMM and in the linear region the PDSMM takes the equation format of Shockley-Sah MOSFET model. With this modification, the PDSMM model is:

$$I_{ds} = \begin{cases} 0 & V_{gs} \leq V_{th} \\ k \left(V_{sat} - \frac{V_{ds}}{2} \right) V_{ds}(1 + \lambda V_{sat}) & V_{gs} \geq V_{th} \\ & V_{ds} \leq V_{sat} \\ \frac{1}{2} k V_{sat}^2 (1 + \lambda V_{ds}) & V_{gs} \geq V_{th} \\ & V_{ds} > V_{sat} \end{cases} \quad (7)$$

Fig. 3 plots the I-V characteristics of 0.18μm nMOSFET calculated from PDSMM. The I-V characteristics obtained from SPICE simulation by using BSIM3 model is shown as a comparison. It shows that PDSMM is very accurate.

Propagation delay of CMOS inverters using PDSMM
Differential equation of CMOS digital inverter

Fig. 4 shows the CMOS inverter used to calculate the propagation delay. The gate-drain coupling capacitance C_m is included and obtained from SPICE simulation. The capacitance C_{load} consists of the output load capacitance and drain diffusion capacitance.

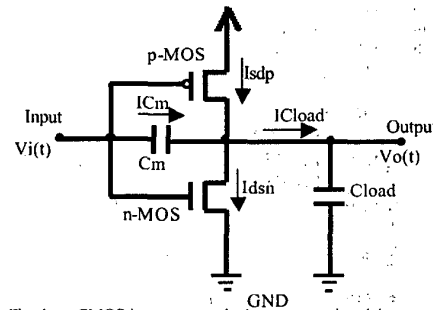


Fig. 4. CMOS inverter to calculate propagation delay

The differential equation to describe the transition behaviors of CMOS inverter is obtained from the application of the Kirchoff's current law at the output node:

$$\frac{dV_{out}}{dt} = \frac{C_m}{C_{load} + C_m} \cdot \frac{dV_{in}}{dt} + \frac{I_{sdp} - I_{sdn}}{C_{load} + C_m} \quad (8)$$

Calculated propagation delay

By using PDSMM and solving the differential equation (8) analytically, we can obtain the propagation delay of CMOS inverters. The detailed solution is beyond the scope of this paper.

Fig. 5 shows the calculated result of the propagation delay of the CMOS inverter as a function of input

transition time and output load capacitance. The input transition time ranges broadly from 10ps to 400ps. The output load capacitance spans largely from 0fF to 800fF. Note that the drain diffusion capacitance is included in *Cl_{oad}*. The calculated delay changes from around 11ps to 137ps.

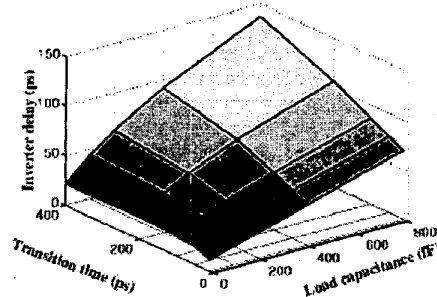


Fig. 5. 3-D plot of propagation delay from PDSMM. Fig. 6 shows that the calculated delay of the inverter from PDSMM compared with the delay of the same inverter from SPICE simulation of BSIM3 model. The dotted lines are $\pm 5\%$ away from BSIM3 model. This indicates that the correlation between them is high and the PDSMM is accurate to describe the deep submicron MOSFET I-V characteristics.

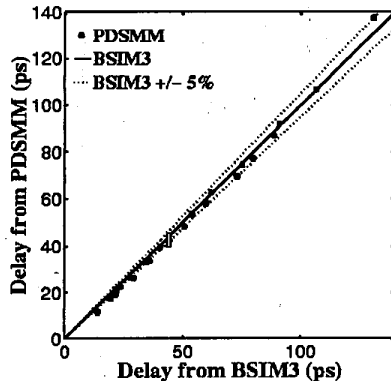


Fig. 6. Correlation of calculated propagation delay with SPICE result

Conclusions

A new and simple proper deep submicron MOSFET model (PDSMM) is introduced to include the second-order effects of deep submicron MOSFETs. The new model expresses the salient features of deep submicron

MOSFET I-V characteristics. The propagation delay is analytically calculated based on the PDSMM. This provides fast and accurate timing calculation for CMOS inverters. The technique presented in this work significantly accelerates timing calculations at least two orders of magnitude faster than SPICE, while maintaining reasonable accuracies. This method can be extended to other CMOS digital circuits such as NAND/NOR logic gates and transmission gates. The accurate analytical timing methodology can be incorporated into deep submicron VLSI digital design, verification, and optimization flows such as timing-driven synthesis, timing closure, and performance-driven place and route (PAR).

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