

Clustering Based Techniques for I_{DDQ} Testing

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Abstract

A new technique for evaluating I_{DDQ} data using a clustering based approach is presented. While prevailing I_{DDQ} test techniques rely on a fixed threshold or the current signature of an IC, the proposed technique relies on abnormalities of the I_{DDQ} distribution of a device with respect to other devices in the test set. Results of applying this technique to data collected on a high volume graphics chip are described. Results are also compared to the conventional single threshold approach, and benefits of the new technique are presented.

1. Introduction

Considerable evidence has been presented over the last few years on the benefits of I_{DDQ} testing and that it can significantly contribute to the overall quality of the device under test (DUT) [1, 2]. Ample studies have shown the practicality in using this method of testing to improve the thoroughness of the test strategy adopted [3, 4]. Despite this, there has been some hesitancy on the part of IC manufacturers to universally adopt I_{DDQ} testing as an integral part of their test strategy due to several reasons. A major issue has been the absence of a commonly accepted procedure for selecting a threshold level beyond which a device can be deemed defective [5]. Another factor is the notion that elevated I_{DDQ} currents do not necessarily translate into defective ICs in all cases. In addition to this existing scenario, doubts have been expressed about the applicability of this technique in the future [6]. Advances in IC design and process technologies have equally fostered this line of thinking due to the adoption of deep sub-micron processes for IC manufacturing. This has resulted in more complex functionality being integrated onto the same piece of silicon. In turn, this has directly resulted in an increase in the quiescent currents of ICs being manufactured today. Since the fundamental notion of I_{DDQ} testing lies in the ability to differentiate between the quiescent currents of normal and defective ICs, the possibility that I_{DDQ} testing may have reached its limits of applicability is a valid concern. The fact that the normal quiescent current of an IC will be

indistinguishable from the current that would be measured in the presence of a defect may result in I_{DDQ} testing not being a feasible practice in the near future. Hence, newer and more innovative approaches are required to evaluate the measured I_{DDQ} data.

In this paper, we present a new I_{DDQ} test technique based on clustering through which decisions on device quality can be made with a higher degree of confidence. The motivation for this work was the inability of current approaches to address both existing problems and ones that are bound to arise in the future. This technique allows for the identification of ICs with abnormal current distribution with respect to other ICs being tested. The term current distribution refers to the set of measured I_{DDQ} values of a device for all the applied vectors. This contrasts with present approaches where each IC is tested individually with respect to a predetermined threshold level. There are several advantages to this technique, some of which include a natural classification of devices based on I_{DDQ} measurements, elimination of the need to set a static threshold, and in cases where it is so desired, to provide a means by which a threshold level can be chosen.

The core of the new approach lies in applying conventional cluster analysis techniques to I_{DDQ} testing. This is done by representing each IC as a point in the n -dimensional space of I_{DDQ} measurements, where n is the number of vectors applied. The outputs of this process are groups of devices that are in close proximity to each other with respect to I_{DDQ} values measured across all the applied vectors. In a typical scenario, one large group containing the majority of devices with normal quiescent current distributions and several smaller groups with abnormal distributions can be expected. The goal is to allow the clustering process to classify the devices as opposed to classifying with an arbitrary or predetermined threshold.

This technique was first introduced in [8] where the basic clustering technique along with the initial results obtained when it was applied to manufacturing data was

presented. It also included details on specifying various clustering criteria for forming different numbers of clusters and how that affected the classification of devices. The ideal number of clusters to be formed while using this technique was suggested. In this paper, we extend our earlier work by presenting a comparison of the results obtained through the use of the clustering technique to those obtained when a static threshold is used. Descriptions of the different devices detected through each technique and an analysis on why the differences exist are presented. Details on the process and methodology that were developed while working on the new clustering technique are also outlined. A description of how the steps involved in the new technique fit into the overall product development flow are also included. A detailed description of the proposed technique can be found in [9].

This paper is organized as follows: Section 2 reviews the 'current signatures' approach and contrasts that with the proposed technique. A brief introduction to cluster analysis techniques and their uses are discussed in section 3. Section 4 provides an overview of the complete flow involved in the new technique, which is followed by a brief description of the concept and the data involved in this work. In section 5, results obtained by applying the clustering technique to production data are presented. Interpretation of the results and the benefits are presented in sections 6 and 7. The paper ends with conclusions in section 8.

2. Comparison with Current Signatures

In the 'current signatures' approach [7, 10], the concept of using a dynamic threshold as opposed to a static threshold limit was proposed. In this method, all vectors applied to the DUT and their corresponding I_{DDQ} measurements are taken into account. Predictions on device quality are made by constructing 'current signatures' which are recognizable responses for each die to all the applied vectors. These 'current signatures' are arrived at by allocating measurements of equal magnitude corresponding to all the vectors into one level, and then sorting the levels in order of magnitude. Based on the number of levels in the signatures and the magnitude of the different levels, conclusions on the quality of the devices are made. From the 'current signature', information on the kinds of defects that may cause this elevated I_{DDQ} can also be gathered.

There are several advantages to this technique. The main benefit being that instead of using a static limit for evaluating I_{DDQ} measurements, a dynamic threshold approach is used. This eliminates the need for pre-determining the value beyond which I_{DDQ} values can be termed abnormal. The approach can thus be used in the

presence of elevated background currents as it uses the differences between I_{DDQ} measurements instead of the magnitude of the measurements itself [10]. Another benefit of this technique is in the diagnosis of the physical defect behind the high current.

Though the 'current signatures' approach is definitely a step forward, there are still several questions that need to be answered about the applicability of this technique in the future. One of the problems facing this approach is that inherent high current states in the design can also result in an IC being classified as defective. Normal circuit operation can also result in these elevated I_{DDQ} currents resulting in a step in the I_{DDQ} signature. In addition, since the measurements are eventually compared against a predetermined threshold value, it is insensitive to larger current values. This can result in incorrectly labeling an IC as defective in the presence of large background currents. In cases where one vector is causing a high current state in the majority of devices, since each device is considered in isolation, such states instead of being considered a design trait cause the device to be labeled defective.

The approach proposed in this paper takes into account the inherent high current states of the design in addition to being able to differentiate between good and bad devices even in the presence of large background currents. The proposed method does not rely on a fixed threshold. Rather, it detects devices with abnormal current distributions with respect to other devices from a larger set. This is possible because the measurements are viewed relative to the measurements made on a number of devices.

3. An Introduction To Clustering

The objective of cluster analysis techniques is to sort observations or data points within a large data set into smaller groups or clusters such that members of each group have a high degree of similarity with other members of the same group. It is a process by which observations exhibiting similar characteristics are grouped together. The aim in applying cluster analysis techniques to any set of data is to uncover hidden patterns that reside within the set. Clustering helps in formulating a statistical classification based on which further conclusions can be drawn. An important trait of any clustering technique to bear in mind is that its application and interpretation are subjective.

Clustering can be more formally defined as a process by which a collection of N objects or entities, each of which is described by n characteristics (n I_{DDQ} measurements), are divided into k groups, where typically $k \ll N$. The

total number of members, m_i , in each cluster C_i adds up to the total number of entities N .

The number of groups to be formed and the basis on which this classification is done is a function of the specific clustering algorithm being used and can be customized to fit the application and purpose of the process. More information on cluster analysis techniques and their uses in different areas can be obtained from [11] and [12]. Since such techniques can be applied to varied fields, a large number of clustering algorithms have been developed. Due to the subjective nature of the clustering problem, the task of finding the best technique is fruitless. Rather, the peculiarities and features of a technique or program should be kept in mind while selecting the clustering program for a particular application. The clustering program that we selected is based on two common clustering techniques called the K-means algorithm and the leader algorithm [8, 9].

4. Clustering Applied to I_{DDQ} Testing

An approach that is based on applying the same fundamental cluster analysis techniques to the I_{DDQ} testing arena is presented here. The criteria that we considered while selecting the application was the ability to define the number of final clusters to be formed, user specifiable distance metrics, customizable minimum distances separating data points, computational speed, flexibility to add new features, and the treatment to outliers in the data set. The different steps involved in the new clustering based technique and where they fit into the overall flow are shown in figure 1.

To the left of the flow chart, the high level steps involved in the product development flow are shown. On the right of the figure, the steps inherent to the clustering technique are shown inside the dotted area. Once the I_{DDQ} measurements are taken on the Automated Test Equipment (ATE), a data-formatting step to translate the ATE data into a format acceptable by the

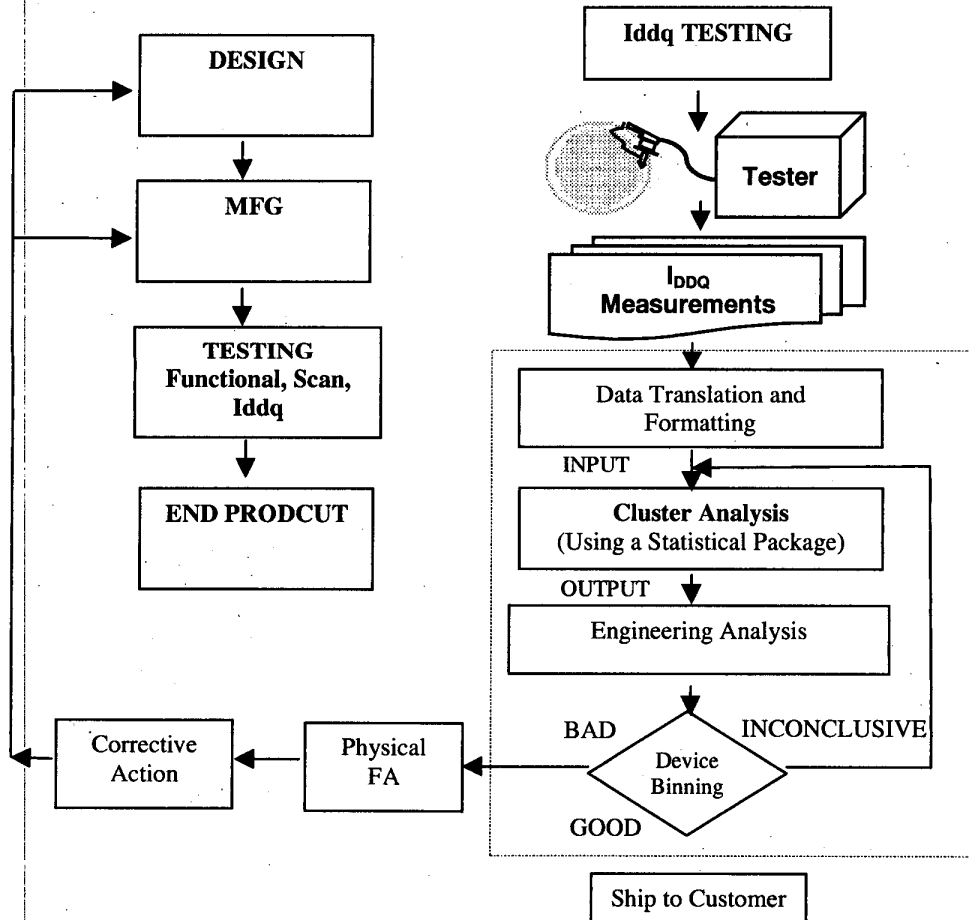


Figure 1: Flow Diagram

statistical tool is required. This data is then subjected to cluster analysis. The results from this step are used in the engineering analysis stage of the flow. Here, the results are formatted into an easily interpretable graphical form. These steps can be easily automated and integrated into the production test environment.

Through the clustering process, classification of devices into different clusters that exhibit a varied range of current distribution, upper and lower bounds, and average current values is achieved. Unless abnormalities exist, all devices in the cluster(s) that does not exhibit any abnormalities on the above mentioned factors are treated as good ICs and shipped to the customer once the necessary steps in the product flow are complete. If there exist any abnormal conditions in any cluster, depending upon the extent of such conditions, the devices in that cluster are either subjected to another iteration of the clustering process or sent for physical failure analysis (PFA). Based on the PFA report, corrective action is fed back to either the manufacturing or design steps of the product flow.

4.1 Background on the Data used

The feasibility of the proposed approach was studied by applying it to I_{DDQ} data collected on a high volume device manufactured in a deep sub-micron process at Texas Instruments. The device contains ~650k (2-input NAND equivalent) gates and has extensive Design-for-Testability (DFT) features including full scan. All the vectors that were applied while obtaining the I_{DDQ} measurements were generated using a commercially available ATPG tool.

For the purpose of our work, 30 I_{DDQ} measurements were taken on 627 devices. The number of I_{DDQ} measurements in the production environment is typically around 10. A fault coverage of 95% (pseudo stuck-at fault model) was obtained with these 30 vectors. The cluster analysis done here was thus in 30-dimensional space. Due to the proprietary nature of the data, a certain degree of normalization has been done before presenting it here.

4.2 Theoretical Foundation of the Concept

The proposed clustering technique takes into account the I_{DDQ} distribution of each device for all applied I_{DDQ} vectors. By comparing this I_{DDQ} distribution of each device to that obtained on other devices and using the results of this comparison while evaluating device quality, the proposed technique eliminates problems associated with prevailing practices of I_{DDQ} testing. As

mentioned earlier, these problems include threshold level determination, high normal and background currents, and inherent high current states. Since a broader range of parameters are considered while making final decisions, dependencies on individual parameters are reduced and greater confidence on device quality can be achieved. Variations in the manufacturing environment that cause process to process and wafer to wafer changes in the measured values can be accounted for. As a large set of devices are grouped into a much smaller sub-set containing all the devices from the original data set, further possibilities of the clustering process result. An inherent advantage of this classification is that a small number of devices from one cluster will prove to be a representative sample of the majority of devices. This advantage lends itself to extrapolating the results and inferences made on this smaller set of devices to a larger set within the same cluster, thereby reducing the effort involved in yield enhancement. This is discussed in more detail in section 7.

5. Results

Clustering the 627 devices in 30-dimensional space resulted in 5 groups of devices that exhibited similar characteristics for all I_{DDQ} vectors. Table 1 shows the distribution of I_{DDQ} currents over 5 clusters. Figure 2 is a graphical representation of this data. On the X-axis, the number of devices grouped into each cluster are shown. On the Y-axis, the I_{DDQ} distribution in mA of all the devices in that cluster are shown. This is a range as opposed to a single value due to the fact that the measurements corresponding to each of the 30 vectors are being depicted. The lowest, highest and mean of the readings is also shown in the figure. The mean value is the average value of all the I_{DDQ} values included in that cluster.

As can be seen from the figure, out of the 627 devices that were in the original data set, a majority of them (472) were grouped into cluster 4. Of the remaining devices, 104 were grouped into cluster 5. Cluster 2 contained 39 devices and cluster 3 contained 11. The sole device remaining was grouped into cluster 1 by itself. From the grouping of devices into different clusters, it is clear that devices classified into a particular cluster exhibited similar I_{DDQ} current distribution. This is evident from the fact that a majority of devices were classified into the cluster that had the smallest magnitude and current distribution (cluster 4). Similarly, devices that exhibited I_{DDQ} currents of a higher magnitude and distribution were grouped into different clusters and were smaller in number. The device that was in a cluster by itself had a wide range of I_{DDQ} currents for the 30 vectors applied and hence its placement can be justified

since this was not similar to devices in any of the other clusters.

Cluster	Die Count	MIN	MAX	MEDIAN
1	1	0.70116	7.16175	6.228105
2	39	3.65497	8.40208	5.846465
3	11	6.62434	9.93447	8.072035
4	472	0.42272	3.51672	0.744
5	104	0.87057	6.86384	0.87057

Table 1: Cluster Statistics

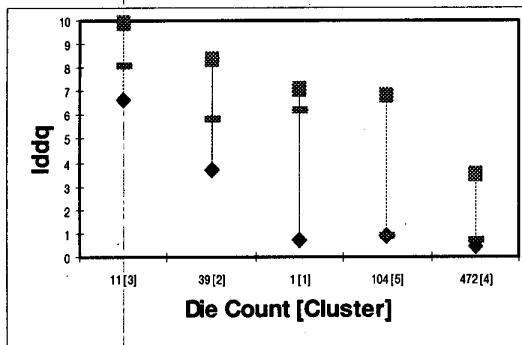


Figure 2: Cluster Statistics

Further proof of good classification of the devices can be seen in figure 3, which presents a normalized histogram of the currents in each cluster. In this figure, cluster 1, which contained only one device, is not shown. Although there was a slight overlap of I_{DDQ} measurements, a clear demarcation exists between the different clusters. It should be noted that this is a normalized figure and the values shown are not actual measurements.

6. Discussion

From figure 2, by considering various factors, for instance, the distribution of devices into different clusters, the maximum current distribution of each cluster, and the minimum, maximum and median values of each cluster, device quality predictions can be made. A fair assumption to start off with is that the majority of devices are defect free and that only a small percentage of devices are defective. If this assumption were valid, the variation in currents of the cluster into which the majority of devices were grouped can be used as the benchmark. Any cluster that exhibits a variation beyond this cluster can be viewed with some amount of suspicion with respect to their quality, thus providing a

dynamic threshold. In our case, the majority of devices were in cluster 4 and this cluster has the smallest value in its I_{DDQ} distribution. By starting with this assumption, a standard beyond which all other clusters can be deemed defective is being set.

Due to a systemic error in the manufacturing process, there may be cases where the majority of devices are defective. In such a case, the majority of defective devices would be grouped into one cluster. In this case, the variation of currents for this cluster would be correspondingly high and hence, would be immediately flagged in this process. If however, they are indeed showing either a small variation of currents or a small median value, the assumption that the majority of devices are defect free would be generally valid.

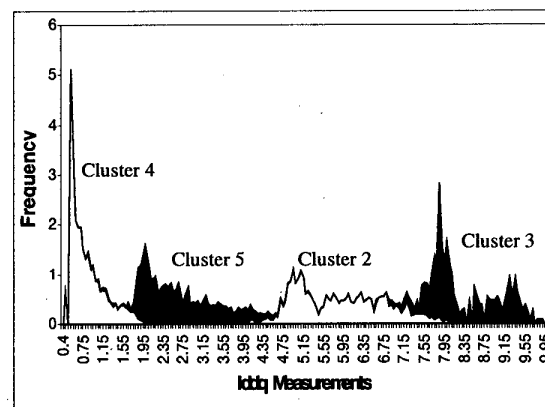


Figure 3: Normalized Histogram

Though cluster 5 from figure 2 exhibits a very low median, the variation of the currents in this cluster is relatively large. Hence, it is obvious that some devices that had high I_{DDQ} measurements were grouped into this cluster along with other devices that had lower measurements. Three possibilities to explain the classification of such devices into cluster 5 exist. The first is that there could be a single vector causing a high current state in all devices. The second could be that there are certain devices that exhibited higher quiescent currents for all vectors. The former can be ruled out due to the median of this cluster being very low. The latter can be eliminated due to the fact that if this were the case, these devices would be grouped into a different cluster. The third explanation is that there is a combination of these two. In other words, a small number of devices may have exhibited higher currents for a small number of vectors. This seems to be the most plausible explanation. To fully understand why this happened, and to explain the higher current distribution, the devices in cluster 5 were subjected to the clustering process again i.e. the 104 devices that were in cluster 5

were treated separately and the clustering process repeated. The results obtained fully justified this line of thinking. The results of this analysis are shown in table 2 and figure 4 respectively.

Cluster	Die Count	Min	Max	Median
5.1	35	1.62411	4.83882	2.69892
5.2	1	1.20742	6.86384	3.225625
5.3	26	2.29587	5.05106	3.69001
5.4	41	0.87057	3.34342	2.05248
5.5	1	1.65915	5.36066	1.878205

Table 2: Statistics of Cluster 5 - 104 Devices

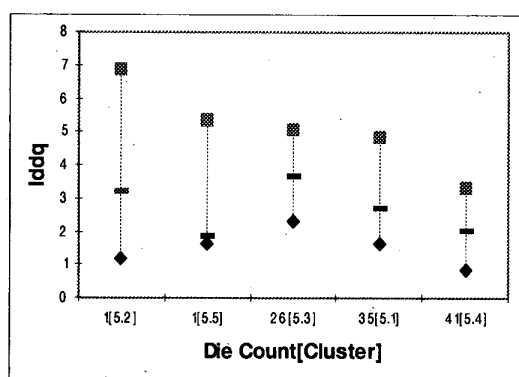


Figure 4: Statistics of Cluster 5 – 104 Devices

As anticipated, there were indeed some devices that exhibit higher currents for a small number of vectors as seen from the distribution of devices into the 5 clusters and the variation of currents. The classification of the devices in cluster 5.4 (numbering 41 devices), cluster 5.1 (35 devices), and cluster 5.3 (26 devices), cannot have caused the higher variation of current in cluster 5 of figure 2. That variation is due to the presence of the devices in clusters 5.2 and 5.5 (each containing 1 device). This raises the questions of whether incorrect classification of the devices occurred, thereby escaping detection through the clustering process and further, if these same devices would have been classified as defective using a threshold limit. The former can be attributed to the fact that since a limited number of final clusters were specified these devices were more similar to other devices in this cluster rather than any other. The latter is not valid since the high variation in currents did raise a flag about the devices in cluster 5. Upon running these devices through the clustering process a second time, such abnormal devices were isolated. Hence,

though the first round of clustering did not reveal this anomaly, subsequent analyses did identify these devices. Once the initial benchmark is set, further subdivisions of the other clusters can also be made. For instance, once all devices in cluster 4 (figure 2) have been labeled good devices, clusters 1, 2 and 3 can be qualified as defective devices. The remaining cluster, cluster 5, cannot be conclusively classified as either defective or defect-free. Since it contains a very wide range of distribution, a little caution before labeling them defect-free might be prudent. On the other hand, devices in this cluster cannot be termed defective due to the very low median of this cluster. As explained earlier in this section, in such cases, a second round of clustering will provide more information that can be used to arrive at a final conclusion. Hence, from the output of the new clustering technique proposed, out of the 627 devices analyzed, 472 were labeled defect free resulting in a yield loss of approximately 25% if taken alone and all the remaining devices are rejected. However, in practice, only devices in clusters 1, 2, and 3 have a probability of being rejected. This would translate to a yield loss of 8%. And with the devices in cluster 5, which cannot be immediately termed as either good or bad devices, several options exist. They can be subjected to targeted failure analysis in an attempt to improve yield during the early life of a new product. Or, physical failure analysis to understand the reasons behind the higher currents can be performed. In the latter case, process and design enhancements can be adopted thereby improving the overall quality of the device.

Though the results obtained were promising, a comparison to conventional threshold setting approach was felt necessary. One of the biggest problems with the static threshold approach is the threshold value determination itself. Since this is a problem that is widely known and commonly accepted, it is not used in the argument here. As the goal was to make a fair comparison in evaluating the new technique, a threshold level that could identify an equal number of defective devices as obtained through the clustering technique was used. The number of defective devices from clustering was estimated at 51 (clusters 1, 2 and 3 of figure 2). Accordingly, the data was evaluated and it was found that a threshold set at 5.15 mA resulted in 51 devices failing the static threshold tests. After the identification of these devices, the failing sets of devices from the two techniques were compared to observe any overlap that existed. It was found that 49 devices were common to both sets. There were two devices flagged by each technique that were different. The devices rejected only through the clustering process were identified as devices 183 and 471. And those that were rejected only by the

static threshold method were identified as devices 249 and 254. These results are shown in figure 5.

From these results, it seemed that the clustering was working at least as well as a static threshold approach. We now had to understand why the devices detected only through the static threshold approach escaped detection using the clustering technique. The first issue was to understand how devices that were detected as being defective using a threshold of 5.15 mA escaped detection through the clustering process. Upon closer observation, these two devices were ones that exhibited elevated I_{DDQ} values for 8 of the 30 measurements taken. Due to the fact that there were several readings that were not very high, and further, since the clustering was done by restricting the number of clusters to only five, these devices were grouped into cluster 5 in the first iteration of the clustering process (figure 2). Since this immediately raised a flag, as the distribution for this cluster was relatively high, this cluster was subjected to further clustering as noted earlier. From the results obtained in the second analysis, as shown in figure 4, these two devices were now classified into clusters 5.2 and 5.5. In other words, though these devices escaped early detection through clustering, by performing an additional iteration, these devices were classified as 'outliers' and hence grouped into different clusters when compared to the majority of other devices in the original cluster. This explained the two devices that were rejected using the threshold approach.

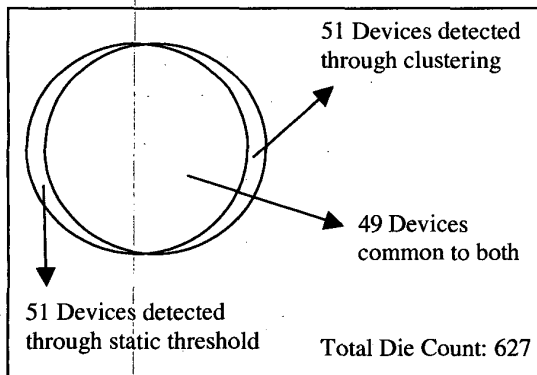


Figure 5: Venn Diagram comparing Clustering Vs. Static Threshold at 5.1 mA

The two devices that were detected using the clustering process alone were devices that exhibited I_{DDQ} measurements for all vectors in the 4.9-5.0 mA region. Since none of these measurements were beyond the threshold value chosen (5.15 mA), these devices escaped detection. These results indicate the flaws associated with the static threshold technique. These devices should have been classified as defective due to the higher I_{DDQ}

currents seen across all vectors. But since all these measurements were below the selected threshold, they escaped detection. The fact that through the clustering process these devices were classified into cluster 2 of figure 2 and thus did not escape detection is very encouraging.

7. Benefits

The main benefits of the proposed clustering technique lie not only in eliminating the need for setting a threshold limit but also in its applicability in the future. The new technique will prove effective even in the presence of high background currents or high current causing states in the design as it is based on considering all the measurements across all devices in a set relative to each other. Though this benefit may be the driving force in thoroughly examining the proposed technique as a viable alternative, there seem to be several other useful advantages to this technique. These include 'binning' of the devices and the cost savings in yield improvement and rapid ramp to volume production efforts.

The benefit of 'binning' devices lies in the classification of a large set of devices into smaller groups based on device quality. This paper does not deal with the aspect of whether devices exhibiting high I_{DDQ} are necessarily bad and should be thrown away. However, the first step in making this determination is to identify those devices. Once that is done, by analyzing a small sub-set of devices, a better understanding of the causes behind the high I_{DDQ} can be obtained. Another possible use is the targeting of devices in the clusters that are in the middle ground, a perfect example is the set of devices in cluster 5 of figure 2, to relatively less critical applications or applications where the amount of current drawn is not a critical factor. For instance, low-end gaming manufacturers are not as concerned about the reliability relative to a manufacturer in the medical application field. Similarly, a manufacturer of cellular phones would consider the power consumed by an IC more important than would a heavy equipment manufacturer. Due to these different concerns of customers, devices from different clusters can potentially be shipped to different customers. This can result in considerable savings for IC manufacturers. Before these observations can be put into practice, however, larger sets of devices have to be analyzed and further proof for the new technique has to be obtained.

Another advantage of the new technique is the savings in time and effort required for failure analysis (FA). This is because rather than performing FA on all failing devices, a representative sample of devices in a cluster can be selected for FA. The results thus obtained can be extrapolated to other devices in the same cluster. This is

especially significant during the ramping up of a new process since a relatively large number of systematic defects, as opposed to random defects, would be present. From the FA reports corrective action can be identified and fed back to make necessary changes during design and/or manufacturing. These will in turn improve the yield in a timely fashion by expediting ramp to volume production and providing cost savings in reduced engineering time and silicon that needs to be scrapped due to process errors.

One of the fortuitous benefits of this technique lies in its applicability to the single threshold approach. In situations where the clustering technique is not a viable option to be implemented into the overall flow due to any reason, it can be used for threshold level determination. As in the comparison that was performed, by clustering an initial set of devices, a clear distinction between defective and defect-free devices can be obtained. By estimating the value at which the same number of devices are classified as defective in the static threshold approach can be found. This value can be used as the threshold level.

8. Conclusions and Future Work

The process of separating a good device from a bad device based on I_{DDQ} has become tricky due to device integration, scaling of device geometries and reduction in threshold voltages (V_T). Hence, it has become necessary to inspect measured I_{DDQ} currents in a relative perspective over a spread of devices rather than comparing with a static threshold value. We have demonstrated that clustering the devices based on measured I_{DDQ} will help accomplish this objective by providing a natural classification of devices.

A process for making judgements based on I_{DDQ} measurements from the test floor was presented. An example of implementing the process on real devices was shown. The traditional single threshold approach treats each vector in isolation, and the current signature approach treats each device in isolation. The goal of our approach in contrast is to identify abnormalities in terms of measured currents for all I_{DDQ} vectors over a set of devices. The proposed approach looks for abnormal current distributions with respect to other devices. In our opinion, such new techniques are needed for the continued use of I_{DDQ} testing in the industry. Using this technique, wafer-wafer and process-to-process dependencies can be accounted for and utilized while accepting or rejecting devices.

We plan on comparing this method to the current signature method by using the same set of data and arriving at device quality predictions. Further, we plan

to apply this technique to data collected from the 'SEMATECH Test Methods Experiment'.

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References

1. L. K. Horning, et al, "Measurements of Quiescent Power Supply Current for CMOS ICs in Production Testing", Proc. of IEEE Int. Test Conf. 1987, pp. 300-309.
2. C. F. Hawkins, et al, "Quiescent Power Supply Current Measurement for CMOS IC Defect Detection", Proc. of IEEE Trans. on Industrial Electronics, 1989, pp. 211-218.
3. K. Baker and B. Verhelst, " I_{DDQ} testing because Zero Defects isn't Enough: A Philips Perspective", Proc. of IEEE Int. Test Conf. 1990, pp. 253-254.
4. S. McEuen, " I_{DDQ} Benefits", Proc. of IEEE VLSI Test Symp. 1991, pp. 285-290.
5. R. Perry, " I_{DDQ} Testing in CMOS Digital ASIC's - Putting it All Together", Proc. of IEEE Int. Test Conf. 1992, pp. 151-157.
6. T. W. Williams, et al, " I_{DDQ} Test: Sensitivity Analysis of Scaling", Proc. of IEEE Int. Test Conf. 1996, pp. 786-792.
7. A. Gattiker and W. Maly, "Current Signatures", Proc. of IEEE VLSI Test Symp. 1996, pp. 112-117.
8. S. Jandhyala, et al, "Clustering Based Identification of Faulty ICs Using I_{DDQ} Tests", Proc. of IEEE Int. Workshop on I_{DDQ} Testing, 1998, pp. 48-53.
9. S. Jandhyala, "Clustering Based Techniques for I_{DDQ} Testing", M.S. Thesis, Colorado State University, 1998.
10. A. Gattiker and W. Maly, "Current Signatures: Application", Proc. of IEEE Intl. Test Conf., 1997, pp. 156-165.
11. M. R. Anderberg, "Cluster Analysis for Application", Academic Press, 1973.
12. B. S. Everitt, "Cluster Analysis", John Wiley, 1993.