EE571 Lab Instructions
SP07

- **Initial environment setup**
  - Setting up the .cshrc file
    - from your home directory backup your current .cshrc file
      - ***cp .cshrc .cshrc_old***
    - from your home directory copy the new .cshrc file
      - ***cp ~joewu/.cshrc .cshrc***
  - Create the directories used for lab work
    - make an EE571 directory for lab work
      - ***mkdir EE571***
    - make directories for all the labs(1-6)
      - ***mkdir EE571/lab1***
  - Copy over the process files need for the lab
    - ***cp -R ~joewu/EE571_TA/process EE571/***

- **Design Architect (DA)** – building the schematic
  - go to the working directory:
    - ***cd EE571/lab1***
  - Source DA: ***d***
  - Run DA: ***da***
  - Create/open a sheet: ***File*** -> ***open -> sheet***
    - in Component Name enter ***inv*** after ...../lab1/
  - To get the parts from library: ***Libraries*** -> ***MGC Analog Libraries*** (will open a new bar at right)
    - transistor: use ***Generic Parts -> NENH4 / PENH4***
  - To unselect : ***F2***
  - To change the properties of transistor: ***select the transistor -> right click -> properties -> modify multiple***
    - INSTPAR : ***L=1.2u W=1.3u***
    - ASIM_MODEL: ***nch.4*** (or ***pch.4***)
  - To modify the port name: ***move the cursor over the name -> shift+F7***
  - Once the circuit is complete, the next step is to make a viewpoint: ***Libraries*** -> ***MGC Analog Libraries ->(right side) M/S Utilities -> Create Viewpoint, and then click OK***

- **Accusim** – export the netlist of the circuit
  - in */EE571/lab1/ run accusim
    - ***accusim inv***
  - To export netlist: ***File -> Write Netlist***
    - enter the path and file name (inv.cir) where you want the netlist to be saved, should be end in *.cir, then click OK
  - Exit accusim ***without saving***

- **Modify the netlist** (please find out what those commands mean in lab webpage or google it)
  - Use text editor to open the netlist (inv.cir)
  - In an ELDO spice netlist, lines start with * are comments and can be deleted
  - Lines start with "Design" or "V_" should be removed
  - The first line of the netlist has to be an empty line
  - ***.LIB ~/EE571/process/log018.eldo53 TT*** has to be added near the top of the netlist
  - Add the electrical source defination:
    - ***v0 GND 0 DC 0***
    - ***vcc VCC GND DC 1.8***
  - Add the input signal:
    - ***v1 in GND pwl(0 1.8 5n 1.8 5.01n 0)*** or
    - ***v1 in GND pulse(0 1.8 0 0.01n 0.01n 5n 10n)***
  - Set the transient simulation:
    - ***.trans 0.1n 10n*** (step size and length of simulation)
  - Add a plot: ***.plot v(in) v(out)***
  - Add a measurement: ***.extract label=tr (xthres(v(out),1.62,1) – xthres(v(out),0.18,1))***
  - Add ***.end*** at the end of the netlist

- **esim –** simulate the circuit
  - Source eldo: ***e***
  - Run esim: ***esim***
  - It will open a new window, click the diamond next to ELDO, and double click the file (*.cir) you want to simulate
  - The result window will show all the information about the simulation
  - use ***XELGA*** to view the wave(s) (open the *.cou)

- **IC Station** (IC) – draw the layout for the circuit
  - Source IC: ***i***
  - Run IC: ***ic***
  - Once started need to set the process
    - ***File -> Process -> Load*** : then browse EE571/process to choose ***Tsmc018***
  - To open a new cell:
    - ***File -> Cell -> Create***
      - Cell name is the path and the name of the cell
      - Process is the same process as above
  - To set the grid:
    - type ***set grid***
    - make sure ***Snap Grid On*** is checked and enter ***.01*** for both Snap X and Y
  - Edit:
    - ***Easy Edit -> Shape*** (will open a small box in the lower left corner), in the small box choose options to choose the type of layer you want to put down
    - Once a layer is laid down, you must press **F2** to unselect the layer
    - There are other options that you can choose from the Easy Edit objects that you can explore on your own, some like Path, Text will make things easier in the long run