# IC Instructions for DRC checks and Netlist Extraction
# SP07

**Note:** This instruction will not work for the JAVA consoles!!

**Adding Text:**
Select the layer you wish to add text to, this will be done for VDD, GND, INPUTS, and OUTPUTS.
Type the name of the label in the box that appears in the lower left box, then you can change the size of the font under the options menu, the place the text on the **appropriate layer**, and then click ok.

**DRC Rule Checks:**
Write the gds file to use as an input: **Translate->Write GDSII**
- make sure cell name is in the first box.
- **Output GDS File => enter your_cell_name.gds**

Then run the DRC checks: **Calibre->Run DRC**
-if Setup Calibre box appears browse to: **/mentor/ICFlow_2003.2/ss6_cal_2003.2_19**
-this should bring up the DRC window:
-new runset, unless you have saved one.
-Rules: **Calibre-DRC Rules File**: browse to your process folder and get the file called: **JLG018.drc** then click load.
-Inputs: Layout-> File name should be the gds file created above.
-Run DRC: this will then bring up the Calibcre DRC RVE window, where you can double click on the errors and it will highlight them in your layout.

Once all your errors are fixed, you next need to extract the netlist and the parasitics.

**PEX:**
Download the **xcalibre rules** from the EE571 main website page
-you may save this in your process folder since you will need one for each layout that you do.

You need to edit this file and replace everywhere it says **YOUR_LAYOUT** with the name of your layout and also **replace the word ELDO on line 52 with HSPICE**, then save this file in the directory that contains your layout files. This step will need to be done for each layout that you do.

Now, in IC go to **Calibre->Run PEX**

- new runset, or you can load one if you have one saved
- Rules: Calibre-PEX Rules File => browse to the file that you edited above, click load.
- Inputs: check the diamond next to: Calibre-XRC, under the Layout tab: Files => should be your gds file (ie your_cell_name.gds)
- Outputs:
  Netlist Type should be **RCC** under the netlist tab,
  Format should be **HSPICE,**
  Names should be **Layout,**
  File should be the name of your_cell_name.net).
- Run Control:
  Under Calibre-PEX Settings: select **run 64-bit version of PEX**
- Run PEX:
  This should bring up the extracted netlist, be sure that all the transistors are defined and all the Inputs, Outputs, VDD, and GND are defined.

We need to run a script to clean up the extracted netlist:

- download ***ext.pl*** from EE571 website
- in the directory which contains the extracted netlist(*.net), run
  **- *perl* *ext.pl*** your_cell_name***.net***
- the clean netlist is in *.out (your_cell_name.net.out)
- check the numbers of transistors in your design, as well as the node names

Then you will do the same steps that you did to the DA netlist, once this is complete you can run the netlist through ELDO and get the needed data.