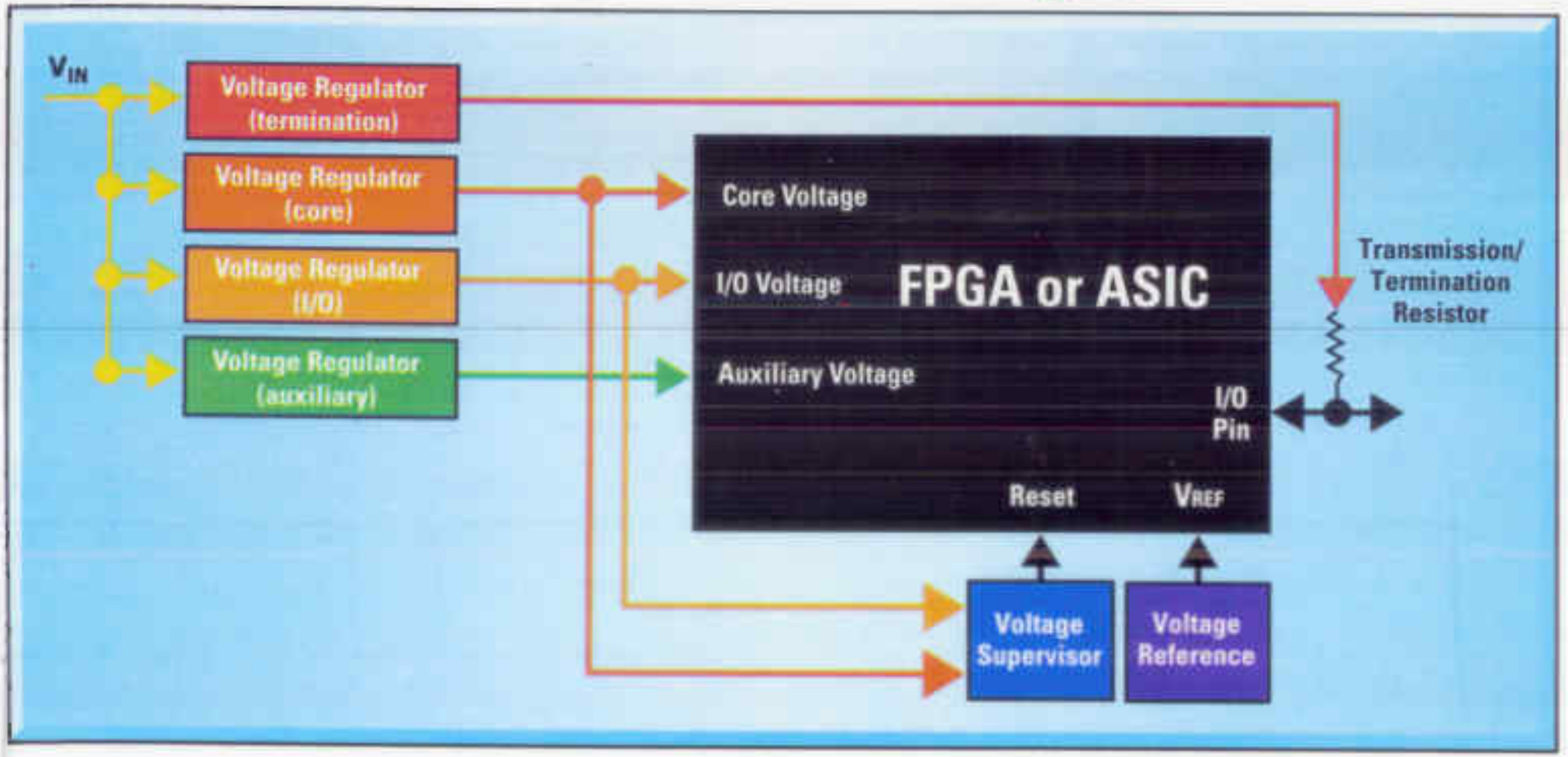
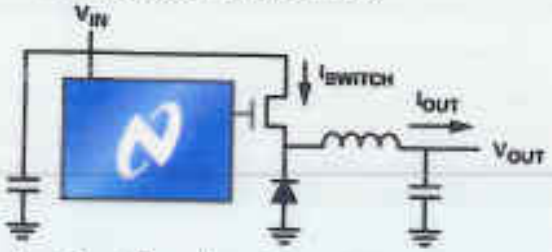


Figure 1: Typical FPGA or ASIC power management requirements

Power Management Considerations for FPGAs and ASIC

Non-synchronous buck



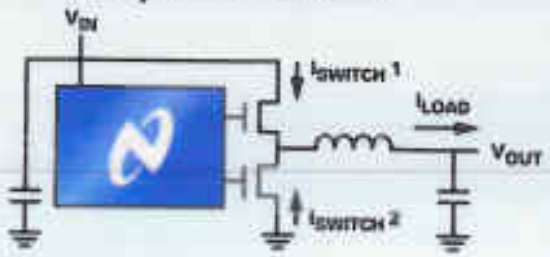
Function: Step-down ($V_{OUT} < V_{IN}$)

When to use: Typically when V_{IN} is 3x to 5x V_{OUT} and I_{OUT} is > 0.5A and < 5A

Characteristics: Easy to design and good efficiency for the above-mentioned typical $V_{IN}/V_{OUT}/I_{OUT}$ conditions

Devices to use: All buck integrated regulators and controllers

Synchronous buck



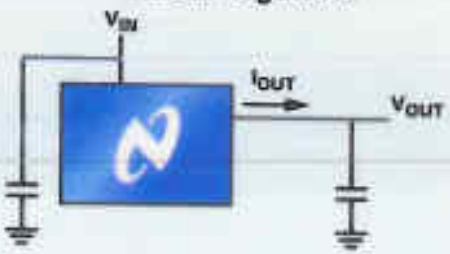
Function: Step-down ($V_{OUT} < V_{IN}$)

When to use: When high efficiency is required with high-output current (> 5A) or low duty cycles ($V_{IN} > 5 \times V_{OUT}$ and/or $I_{OUT} < 0.5A$)

Characteristics: A second switch replaces the diode in the basic buck topology, reducing losses in the conditions mentioned above

Devices to use: Any "synchronous rectification" buck integrated regulator or controller

Linear regulator



Function: Step-down ($V_{OUT} < V_{IN}$)

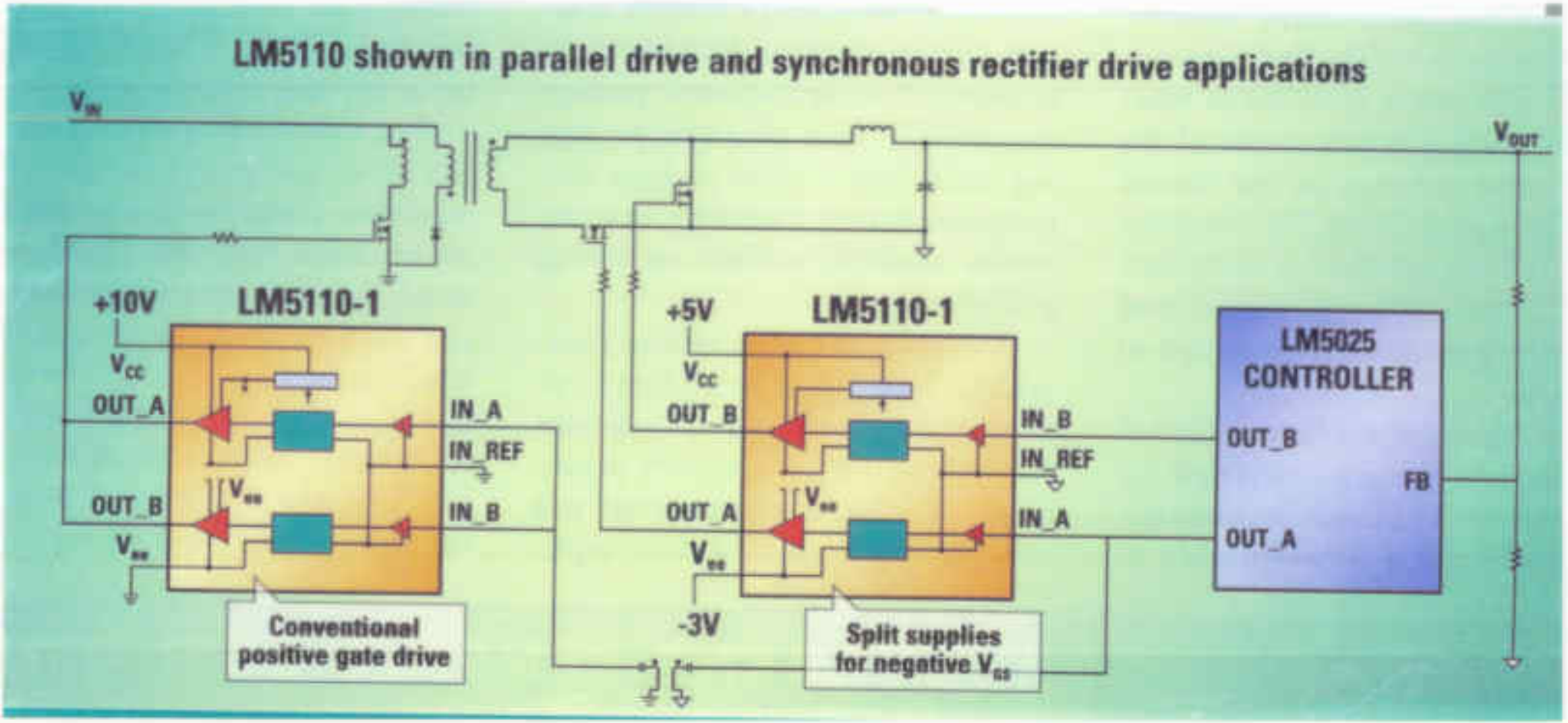
When to use: Typically when $I_{OUT} < 1A$, ultra low-dropout, and low-noise applications

Characteristics: Excellent option where fixed output, low current, and low voltage drops are required. Easy to implement

Devices to use: Any low-dropout, linear regulator

Comments: Great for micropower applications

Figure 2: Step-down configurations


LM5110 shown in parallel drive and synchronous rectifier drive applications
V_{IN}
V_{OUT}
+10V
LM5110-1
V_{CC}
OUT_A
OUT_B
V_{EE}
IN_A
IN_REF
IN_B
Conventional positive gate drive
+5V
LM5110-1
V_{CC}
OUT_B
OUT_A
V_{EE}
IN_B
IN_REF
IN_A
-3V
Split supplies for negative V_{GS}
LM5025 CONTROLLER
OUT_B
FB
OUT_A

- Each channel can sink/source 5A /3A for very fast rise/fall times (20 ns/10 ns into a 2 nF load)
- Short propagation delay times (25 ns typical)
- Integrated under voltage lockout protection (2.8V typical)
- Shutdown pin disables drivers for low-power standby mod
- Offered in three industry standard configurations: dual non-inverting, dual inverting, and one inverting & one non-inverting

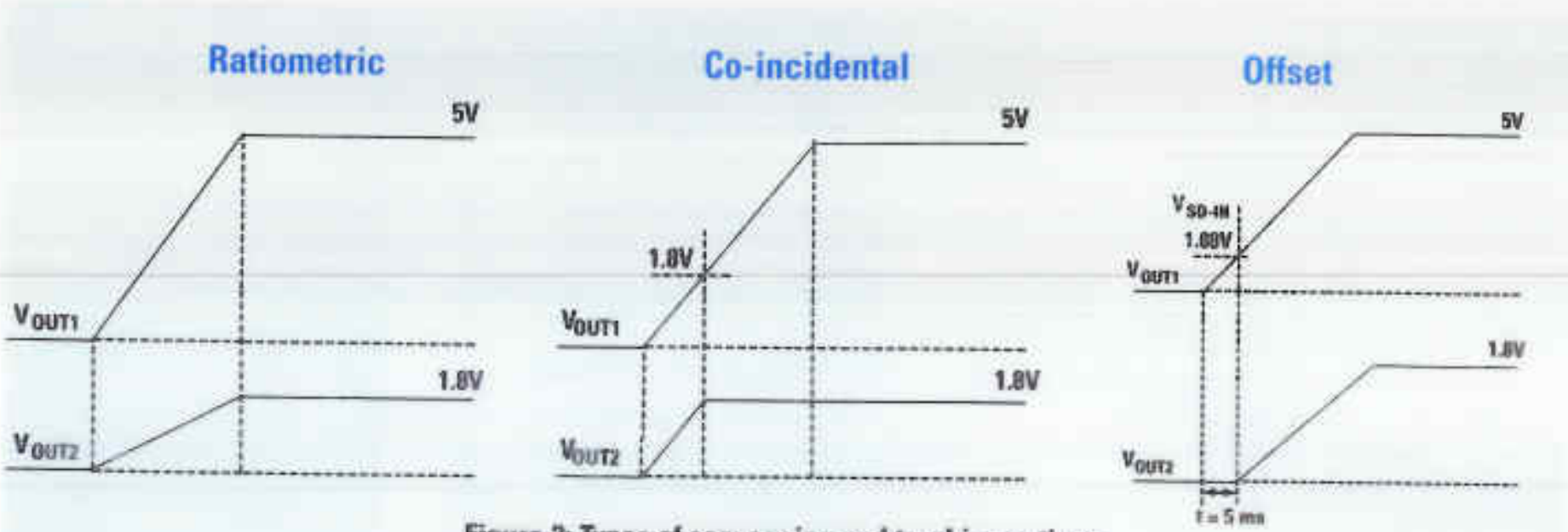
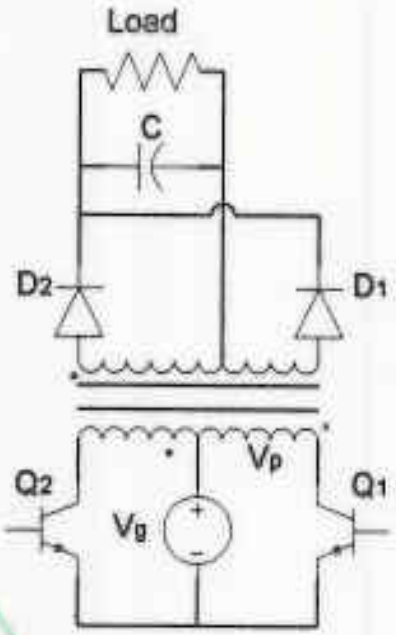


Figure 3: Types of sequencing and tracking options

the two phases can be made to operate out-of-phase, the RMS ripple current in the input capacitor

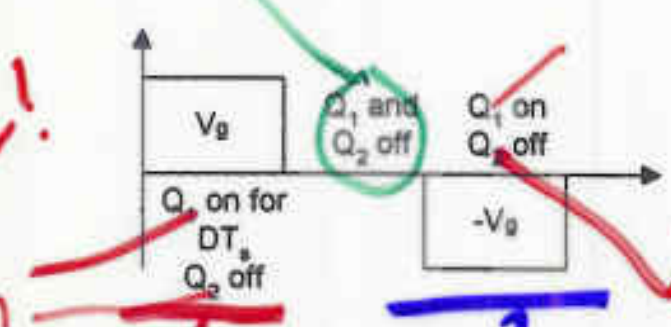
simply or flexibly implemented if the regulators

3. Push-Pull Transformer Balance Problem



To monitor SATURATION of Transformer Core we will employ current sensors in Q_1 and Q_2 collector's to look for high current spikes.

We compare to $I_{control(ref)}$ and we shut off Q_1 and/or Q_2 if $I > I_{control}$.



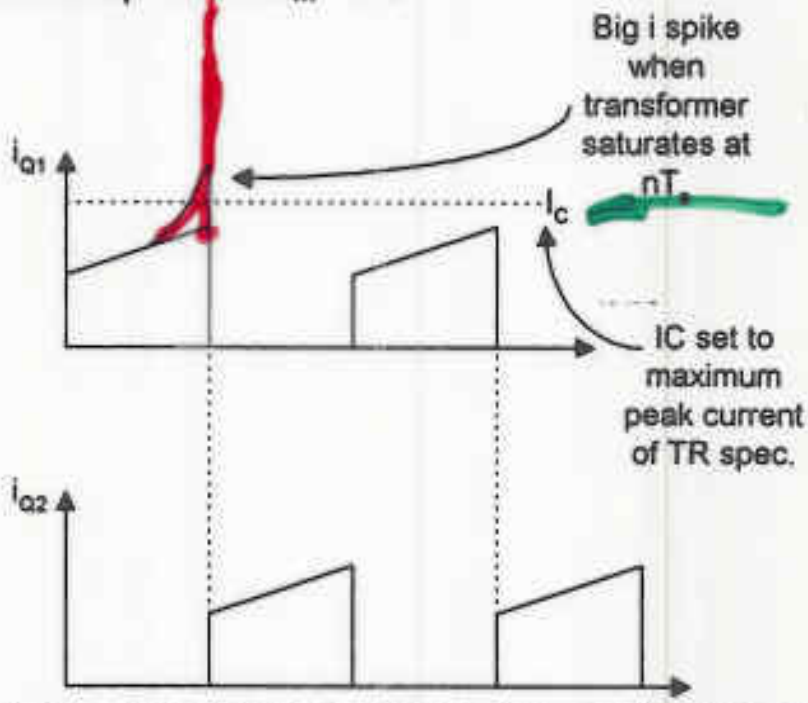
$$i_{Lm} = \frac{\int V_{Lm}\,dt}{Lm} \neq 0 \text{ over } Ts$$

Due $V_{on}(Q_1) \neq V_{on}(Q_2)$ and $\Delta t\,(Q_1) \neq \Delta t(Q_2)$ we might have a slight offset each clock cycle and i_{Lm} is not zero.

$V_{on}(Q_1) = V_{on}(Q_2)$?

Q death by i spike

Even a small imbalance adds up after 100 switch periods and the transformer will ultimately saturate. Then for example the current on $i(Q_1)$ will shoot up when $L_m \rightarrow 0$



Safe limit of Q

Use I_c(control) as a maximum to sense if i_{Q1} gets excessive and shut it down if it does. In practice we never build push pull converter with duty cycle control and voltage. Rather we use current programmed control of Chapter 11. Below we compare switch stress in the topologies of lectures 15 and 16.

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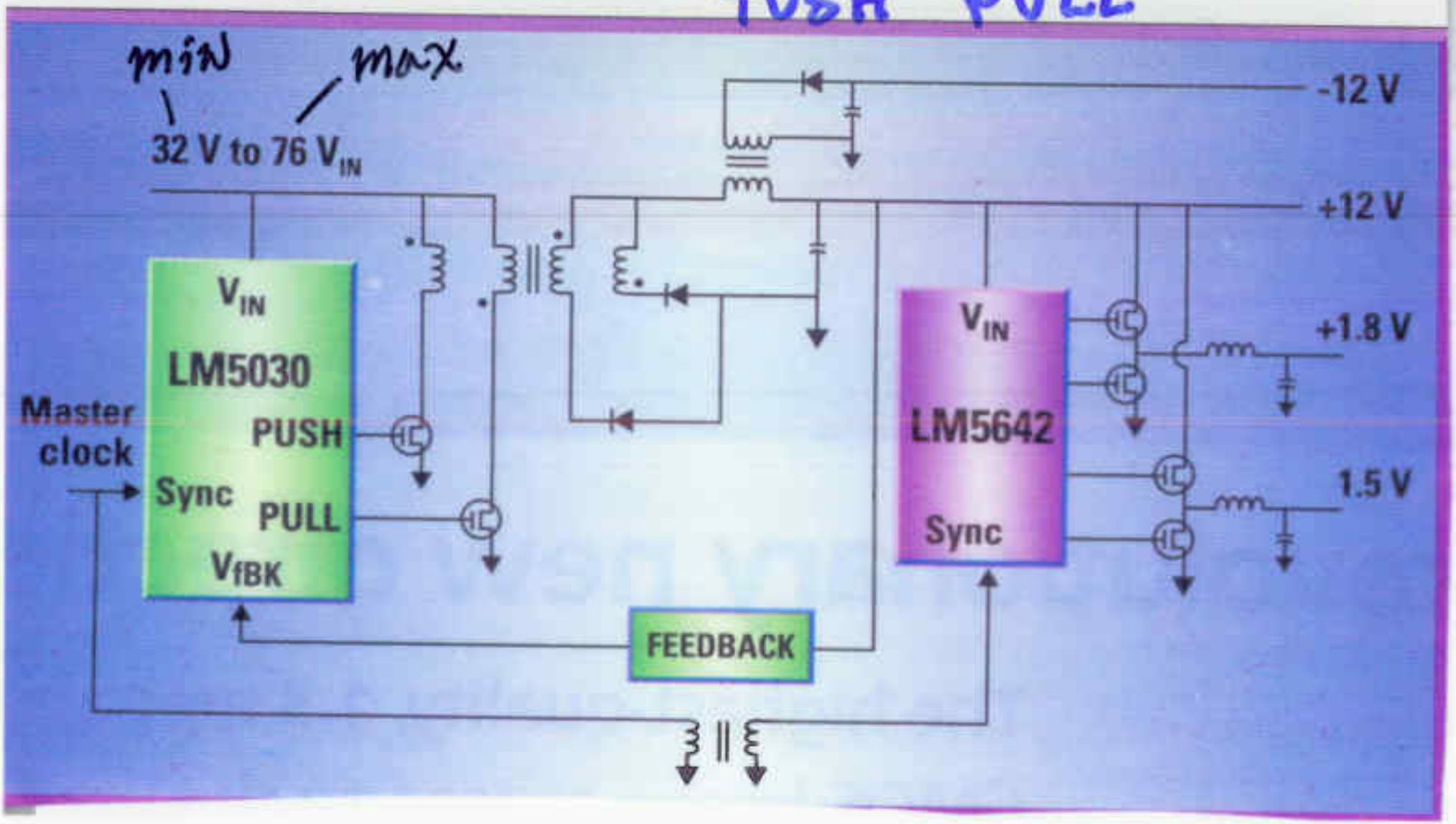
Final Solution to V_{DC} across "2"

DSL Line Card: -48 V multi-output isolated pow

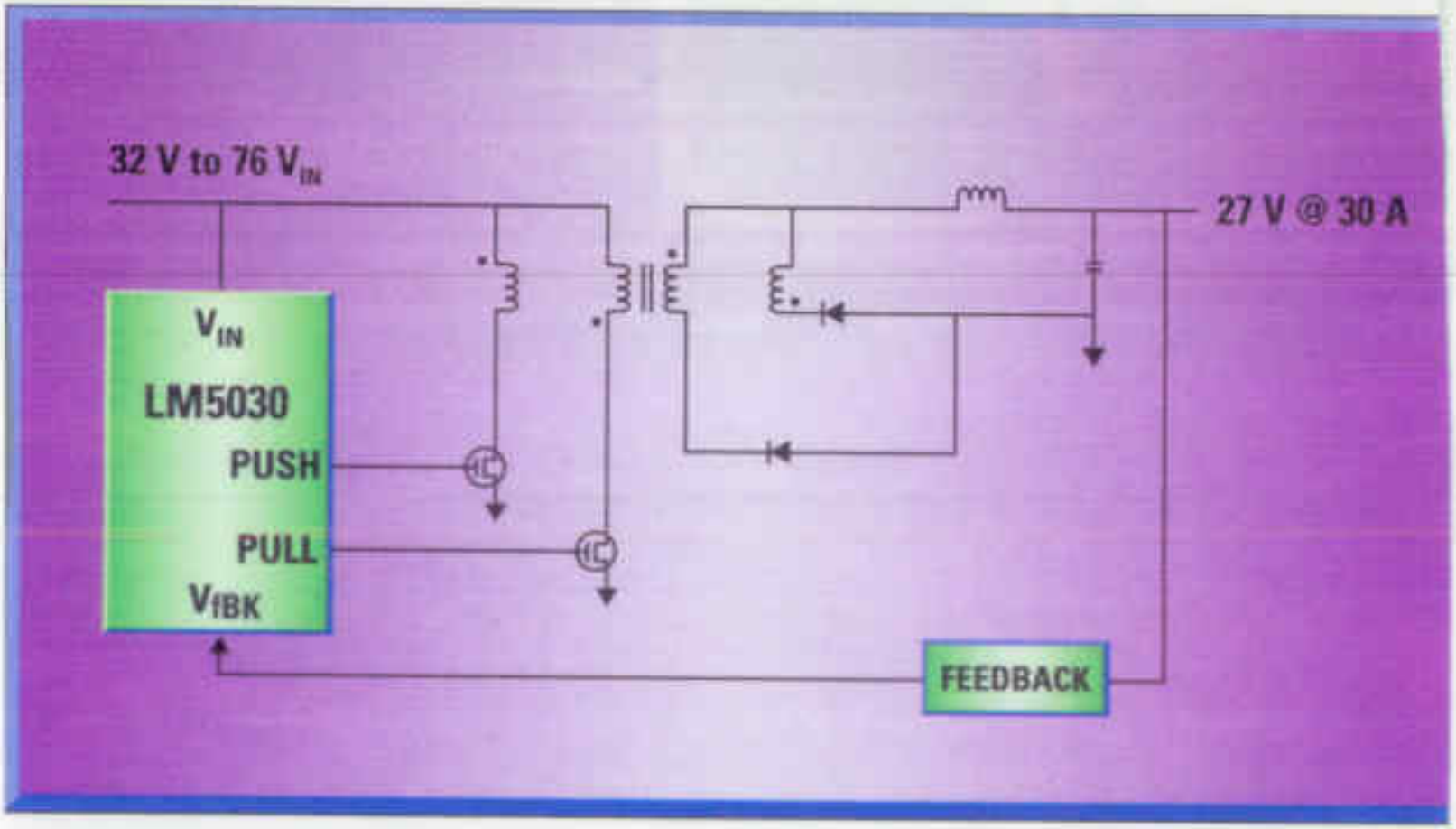


r supply

Primary controller: LM5030 100 V current-mode
Secondary controller: LM5642 dual synchronous bu

- 48 $V_{IN,}$ multiple outputs ±12 V, 1.8 V, and 1.5 V_{OUT}
- High efficiency >90%
- Tight regulation <2%
- Oscillators synchronized to a master clock
- User-programmable softstart and power on/off sequenc
- Available separately or together:
  - LM5030 (MSOP-10)
  - LM5642 (TSSOP-28)

3G Basestations: 850 W Push-Pull DC/DC co



LM5030

- Fully integrated LM5030 includes: high bandwidth error amp, precision reference, programmable softstart, and dual-mode current sense
- Internal high-voltage (100 V) start-up regulator

Primary controller: **LM5030 100 V current-mode Push-Pull**

Secondary controller: **LM5642 dual synchronous buck**

- 48 $V_{IN,}$ multiple outputs ±12 V, 1.8 V, and 1.5 V_{OUT}
- High efficiency >90%
- Tight regulation <2%
- Oscillators synchronized to a master clock
- User-programmable softstart and power on/off sequencing
- Available separately or together:
  - LM5030 (MSOP-10)
  - LM5642 (TSSOP-28)

First we review the switch stress of the push-pull compared to the half and full bridge covered earlier.

Estimating the Significant Minimum Parameters of the Power Semiconductors

	Bipolar Power Switch		MOSFET Power Switch		Rectifier(s)	
Topology	V_{ceo}	I_c	V_{oss}	I_D	V_R	I_F
Push-pull	$2V_{in}$	$\frac{1.2P_{out}}{V_{in(min)}}$	$2V_{in}$	$\frac{1.2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}
Half-bridge	V_{in}	$\frac{2P_{out}}{V_{in(min)}}$	V_{in}	$\frac{2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}
Full-bridge	V_{in}	$\frac{1.2P_{out}}{V_{in(min)}}$	V_{in}	$\frac{1.2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}

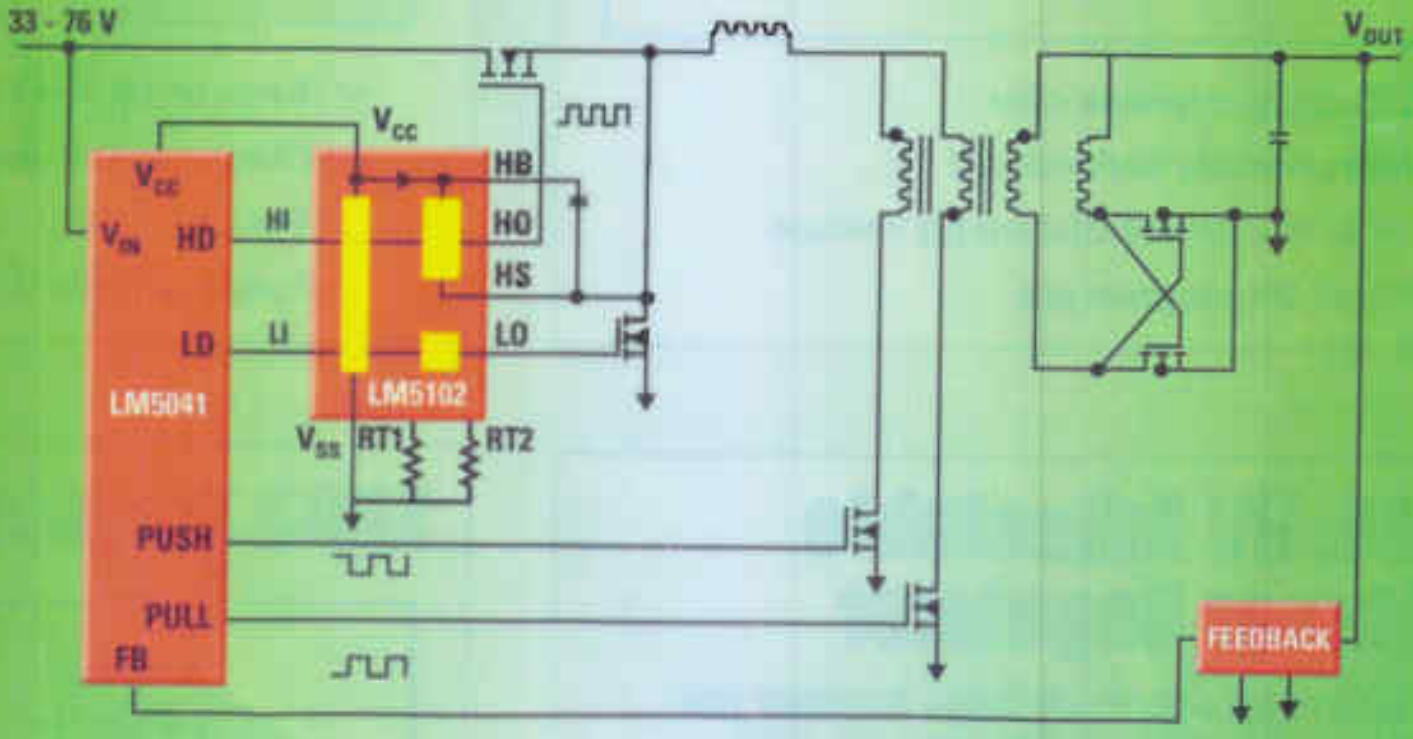
Note that the push-pull is equivalent to the full bridge in switch stress and better than the half bridge. However, the push-pull is a dangerous circuit as it has a tendency towards core saturation which will cause the transformer input to look like a short and will likely kill the switches. This arises when the flux within the core is inadvertently non-symmetric so that a small DC offset occurs. Unfortunately, this small offset will cause a walk towards saturation over many switch cycles. Usually, current mode feedback must be employed rather than voltage feedback to control this difficulty of push-pull. Also possible, is active core re-balancing as illustrated on the next page.

New cascaded controller/100 V driver "chipset" family

Configuration	Voltage-fed or current-fed	Controller	Driver(s)	Benefits/ applications
Cascaded push-pull	Voltage-fed	LM5041	LM5102	High efficiency/ medium power
Cascaded push-pull	Current-fed	LM5041	LM5102	High efficiency/ medium power
Cascaded half-bridge	Voltage-fed	LM5041	LM5102 & LM5100	High efficiency/ medium to high power
Cascaded full-bridge	Current-fed	LM5041	LM5102 & (2) LM5100	High efficiency/ high power

Flexibility for multiple configurations: interleaved forward, cascaded push-pull, half-bridge, and full-bridge

LM5041 typical application



Estimating the Significant Minimum Parameters of the Power Semiconductors

	Bipolar Power Switch		MOSFET Power Switch		Rectifier(s)	
Topology	V_{CEO}	I_C	V_{DSS}	I_D	V_R	I_F
Flyback	$1.7V_{in(max)}$	$\frac{2P_{out}}{V_{in(min)}}$	$1.5V_{in(max)}$	$\frac{2P_{out}}{V_{in(min)}}$	$10V_{out}$	I_{out}
One Transistor Forward	$2V_{in}$	$\frac{1.5P_{out}}{V_{in(min)}}$	$2V_{in}$	$\frac{1.5P_{out}}{V_{in(min)}}$	$3V_{out}$	I_{out}
Push-pull	$2V_{in}$	$\frac{1.2P_{out}}{V_{in(min)}}$	$2V_{in}$	$\frac{1.2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}
Half-bridge	V_{in}	$\frac{2P_{out}}{V_{in(min)}}$	V_{in}	$\frac{2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}
Full-bridge	V_{in}	$\frac{1.2P_{out}}{V_{in(min)}}$	V_{in}	$\frac{1.2P_{out}}{V_{in(min)}}$	$2V_{out}$	I_{out}

Whoa! flyback rectifier is hard to diodes

Whoa! needs new HV FETS

Whoa! 1/2 Bridge sucks & needs new FETS

700V MOSFET and controller on IC

$I_{out} = 0$ P_{IN} < 1.3W

Output V-I

New Ei Law

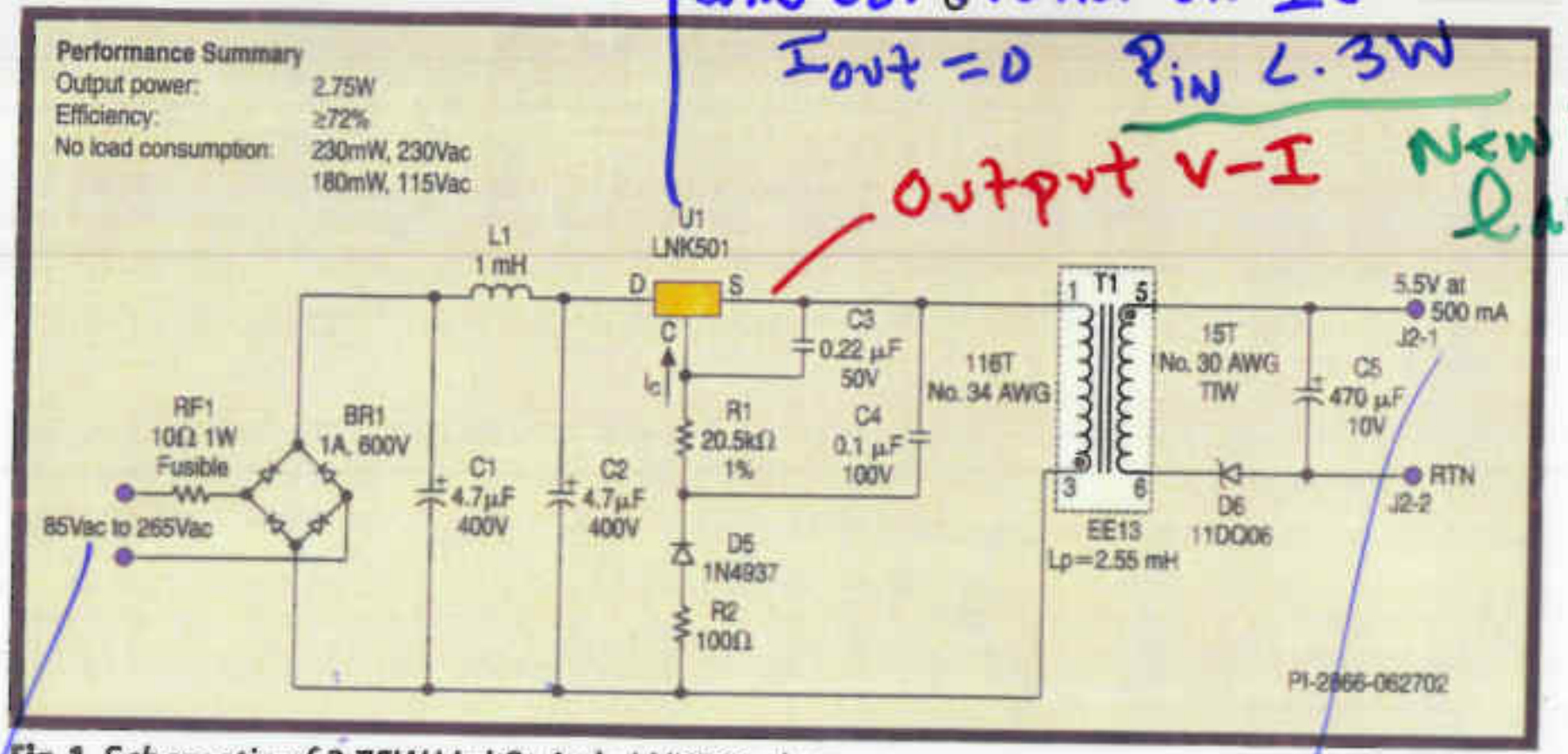


Fig. 1. *Schematic of 2.75W* LinkSwitch *LNK501 charger.*

Universal Input

Battery Charger

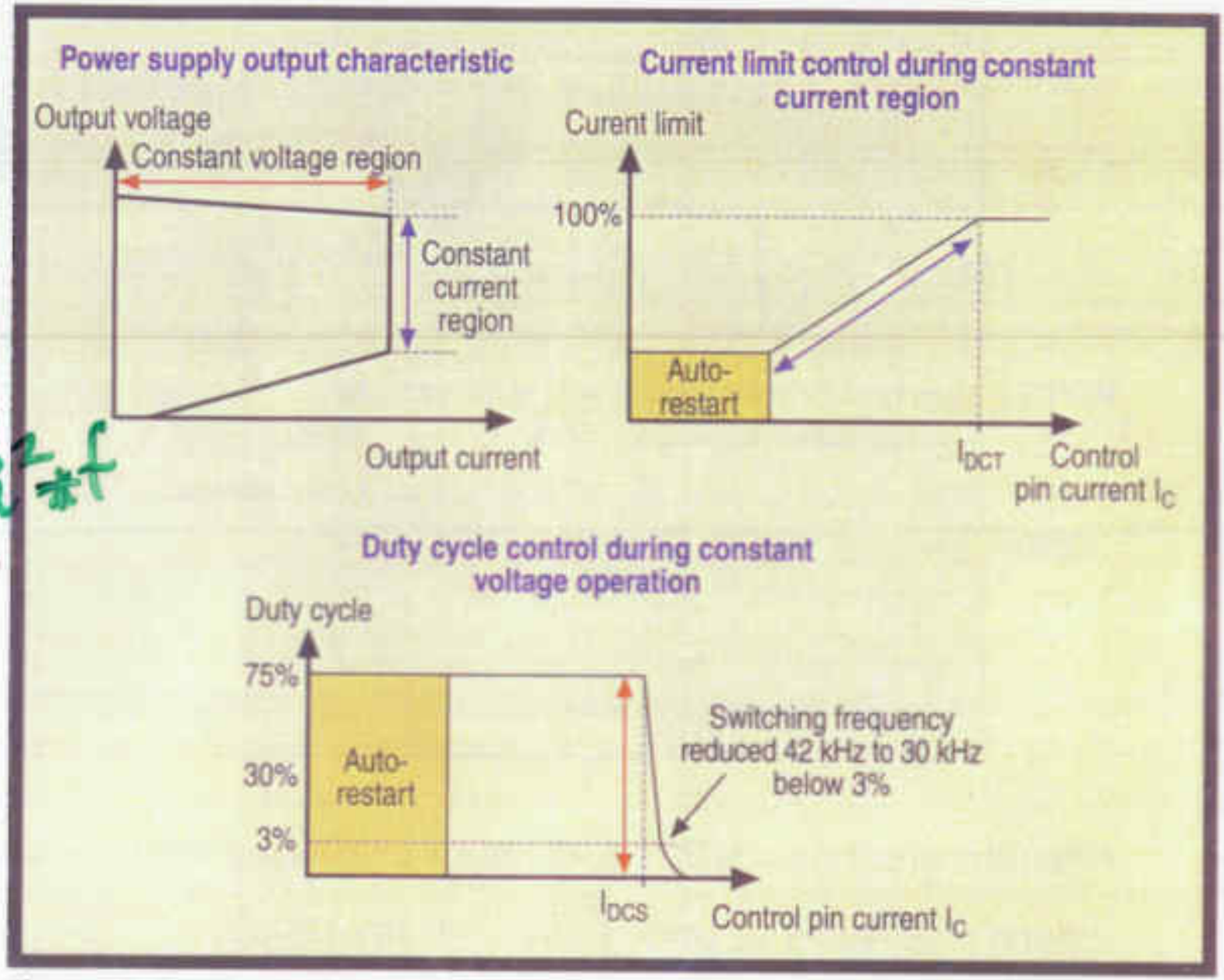


Fig. 3. LinkSwitch *Control pin characteristic provides both duty cycle and current limit control to generate a CV/CC output.*

$V_{IN} = 115$ ac P_{IN} L 200 mW

$I_L = 0$ $V_{IN} = 230$ ac 250mW

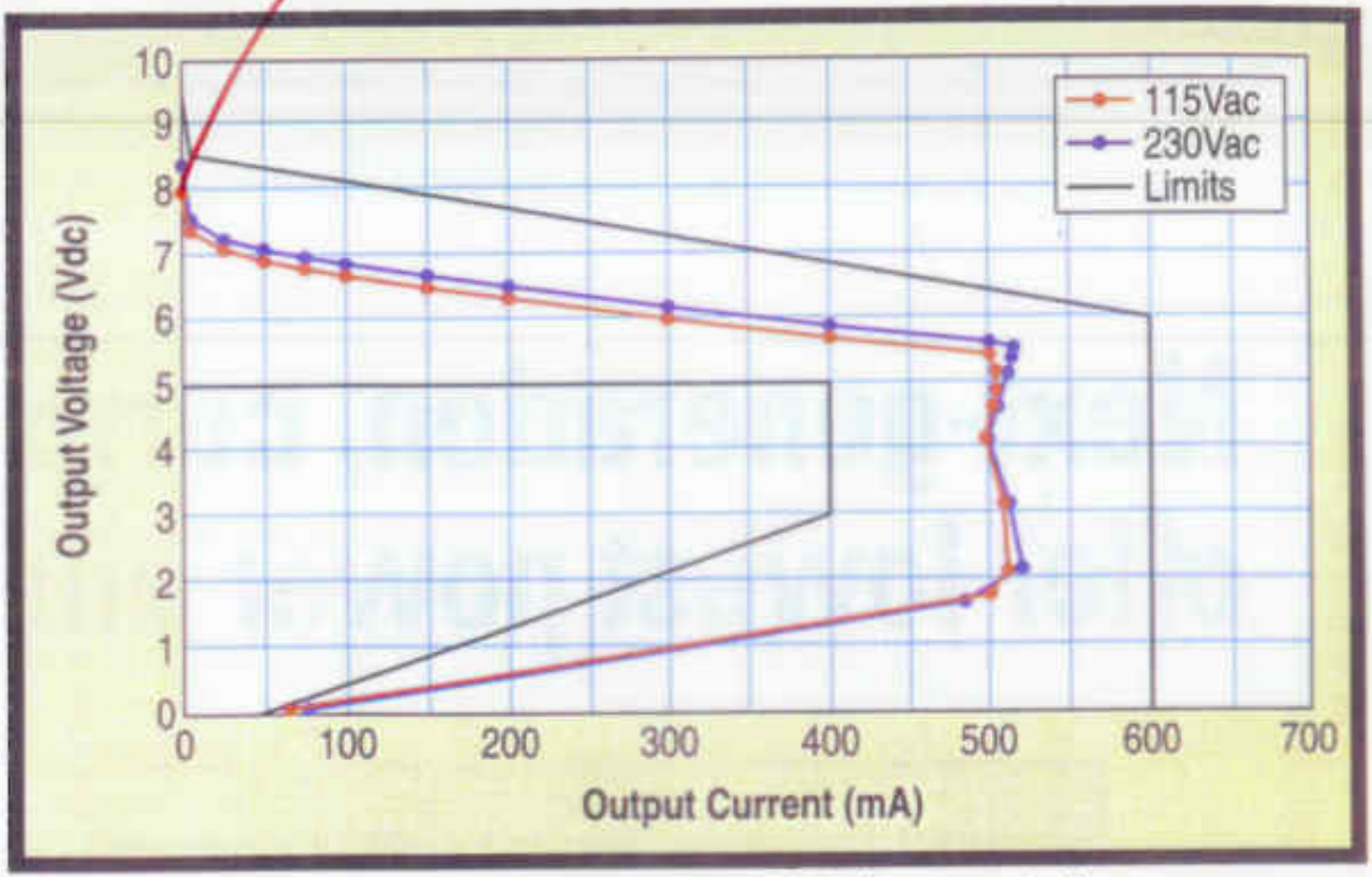


Fig. 2. *Typical* LinkSwitch *charger output VI characteristic.*