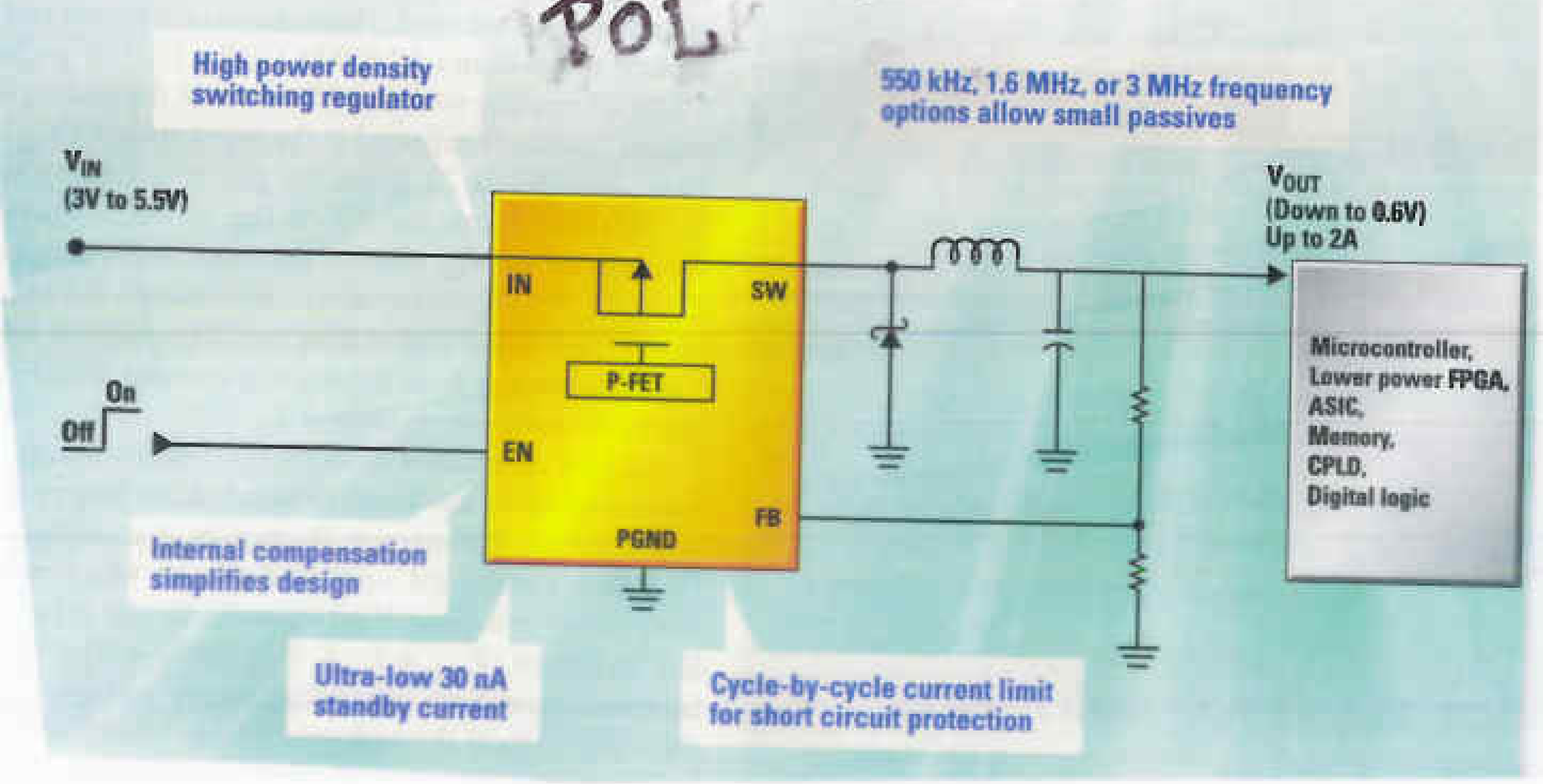
System Power Configuration

POL



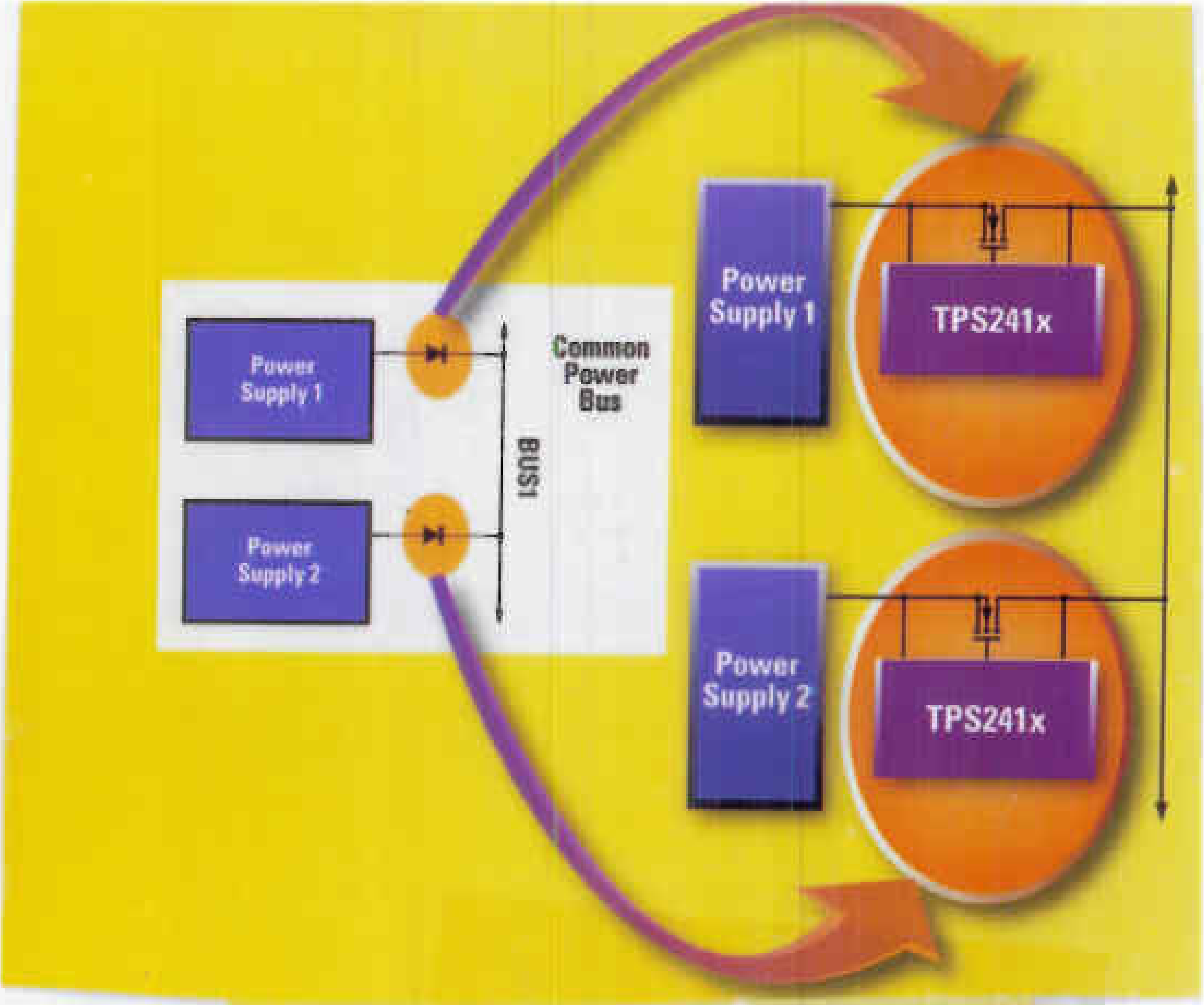
High power density switching regulator

550 kHz, 1.6 MHz, or 3 MHz frequency options allow small passives

Internal compensation simplifies design

Ultra-low 30 nA standby current

Cycle-by-cycle current limit for short circuit protection



Applications

- Blade servers
- N+I redundant systems
- Telecom line cards
- RAID
- Merchant power

Features

- Ultra-fast, adjustable gate turn-off
- Internal charge pump
- Wide voltage operation range
- Adjustable turn-off threshold
- Complements TI's TPS2490 hot swap controller

Common
Power
Bus

5. Comparison of PWM Converters

We now compare the old big three converters (buck, boost and buck-boost) to five new converter topologies that we will be introducing in lectures 14-16. All of the new five topologies will have transformer isolation.. Moreover, as we will see each new topology has a specific power range over which it works best. Below we list converters in ascending order of the power level they can handle as well as the voltage levels. In general, the higher power and voltage level topologies have 2-4 switches rather than the single switch of the big three topologies.

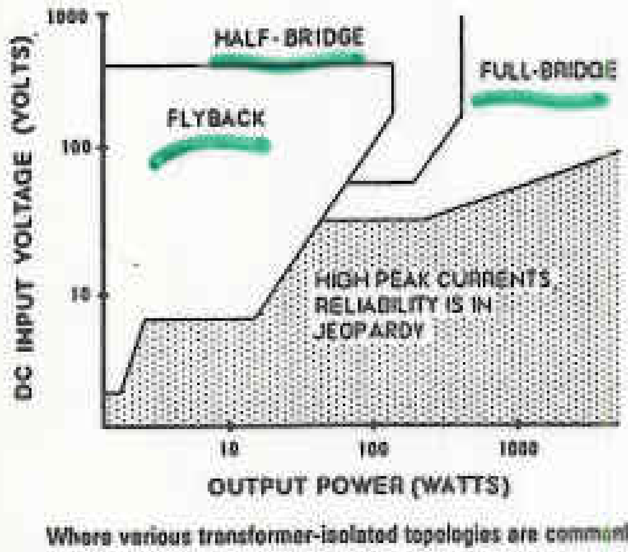
Comparison of the PWM Switching Regulator Topologies

Topology	Power Range (W)	$V_{in(dc)}$ Range	In/Out Isolation
Buck	0–1000	5–1000	No
Boost	0–150	5–600	No
Buck-boost	0–150	5–600	No
Half-forward	0–150	5–500	Yes
Flyback	0–150	5–500	Yes
Push-pull	100–1000	50–1000	Yes
Half-bridge	100–500	50–1000	Yes
Full-bridge	400–2000+	50–1000	Yes

old

New Ch 6

Conversion @ 20KW with new IGBT switches

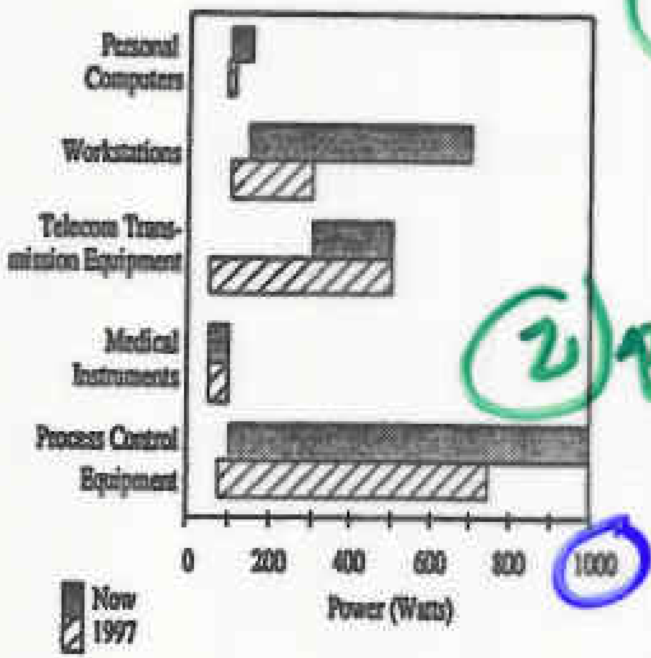


Where various transformer-isolated topologies are commonly used.

All 3 introduced in Ch6

My 562 Web notes

L16



① < 1KW
Buck, Boost, Buck / Boost
flyback

② Big 3 $
Bridges
1KW
10KW —
20KW —

③ Bridges
50KW
200KW

As the power level changes we also will need to determine which of the big eight PWM converter topologies is best suited to the required power level. Choice of PWM topology will in turn determine the switch stress experienced by the power switches. Moreover, the timing sequence for driving the various topologies will also vary. In particular, we will cover both switches drives at f_{sw} and switches synchronized at ½ x f_{sw} in our discussions below. On the next page we briefly summarized what we learned in lecture 11 as regards switch topology and power as well as voltage and current levels in the associated switches.

GH

Gather needs

When selecting a device for the application, it is important to understand the following requirements of the design.

- Output voltage level and regulation needed - is the output protected from surges ? what maximum output voltage protection is required ?
- Output load dynamics such as microprocessor load that changes with various states of the processor.
- Efficiency requirements - will the input source be large reservoir like line power ? or is it a battery that will it be charged often ? or is it a limited supply battery that must be managed well ?
- Other considerations of the input supply e.g. variation of the input supply - is it a battery ? is it simple stepped down AC line with lot of ripple ? what is the output impedance of the supply source ? how far is it from the power solution ?
- Physical and environmental issues - e.g. any height limitations ? how is the ventilation for taking away heat ? area available for the power solution ? what is the ambient temperature of operation ? what are the manufacturing requirements e.g. surface mount vs through hole, PCB line, contact limitations, Lead-free, solder reflow temperatures etc. ?
- Finally the cost available to implement the power solution and relative merits of all of the above.

1-40 Kw

In lectures 16 and 17 we will cover the last of the big eight topologies. We need to employ these circuits to achieve kW power operation. With topology comes different switch stress. That is as the input voltage changes we use different topologies as shown below. The flyback has low parts count but high peak currents than those in a forward converter. The half bridge reduces switch voltage stress because only ½ the V_{in} appears across the primary winding. The full bridge requires four switches, two of which require floating gate drive. The push-pull, as we will see below, also works but has a danger of CORE SATURATION. This could cause us to fry the switch if not careful to balance the core so that no imbalances or DC levels occur.

Comparison of the PWM Switching Regulator Topologies

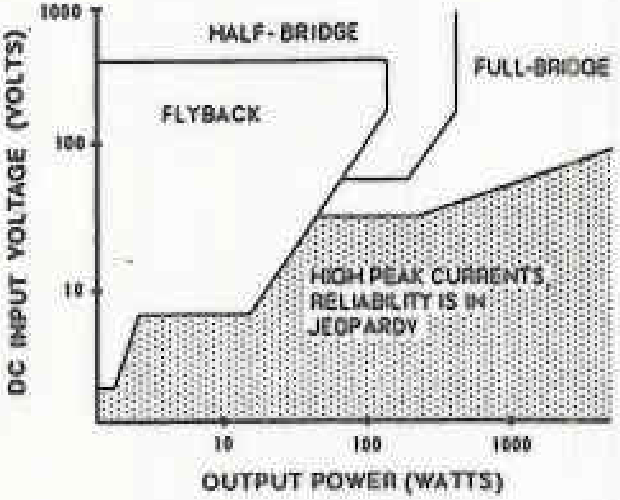
Topology	Power Range (W)	$V_{in(dc)}$ Range	In/Out Isolation
Buck	0–1000	5–1000	No
Boost	0–150	5–600	No
Buck-boost	0–150	5–600	No
Half-forward	0–150	5–500	Yes
Flyback	0–150	5–500	Yes
Push-pull	100–1000	50–1000	Yes
Half-bridge	100–500	50–1000	Yes
Full-bridge	400–2000+	50–1000	Yes

New

3

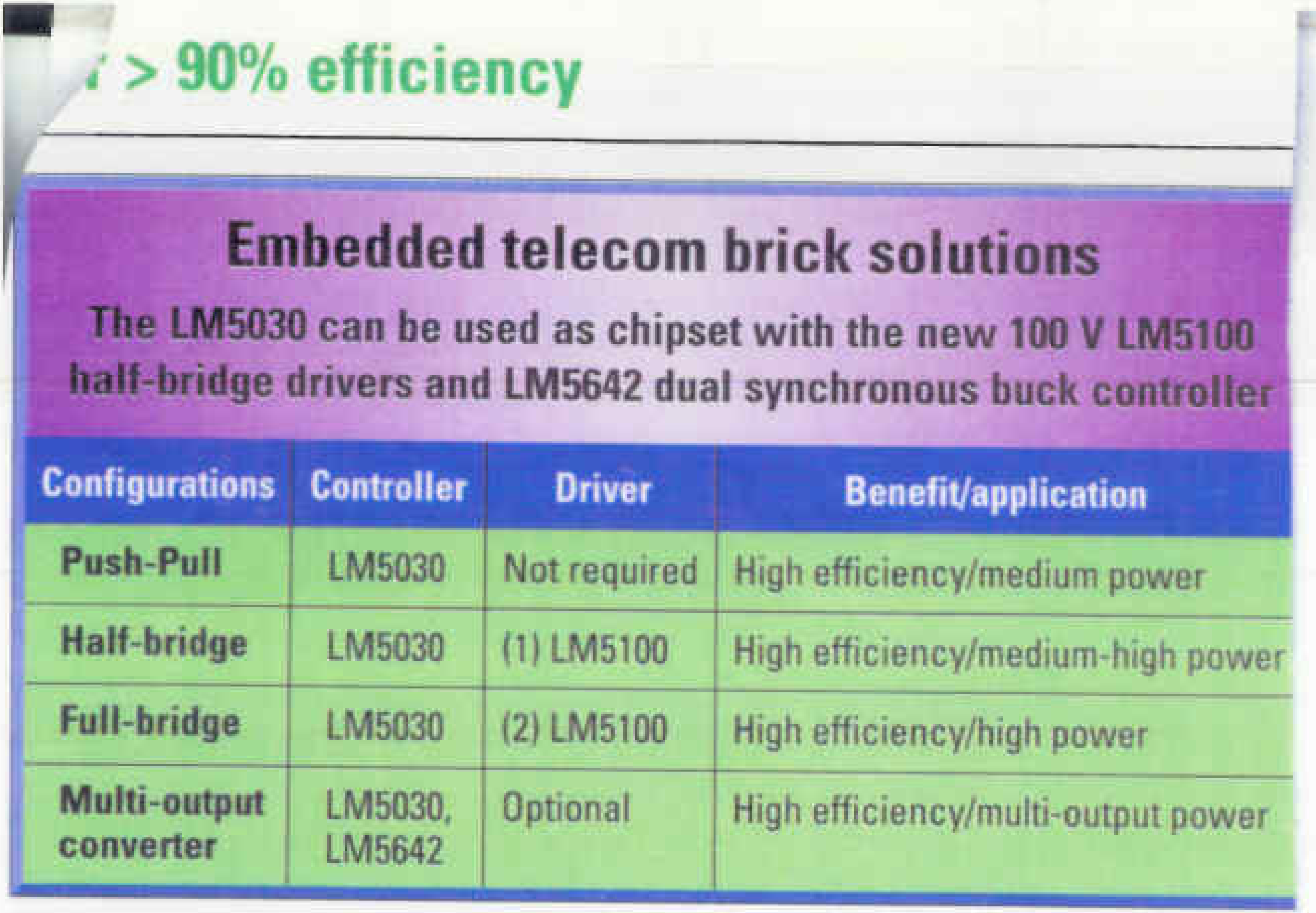
① CAN make a Buck @ 20kW with IGBT

② can do DC up to 200 kW



Where various transformer-isolated topologies are commonly used.

why high V for high power?



> 90% efficiency

Embedded telecom brick solutions

The LM5030 can be used as chipset with the new 100 V LM5100 half-bridge drivers and LM5642 dual synchronous buck controller

Configurations	Controller	Driver	Benefit/application
Push-Pull	LM5030	Not required	High efficiency/medium power
Half-bridge	LM5030	(1) LM5100	High efficiency/medium-high power
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Multi-output converter	LM5030, LM5642	Optional	High efficiency/multi-output power

- Single resistor oscillator setting
- Synchronizable to external clock
- 1 A sink/source drivers
- Thermal shutdown

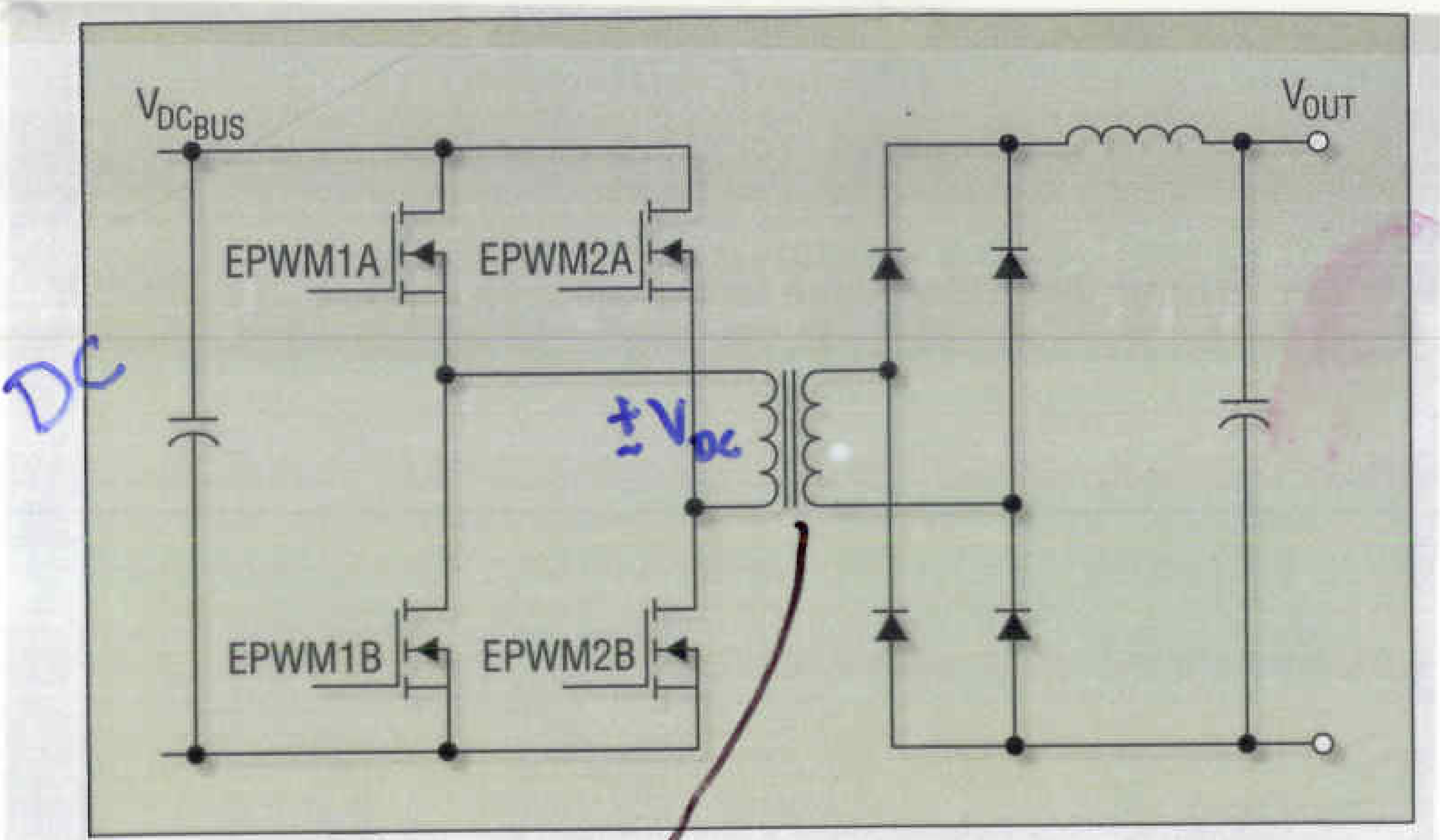
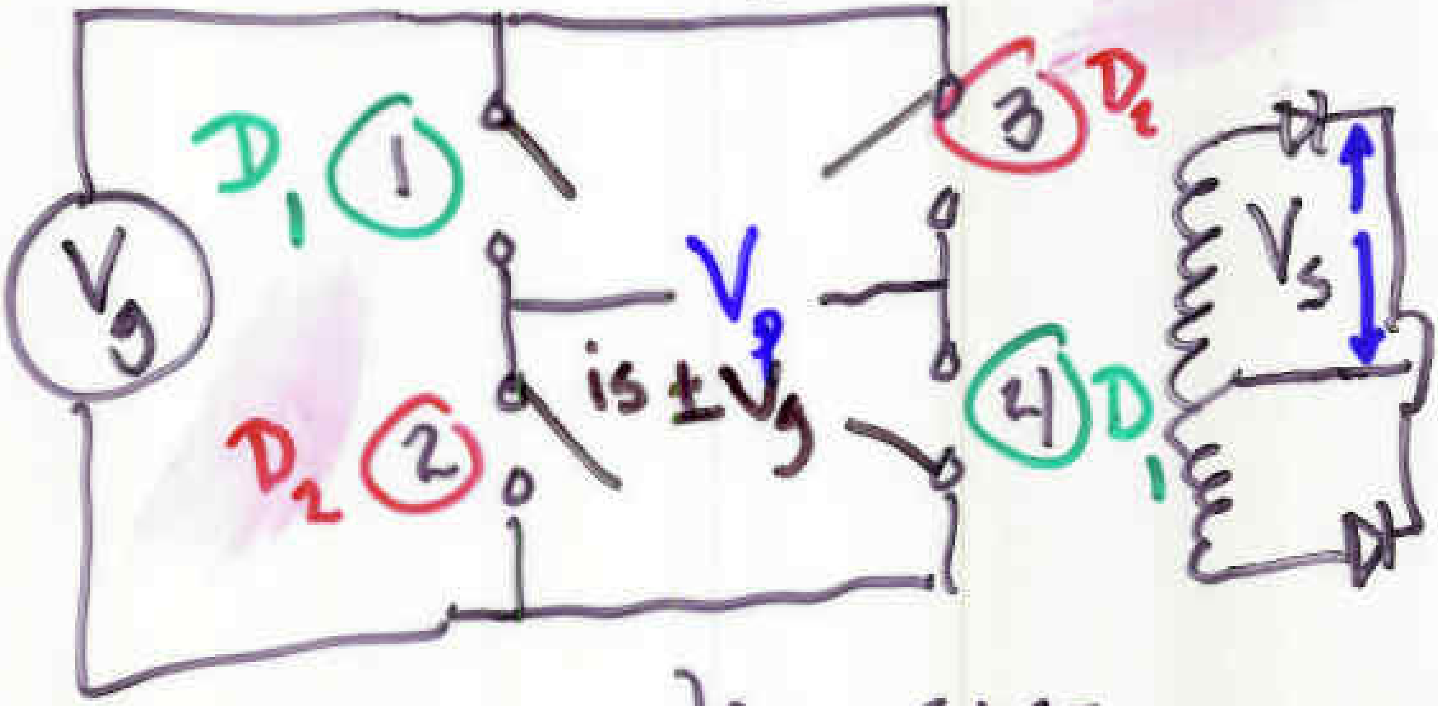


Fig. 3. *A transformer-based dc-ac power stage such as this H-bridge circuit offers galvanic isolation in exchange for added weight, size, cost and efficiency.*

Full Bridge Primary



Cross-connecting case

1,4 ON
2,3 off

$V_p = +V_g$ for DT_{sw}

Case $D = 1/2$

equal time

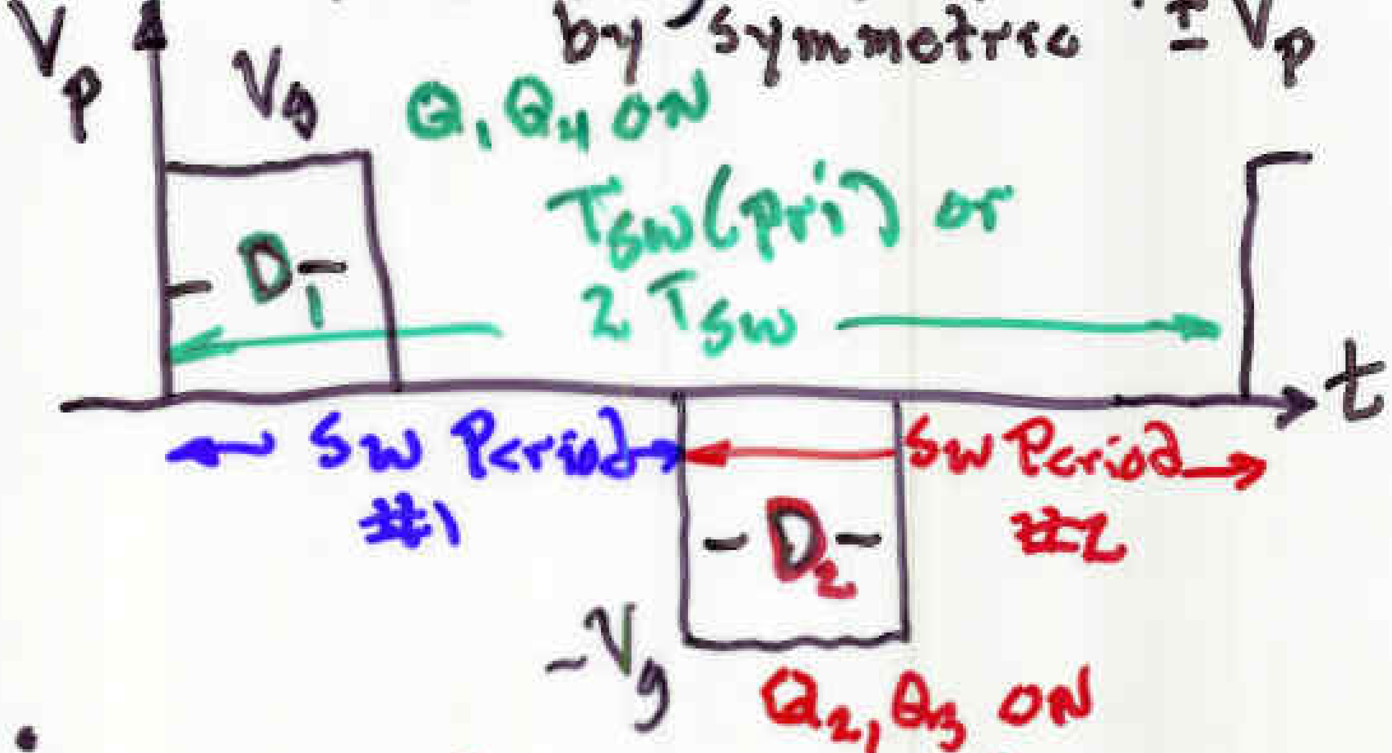
3,2 ON
1,4 off

$V_p = -V_g$ for DT_{sw}

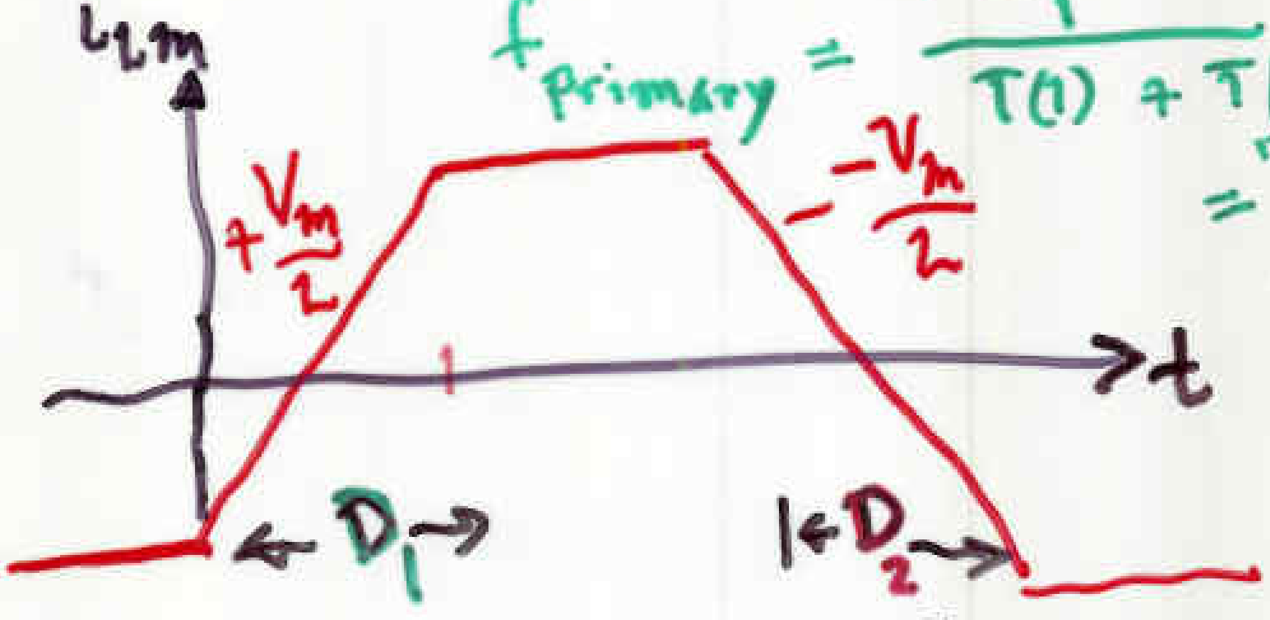
Allows for trf. reset!

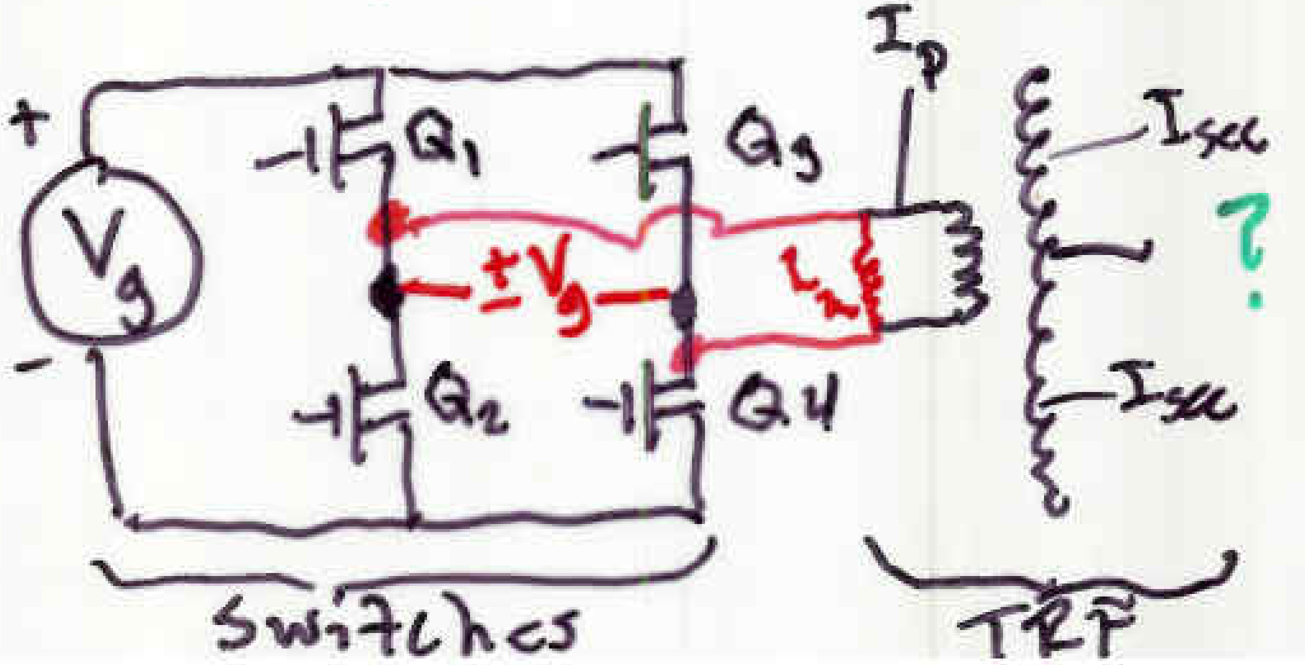
Key to success

Resetting Lm of Trf by symmetric ± Vp

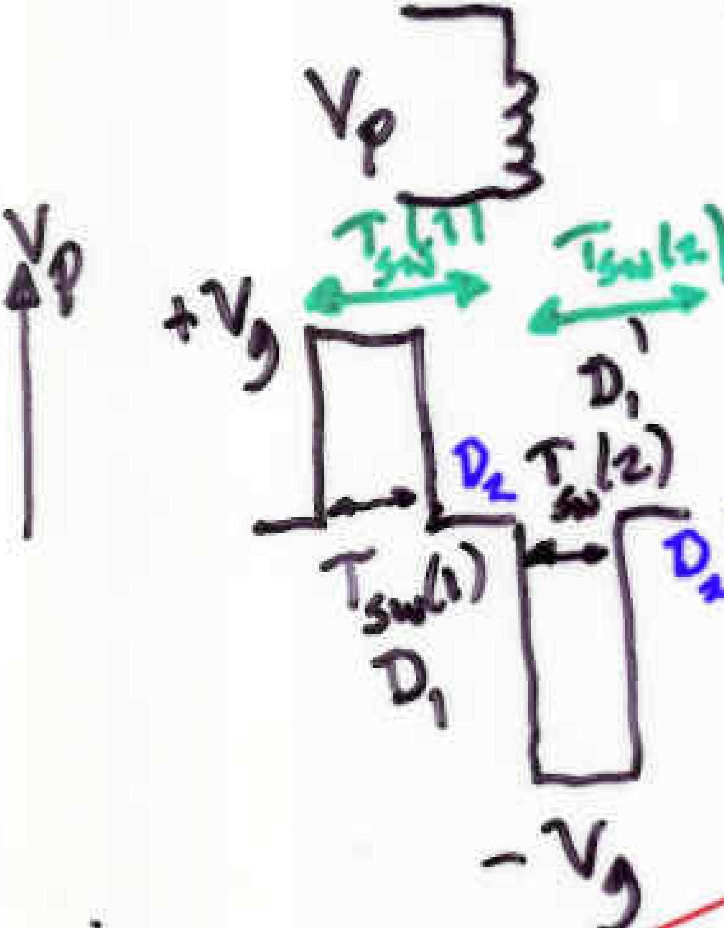


$$f_{primary} = \frac{1}{T(1) + T(2)} = \frac{"f_{sw}"}{2}$$





Reseting L_m of Trf via Bridge Drive



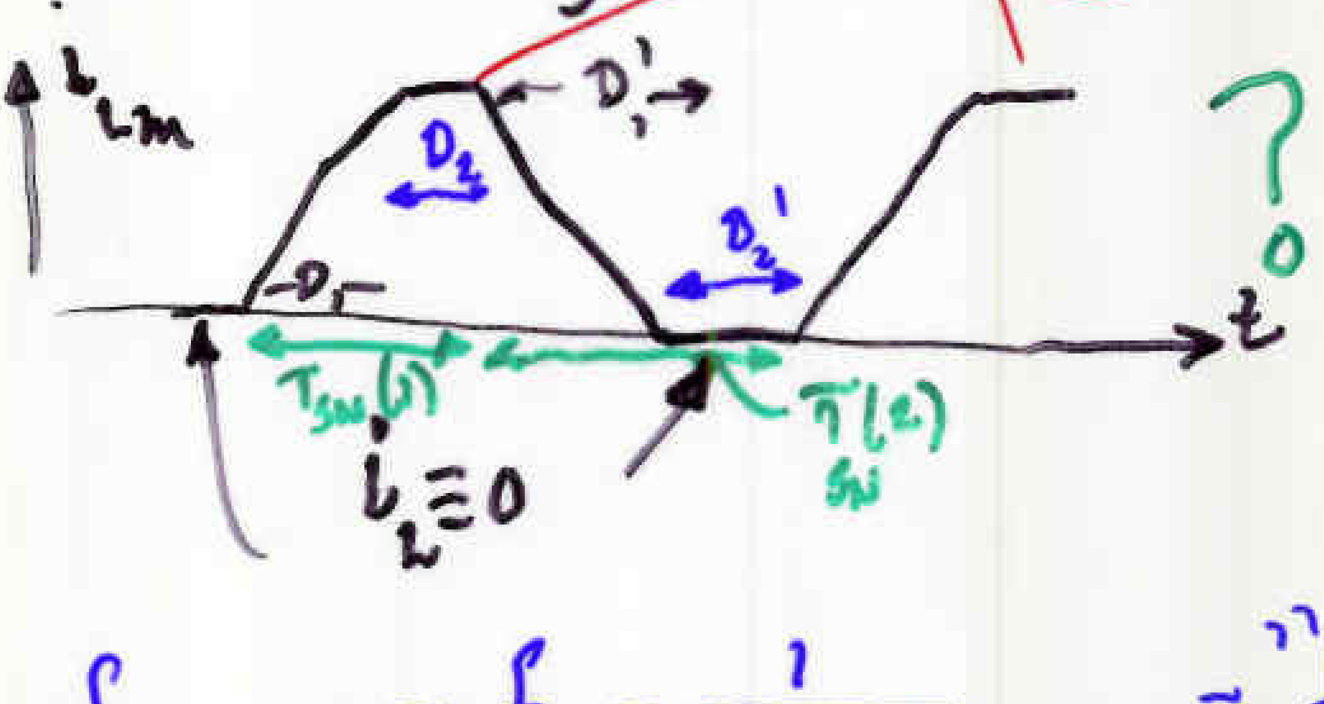
$T_{sw}(1)$: D_1, D_2

$T_{sw}(2)$: D_1', D_2'

$\pm V_g$

Zero intervals are key

$V_g = 0$
i_2 hangs!
☺



$$f_{primary} = f_p = \frac{1}{T_{sw}(1) + T_{sw}(2)} = ``f_{sw}"$$

Effect of nonidealities on transformer volt-second balance

Volt-seconds applied to primary winding during first switching period:

$$(V_g - (Q_1 \text{ and } Q_4 \text{ forward voltage drops}))(Q_1 \text{ and } Q_4 \text{ conduction time})$$

Volt-seconds applied to primary winding during next switching period:

$$-(V_g - (Q_2 \text{ and } Q_3 \text{ forward voltage drops}))(Q_2 \text{ and } Q_3 \text{ conduction time})$$

These volt-seconds never add to *exactly* zero.

Net volt-seconds are applied to primary winding

Magnetizing current slowly increases in magnitude

Saturation can be prevented by placing a capacitor in series with primary, or by use of current programmed mode (Chapter 12) } block DC

① No assurance: $V^{+} \neq V_{D}^{-}$ Insure core reset?

Effect of nonidealities on transformer volt-second balance

Volt-seconds applied to primary winding during first switching period:

$T_{sw}(1)$ $(V_g - (Q_1 \text{ and } Q_4 \text{ forward voltage drops}))(Q_1 \text{ and } Q_4 \text{ conduction time})$ = D

Volt-seconds applied to primary winding during next switching period:

$T_{sw}(2)$ $-(V_g - (Q_2 \text{ and } Q_3 \text{ forward voltage drops}))(Q_2 \text{ and } Q_3 \text{ conduction time})$ = D

②

③ These volt-seconds never add to *exactly* zero. ← Device variations in Q's

Net volt-seconds are applied to primary winding

Magnetizing current slowly increases in magnitude

Saturation can be prevented by placing a capacitor in series with primary, or by use of current programmed mode (chapter 11)

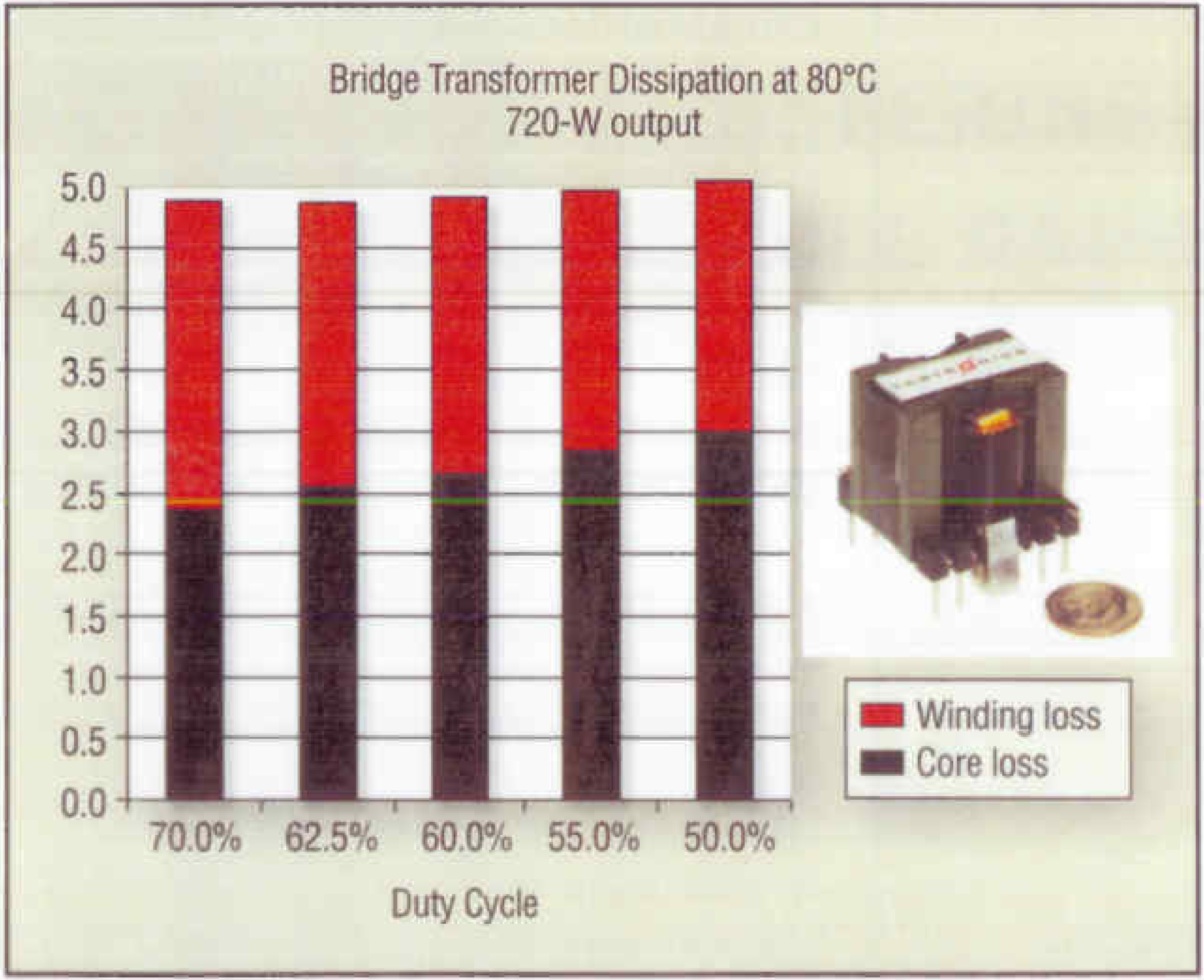
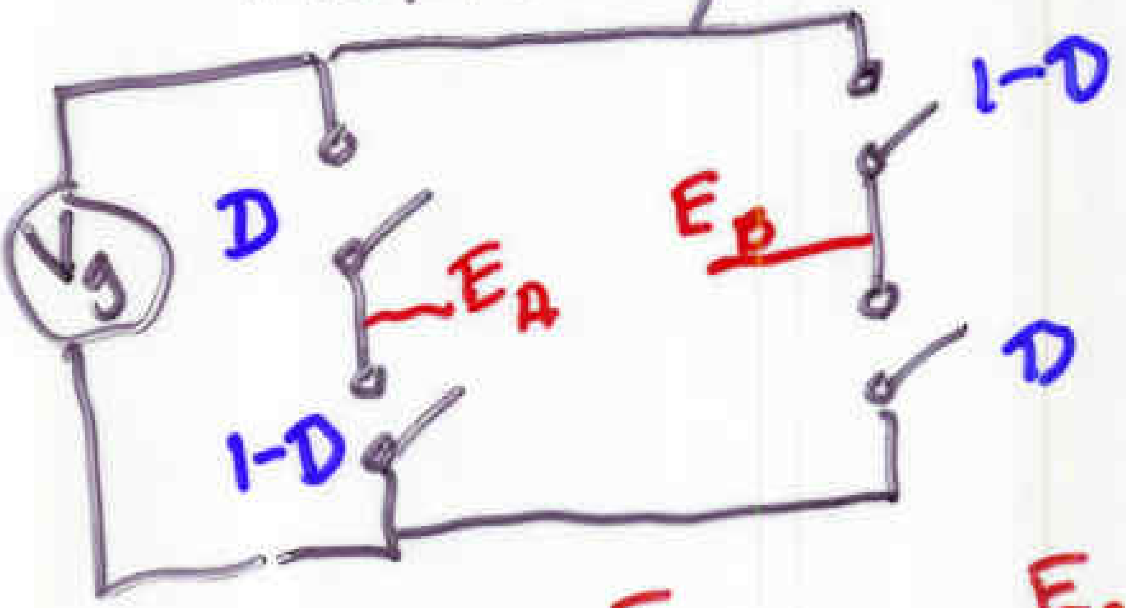


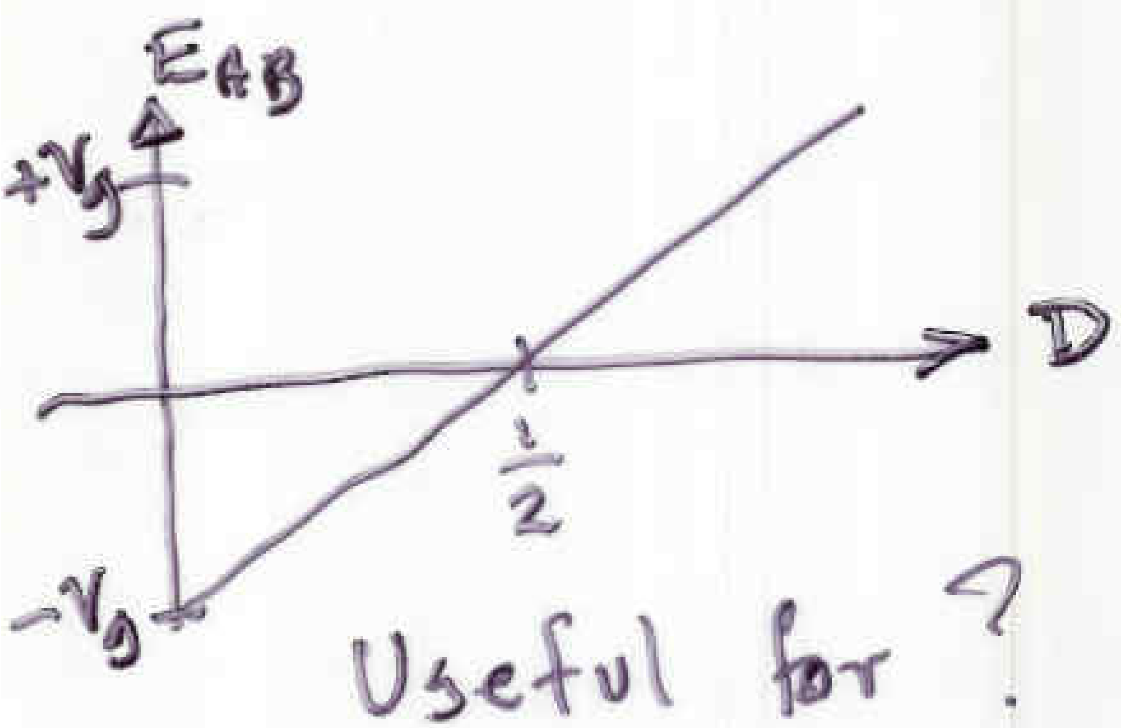
Fig. 10. *Measured total loss of 150-kHz bridge transformer providing 12 V at 60 A.*

Flexibility of Bridge

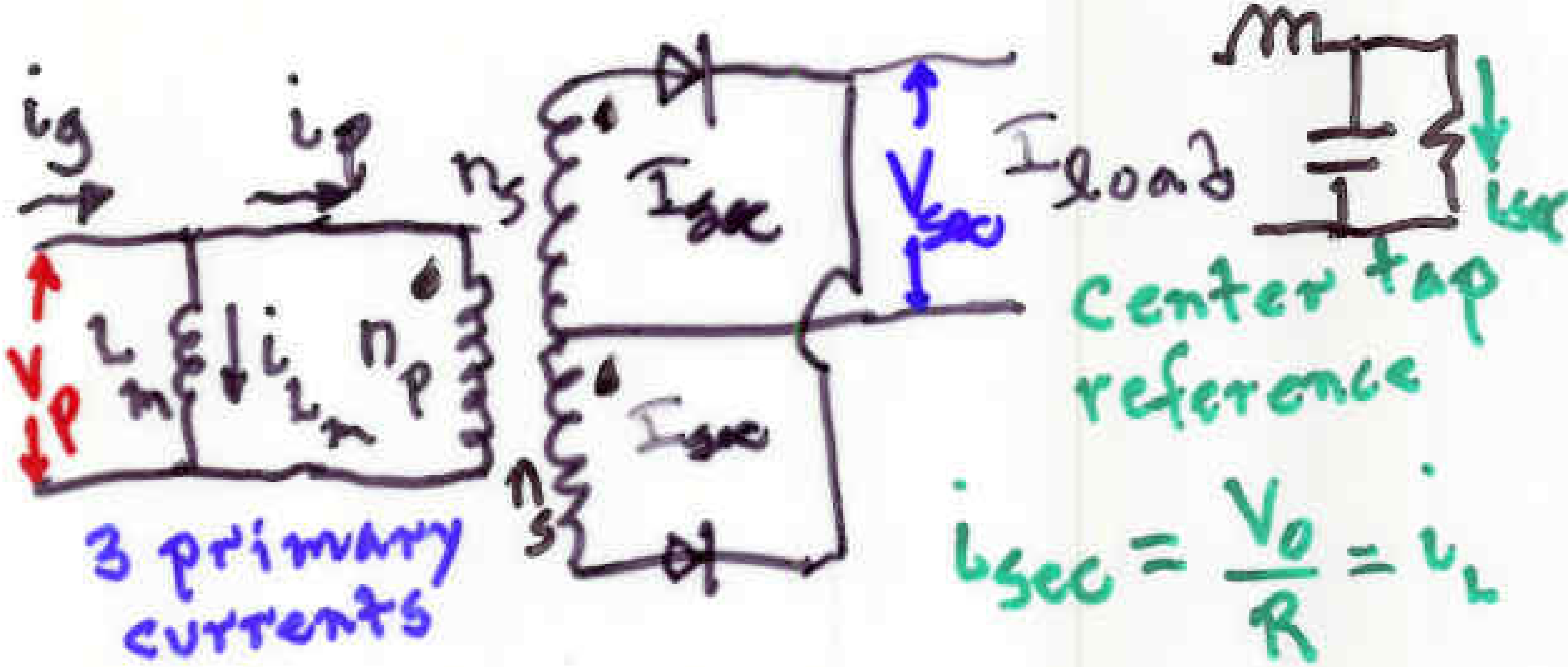


$$E_{AB} \equiv \overset{E_A}{D V_g} - \overset{E_B}{(1-D) V_g}$$

$$= (2D-1) V_g$$



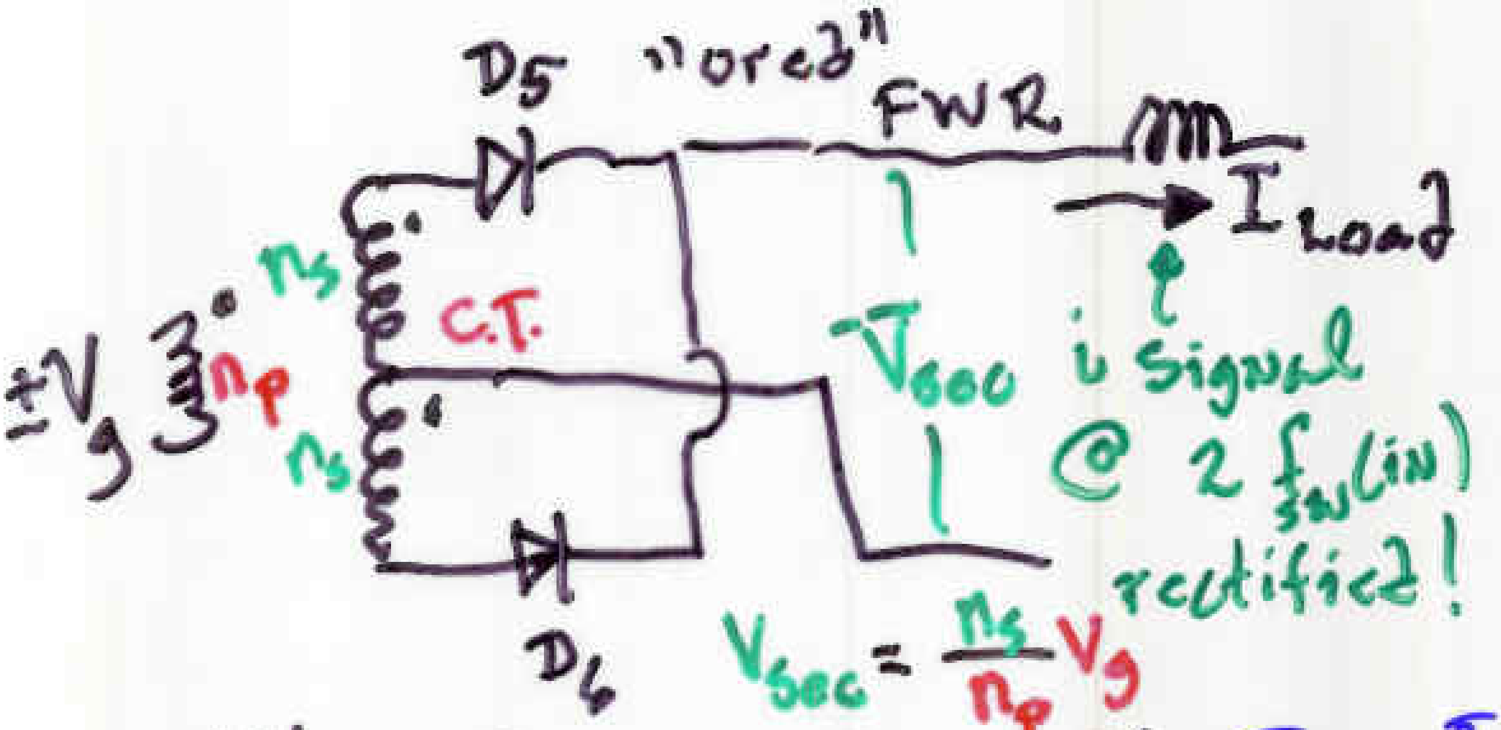
Useful for ?



$$i_{sec} = \frac{V_o}{R} = i_L$$

$$i_p = \underbrace{i_{sec}}_{\text{always sums to } I_L \text{ @ } 2 f_{sw}} \frac{n_p}{n_{sec}} \quad ?$$

$$i_g = \underbrace{i_{L_m}(@ f_{sw})}_{\substack{\text{Always} \\ \text{resets} \\ \text{Trf.} \\ \text{at } f_{sw} \\ \text{due to } v_p = \pm v_g}} + \underbrace{i_p(@ 2 f_{sw})}_{\substack{\text{dominates} \\ \text{@ heavy load}}}$$



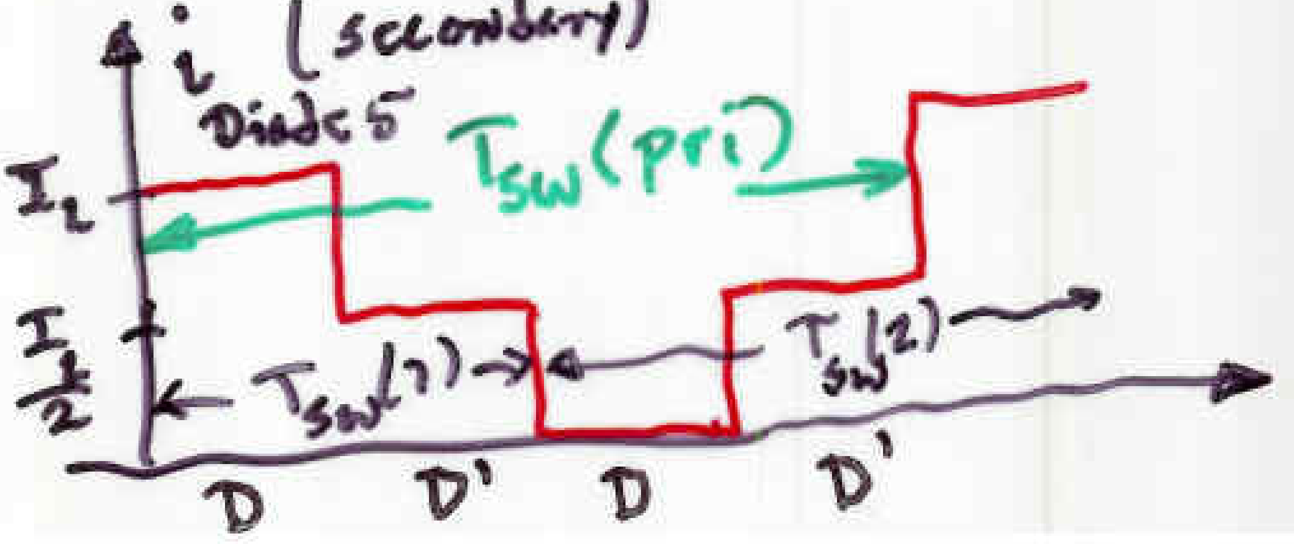
$V_{sec} = \frac{n_s}{n_p} V_g$

$+V_g$: D_5 ON, D_6 off $I_{D5} = I_{Loa}$
for DT_{sw}

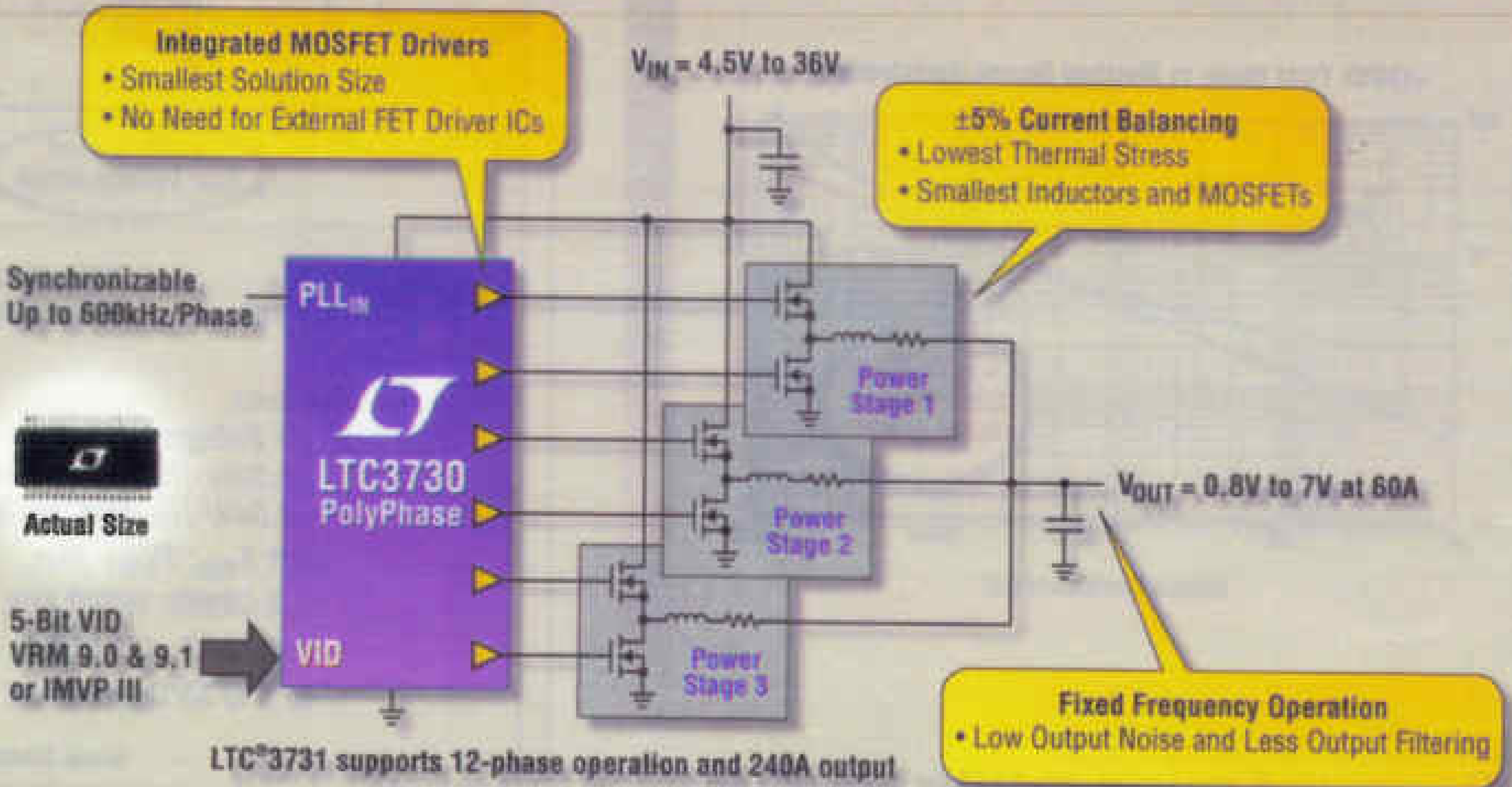
$-V_g$: D_5 off, D_6 ON $I_{D6} = I_{Load}$
for DT_{sw}

$V_g = 0$: I_L pulls both diodes
for $D'T_{sw}$ ON $I_{diode} = \frac{I_L}{2}$
twice

$I_{D5} = I_{D6} = \frac{I_{load}}{2}$



60A, No Heat Sinks



Integrated MOSFET Drivers
- Smallest Solution Size
- No Need for External FET Driver ICs

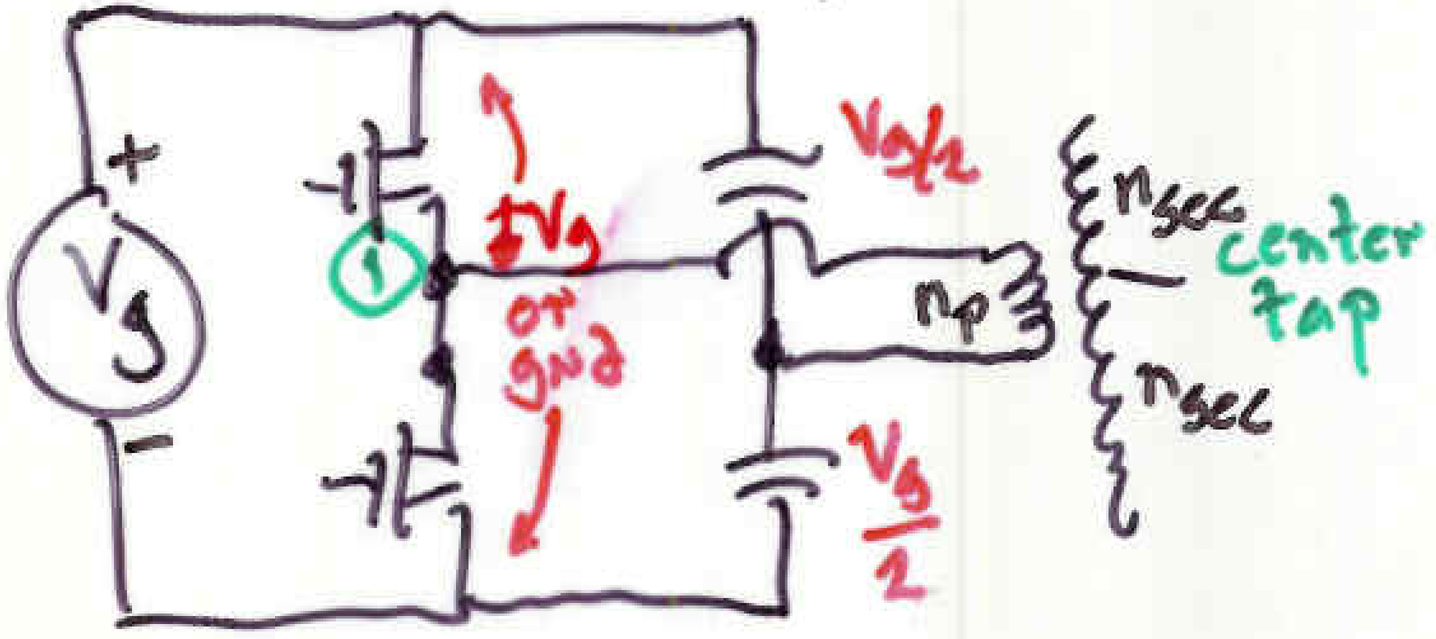
±5% Current Balancing
- Lowest Thermal Stress
- Smallest Inductors and MOSFETs

Fixed Frequency Operation
- Low Output Noise and Less Output Filtering

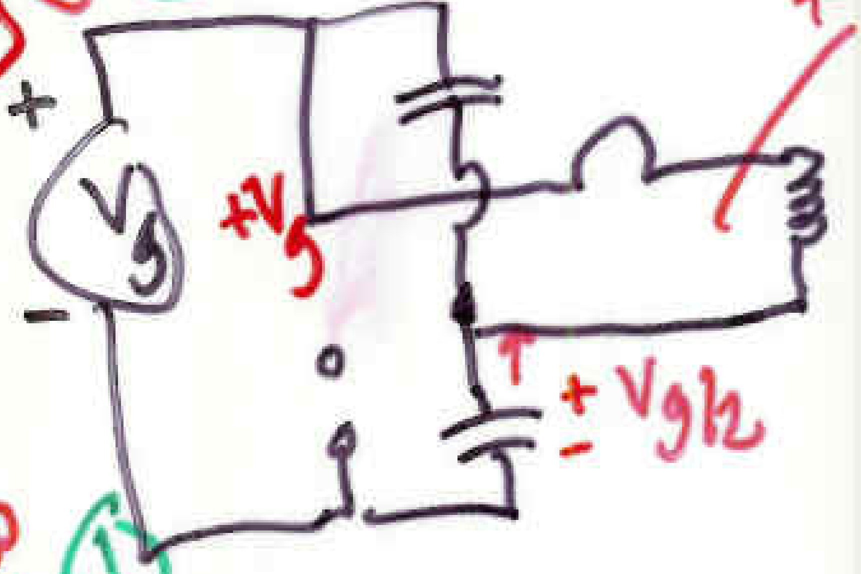
LTC®3731 supports 12-phase operation and 240A output

Broadest Family of PolyPhase® DC/DC Controllers

Replace two Q by two C!



$+V_g$ @ ①



$+V_g/2 = V_p$

You lose $\frac{1}{2} V_g$

Gnd @ ①

$-V_g/2 = V_p$

Again you lose $\frac{1}{2}$ of drive

Embedded telecom brick solutions

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Multi-output converter	LM5030, LM5642	Optional	High efficiency/multi-output power

Pbm 6.10

- Single resistor oscillator setting
- Synchronizable to external clock
- 1 A sink/source drivers
- Thermal shutdown

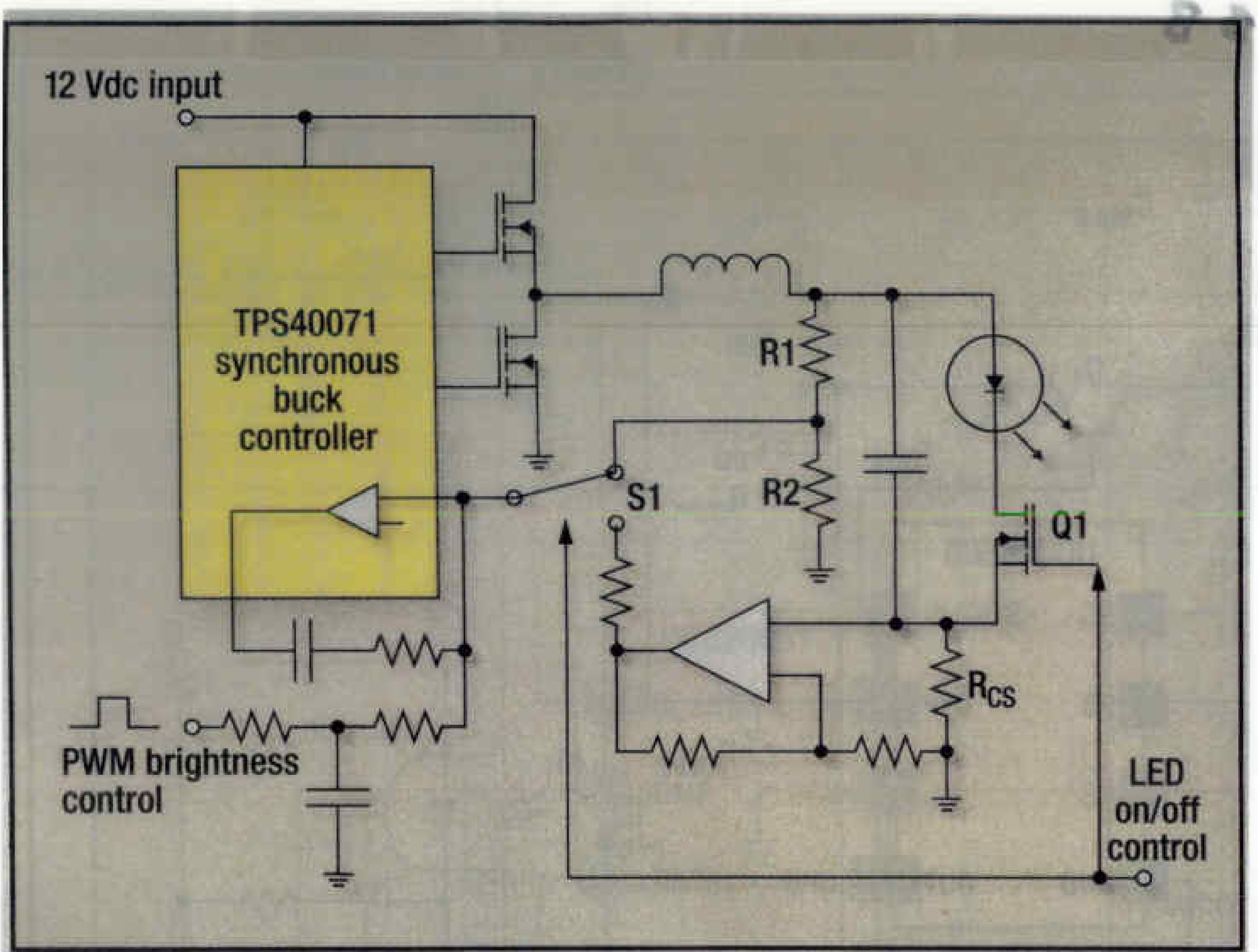
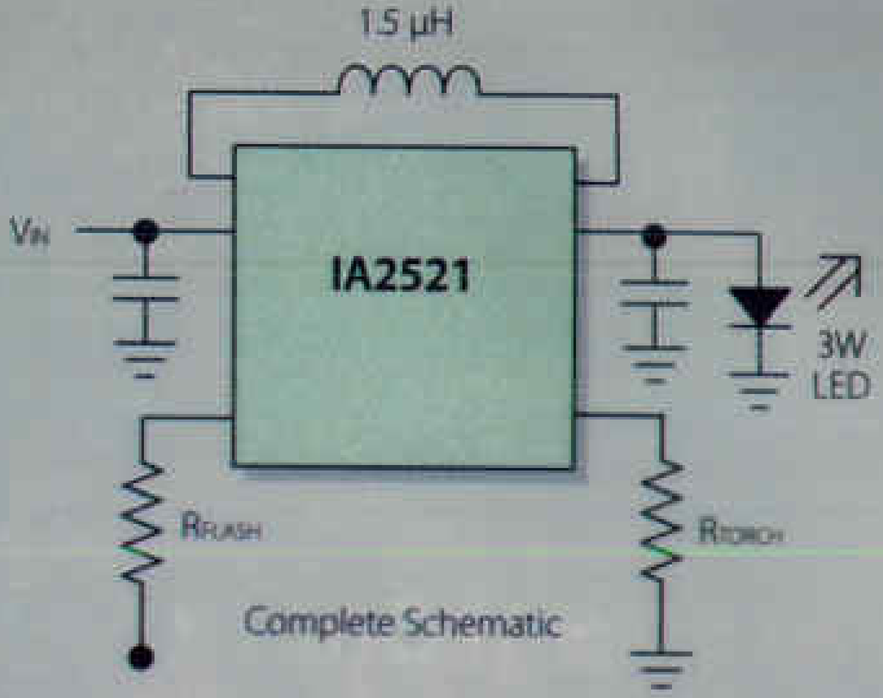


Fig. 7. *Driving LEDs require precise timing, duty factor and amplitude*

Integration IA2521 LED Flash Driver



Complete Schematic

FEATURES:

- Buck-boost, 2.7 – 4.5V input
- 95% efficiency with tiny inducto
- Separately controllable torch and flash brightness
- Flash rise time same as for Xenon tube
- Very low cost!

For more information visit
www.integration.com

Or call Integration at
(650) 969 4100

INTEGRATION

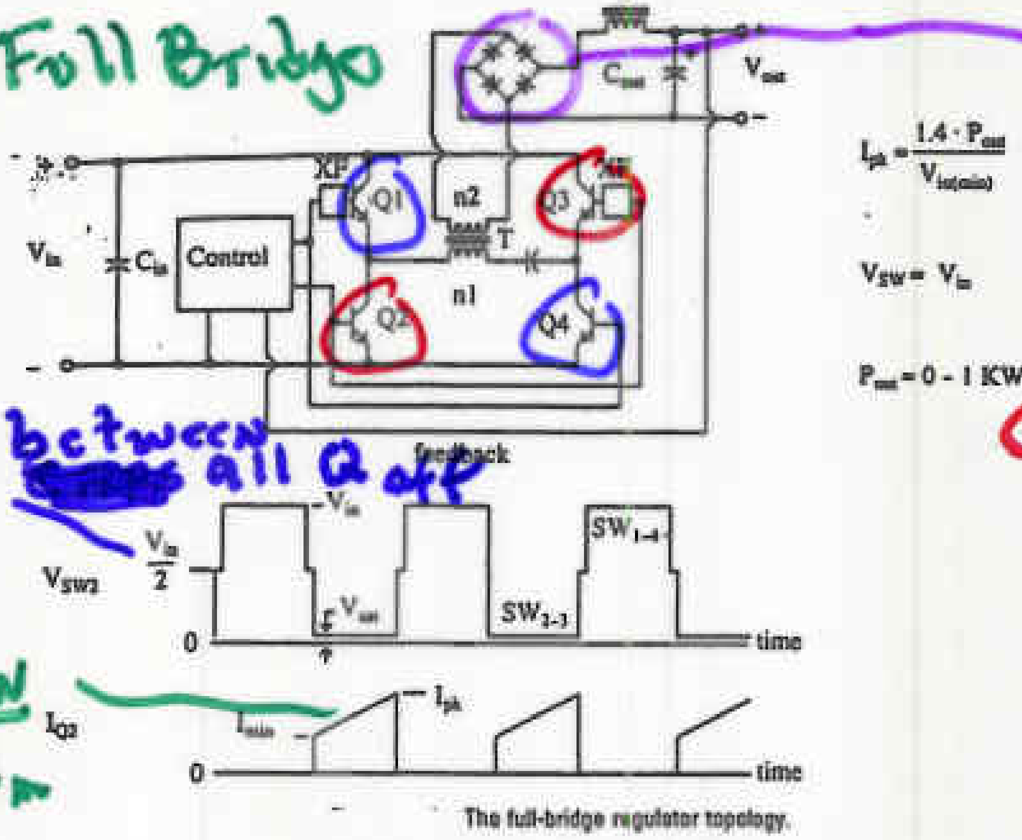
One of the fastest-growing fabless semiconductor companies in Silicon Valley, Integration designs and delivers tested wafers and packaged ICs for Power Management, RF, and Modem/Wireline applications.

All Q off condition for "deadtime"

Given by the full input voltage. A similar situation occurs for the full bridge shown below which also alternatively places V_{in} across the primary winding, but this time using four switches.

rectifier V_{stress} is $2 V_{out}$?

Full Bridge



V between ~~series~~ all Q off

$\frac{V_{IN}}{L_m}$

The full-bridge regulator topology.

Q V_{stress} $\simeq V_{IN}$ | @ One Q on one Q off

All Q off V_{stress} $\frac{V_{IN}}{2}$

We synchronize switches 1 and 4 together in time and then switches 2 and 3. Note that we place the full V_{in} across two switches in series when the timing puts Sw_{2-3} in the same sequence and SW_{1-4} in the alternative sequence. Hence, we reduce switch voltage stress when we employ the required high input voltage to reach high power levels. Again we have a trade-off as we employ more switches but their individual cost may well be much lower-hopefully a factor of ten.

On the next page we will summarize the switch sequence as well as the voltage ramp on the duty cycle circuit for the full bridge converter topology.

above w/o Secondary C.T

Next secondary with C.T. ?

What does centertap bring to the party?

① Two seperate Tsw/intervals

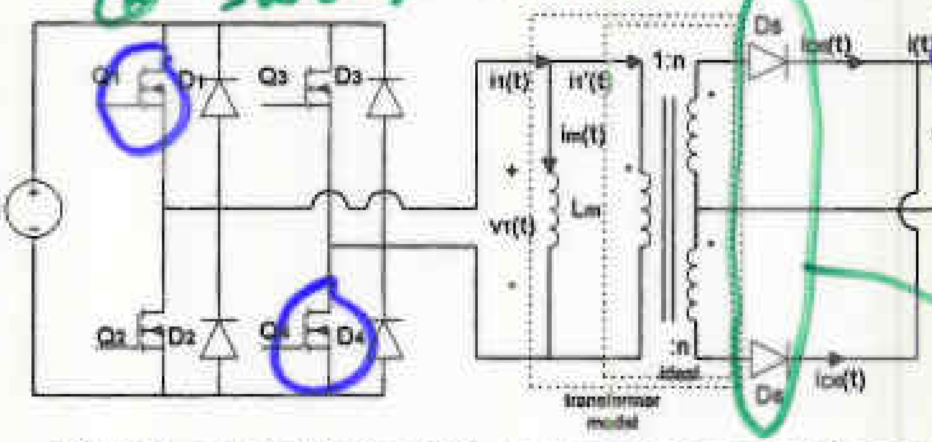
① $T_{sw(1)}$ D_1 D_2 int

② $T_{sw(2)}$ D_1 D_2 int

② opposite dots on diodes ⇒ ?

D: one on one off

$+V,0\ -V,0$



③ i_L will act as flywheel cause?

a. First T_s switch interval: $+V_g$ and zero applied sequentially

There are therefore two T_{sw} intervals one with $+V_g$ and one with $-V_g$ across the primary. Below is that during the first T_s in the primary with $+V_g$. V_T switches between 0 and V_g like non-isolated buck as follows during T_{sw}. During D V_g is applied and during D' zero is applied.

Insures core reset?

Primary (during first T_s)

During D	During D'
Q_1&Q_4 on	To achieve
$V_T = V_g$	$V_T = 0$
	either of two ways:
	1. All Q_1-Q_4 off, $V_T = 0$
	2. Q_1, Q_3 on, $V_T = 0$
	V_T=0 via equal V both sides

Core Goal

OK?

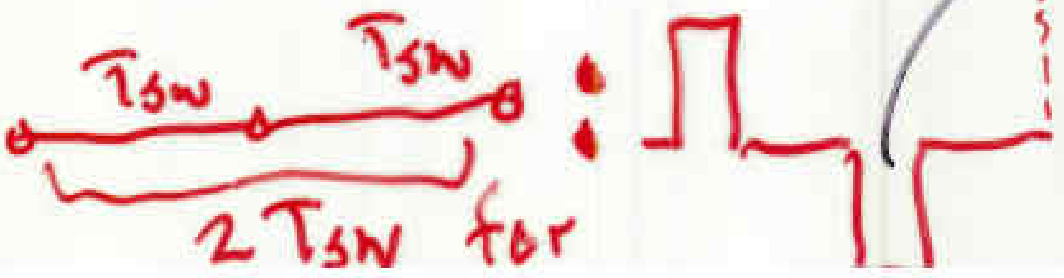
This means i_{Lm} is flat during D'

④ i_L hangtime ⇒ $i(L_m)$ = constant if $R_{L_m}=0$

b) Second T_{sw} interval: $-V_g$ and zero applied

The primary circuit looked at during the second T_s timing interval is different $T_{sw} \rightarrow 2T_{sw}$ because $-V_g$ is applied during D and zero during D'.

Bring i_L to zero



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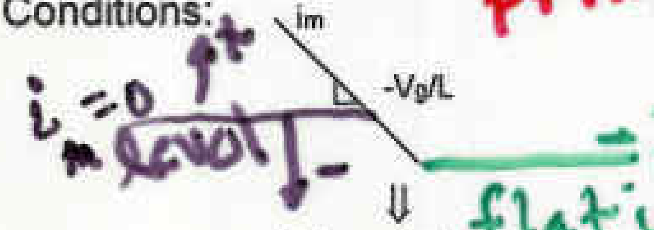
2nd switch period:

Primary(During $T_s \to 2T_s$)

	During D ①	During D'
Second Period Conditions:	Q_1&Q_3 on $V_T = -V_g$ ← reset primary	Achieve $V_T = 0$ by either of two ways: 1. All Q_1-Q_4 off 2. Q_2, Q_4 on — ok? So $V_T = 0$ Equal V on both sides.



⇓ ⇓ — @ $i_2 = 0$ goal

V_T switches between $-V_g$ and 0 in primary.

By symmetry we reset the core of the transformer L_m over $2T_s$. Up during D of the first T_s and down during D of second T_s.

$$\langle v_{Lm} \rangle_{2Ts} = 0$$

② Because of the switching configuration the transformer waveforms are at a frequency $f_s/2$, not at f_{sw}.

2. Secondary Voltage V_s Timing: SECONDARY of TRF

③ a) During first T_s interval

one diode full tilt I_{sec}

④ $\frac{I_{sec}}{2}$ per diode due to i_L flywheel

During D	During D'
V on secondaries is $nV_g = V_s$ * on coils tell diode D_5 on and diode D_6 off	V on secondaries is zero as $V_T = 0$ * on coils tell both D_5 and D_6 will be on D_5 stays on due to i_L D_6 goes on due to secondary polarity and the dot convention

Only D_5 ON carrying full i

} D_5 ON D_6 each I/2

b) During Second T_s interval

Find on your own for D Q_2, Q_3 and D_6 are on while for D' diodes D_5

⑤ each diode

} Diode staircase i

Web 576 L 16

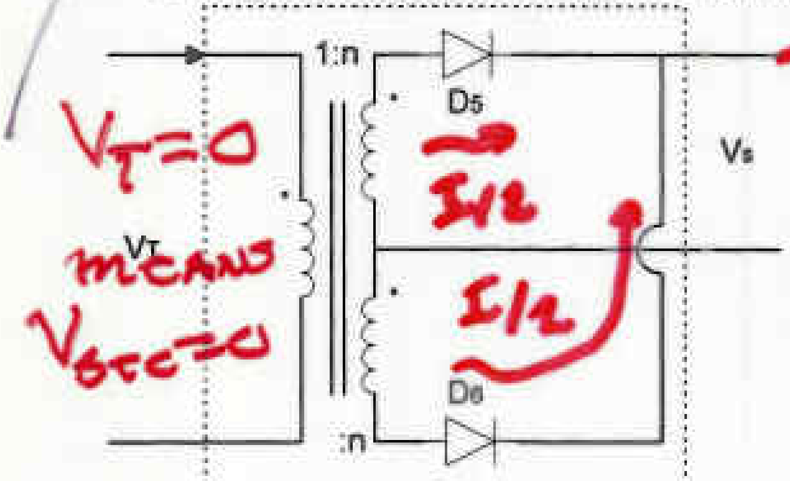
For D' interval
$V_p = 0 \Rightarrow V_{sec} = 0$

and D_6 are on.

2. Input and output currents

$i(out) = i_{D5} + i_{D6}$. How it splits is uncertain, but if at anytime it splits equally then: $i_{D5} = i_{D6} = \frac{i(out)}{2}$

During first T_s interval i_{in}(transformer) = ? When $i_{D5} = i_{D6}$

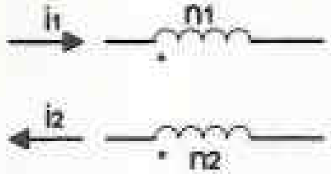


At the output
$i_{D5} + i_{D6}$
while in the primary
i_{D5} causes ni_{D5}
i_{D6} causes ni_{D6}

Ideal Trf

With all Q off $i_{prim} = 0$

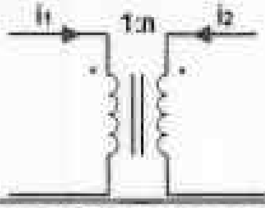
Review the dot convention on a two turn transformer that says:



if $n_1 i_1$ is positive ⇒ $+n_1$ then

is negative ⇒ $-n_2 i_2$

watch dots i_1
$n_1 i_1 + n_2 i_2 = 0$



coming into the dot
in secondary and
into dot of primary

At the primary on top of the page we have three currents.
i_{D5} and i_{D6} flow in opposite directions with respect to the coil dots:
i_{in} and i_{D6} are assumed flowing into the dot

$$i_{in} - ni_{D5} + ni_{D6} = 0 \Rightarrow i_{in} = 0$$

↓ ↓ ↓

first T_{sw} ① D intervals only

2nd T_{sw} "D"

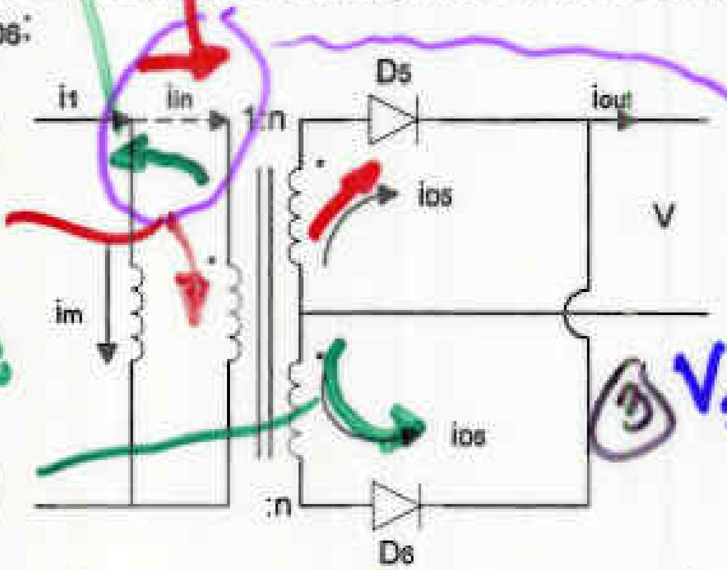
first "D"

± flow direction

$V_o - nV_g = 2 V_{out} = 2n V_g$

flows out of dot	cancel if equal	assuming $i_{D5} = i_{D6}$

For I_{in} alternating then in general i_{D5} and i_{D6} alternate the flows as shown below but always the load receives current either for i_{D5} or i_{D6}:



1st D

2nd D

② I_{stress} primary

$I_{prim}(in) = n \sum I_{sec}$

③ V_{stress} rectifier diodes $\approx 2 V_{out}$?

↓

$i_1 = i_{in} + i_M$. ← i_1 has two components

During the first T_s we find during interval D the two equations below

$$i_m = i_1 - n i_{D5} + \underbrace{n i_{D6}}_{0} \quad \text{Transformer input}$$
$$i(out) = i_{D5} + i_{D6} \quad \text{Transformer output}$$

During the second T_s period $T_s \rightarrow 2T_s$ during the same interval D we get the same result for i_m and i_{out}. Note in the first T_s with $+V_g$ applied $i_{D5} \neq 0$ but $i_{D6} = 0$. Where as in the second T_s with $-V_g$ applied $i_{D5} = 0$ but $i_{D6} \neq 0$.

} only one diode ON during "D"

⇒ Switching ripple at f_s

⇒ Transformer ripple occurs at $f_s/2$!

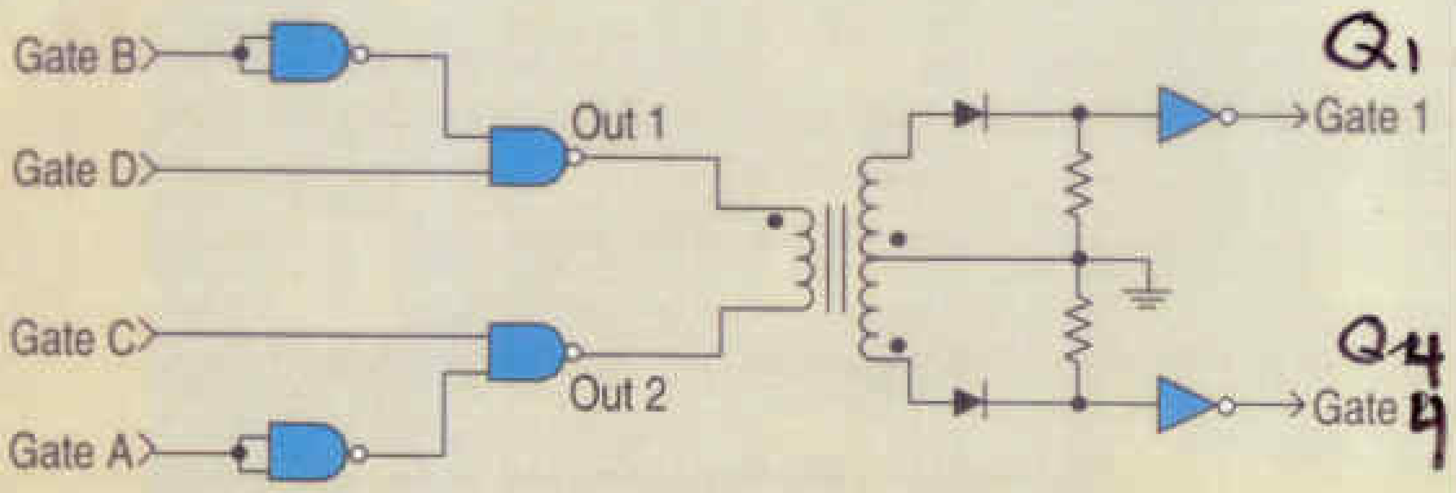
D intervals one secondary diode conducts

D' intervals ?

Control drives recquired for freewheeling $V_p=0$

SYNCHRONOUS RECTIFIER

	Primary PWM Inputs				Trans Inputs		SR Inputs	
State	Gate A	Gate B	Gate C	Gate D	Out 1	Out 2	Gate 1	Gate 2
t0 → t1	1	0	0	1	0	1	0	1
t1 → t2	1	0	1	0	1	1	1	1
t2 → t3	0	1	1	0	1	0	1	0
t3 → t4	0	1	0	1	1	1	1	1



ON
off
same
time

Fig. 2. *Synchronous rectifier truth table and drive logic.*

to one another) turn on during each phase of a clock cycle. For simplicity, the circuit of **Fig. 1** has a common 5-V

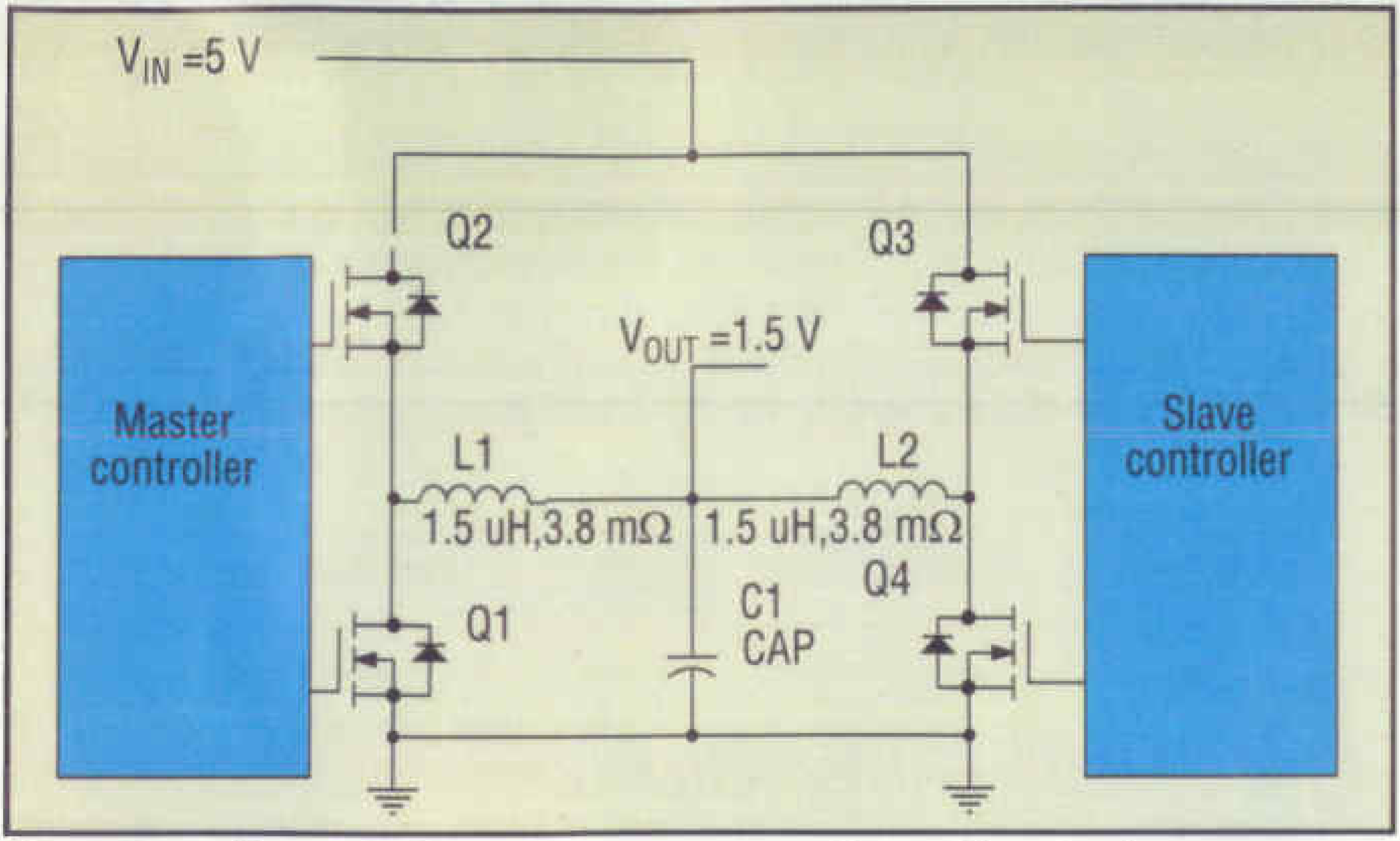


Fig. 1. *Two-phase dual-synchronous controller with a single output. Redrawing the single-chip controller as two separate controllers simplifies the analysis of controller operation.*

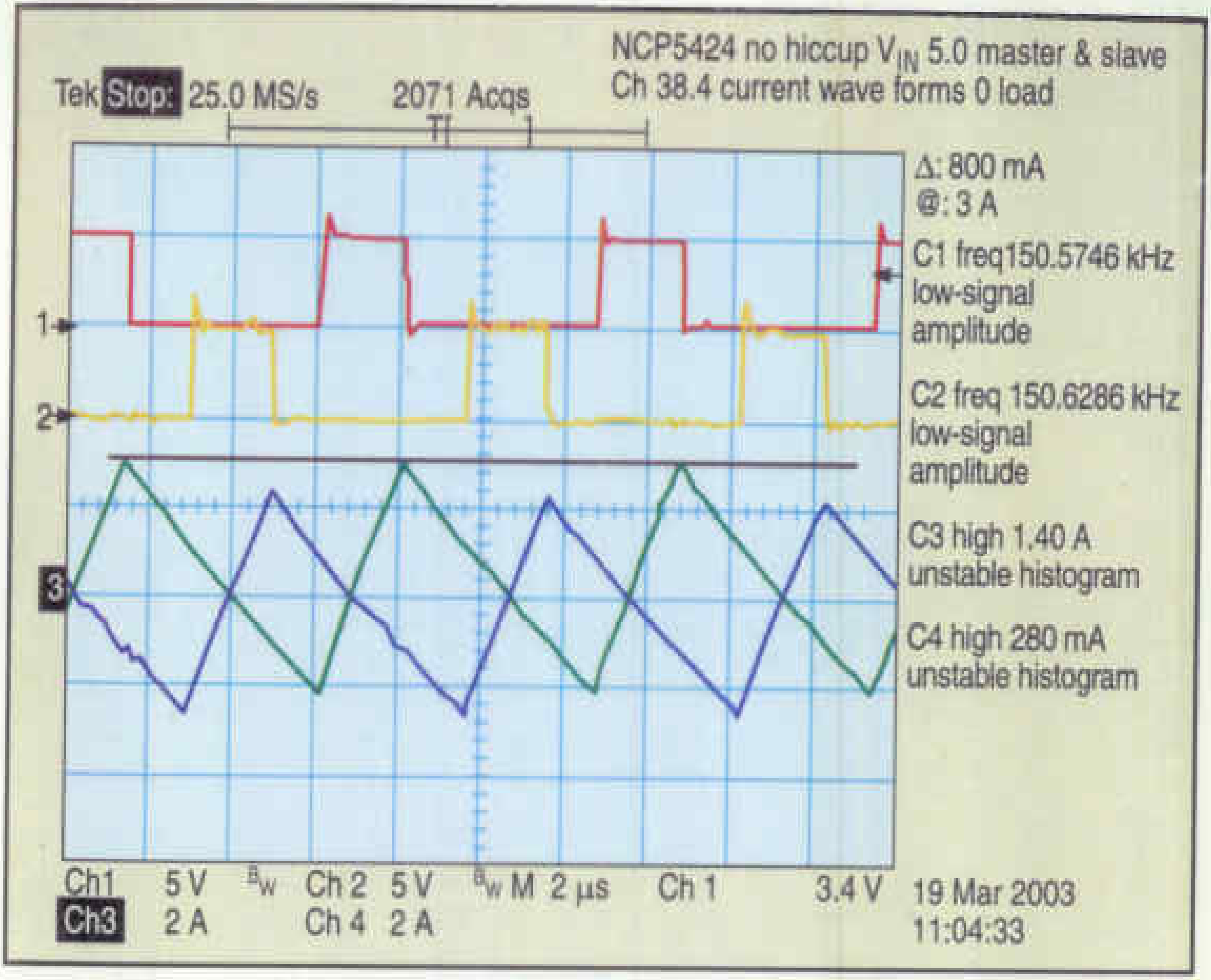


Fig. 2. *Shown here are the waveforms for the Fig. 1 circuit operating under no-load conditions with a common input voltage of 5 V to both controller channels. These waveforms include the switching nodes of the master con-troller (switching waveform shown on Channel 1) and the slave controller (switching waveform shown on Channel 2), as well as the inductor currents for L1 (Channel 3) and L2 (Channel 4).*

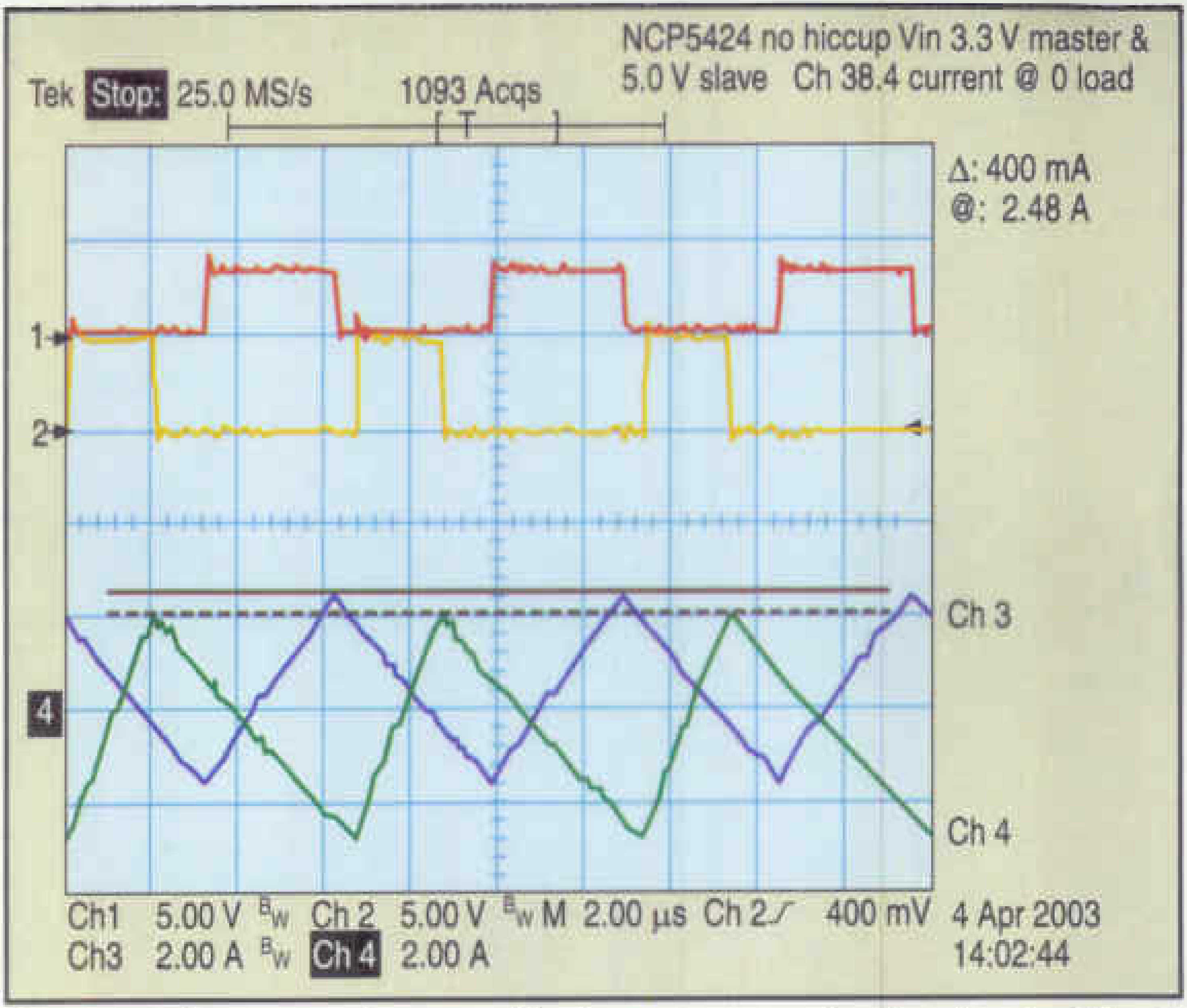


Fig. 3. *Switching waveforms and inductor currents for the circuit of Fig. 1 are shown here as in Fig. 2 with the circuit operating no-load. However, the input voltage on the master controller (switching waveform shown on Channel 1) has been reduced to 3.3 V, while the input voltage on the slave controller (switching waveform shown on Channel 2) remains at 5 V.*

reduced to 3.3 V, the Channel 1 pulse width at zero load increases to about 3.25 µs. This change reflects