Forward Converter

n : 1
Step down

$n\uparrow$ $I_p\downarrow$ $V_{sec}\downarrow$

$n\uparrow$ Also allows

$D = \frac{1}{2}$ max $\Longrightarrow D_{op} = .4$ max

Allows D to change up to 0.5 for rapid changes V_{out}

But $I^2_{rms} R_{on}$ (FET) also changes

Table I - Effect of Changing Specifications on Transformer Turns Ratio Selection

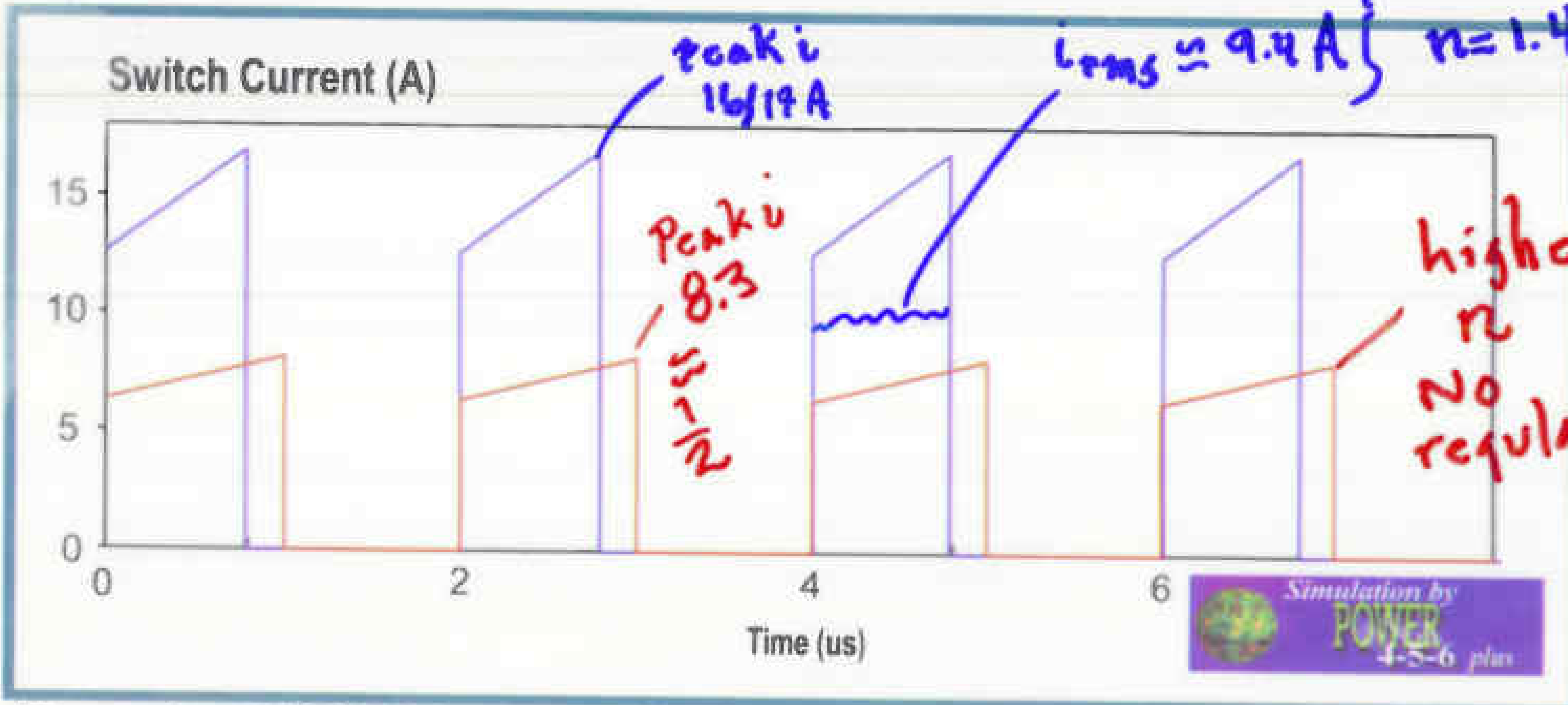
Key	Turns Ratio	Peak Switch Current	RMS Switch Current	Conduction Loss (50 mOhm)	Diode Voltage Stress	Inductor (4A Ripple)
Regulated Forward 40-60 V	1.43:1	16.9 A	9.4 A	4.4 W	42 V	8 uH
Regulated Forward 60 V only	2.14:1	11.3 A	6.3 A	1.9 W	28 V	8 uH
Non-regulated Forward 60 V only	2.7:1	8.9 A	5.5 A	1.5 W	22 V	7 uH
Non-regulated forward 60 V only synchronous rectifier	2.9:1	8.3 A	5.2 A	1.3 W	20.8 V	6.8 uH

trend

Today $\frac{1KW}{in^3}$

"48 volt in" / $\frac{12}{5}$ out

95% efficient



Peak i 16/17 A

$i_{rms} \simeq 9.4A$ } Baseline $\eta = 1.4$

Peak i 8.3 $\simeq \frac{1}{2}$

higher η

No regulation

Figure 2a: MOSFET currents for forward converter with and without regulation

V_{in}: 40-60

V_{out}: 10V @ 20 A

$D_{max} = \frac{1}{2}$ for reset

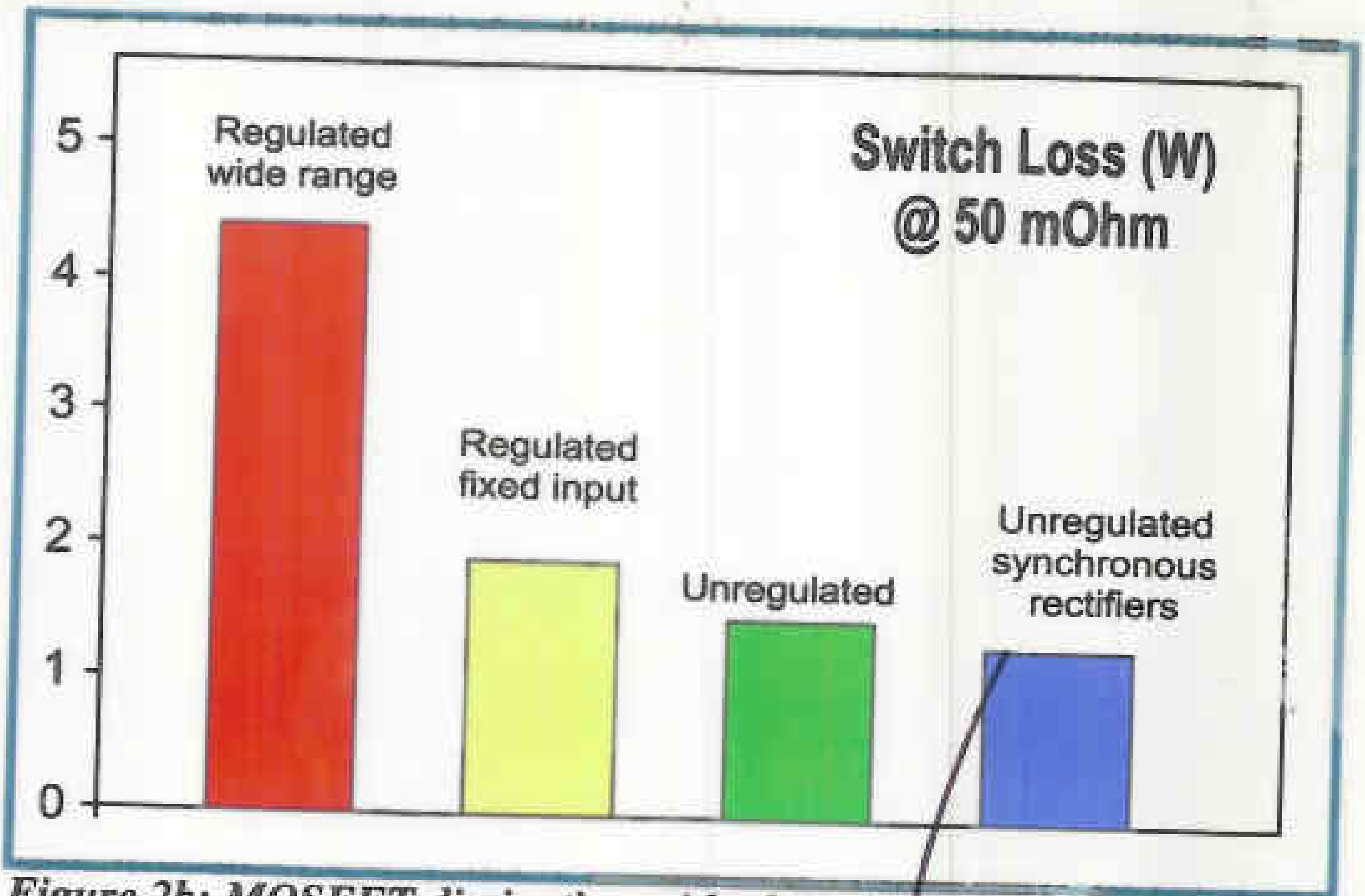


Figure 2b: MOSFET dissipation with changing specifications and fixed on-resistance

x3 lower

43V
Stress

21V
Stress

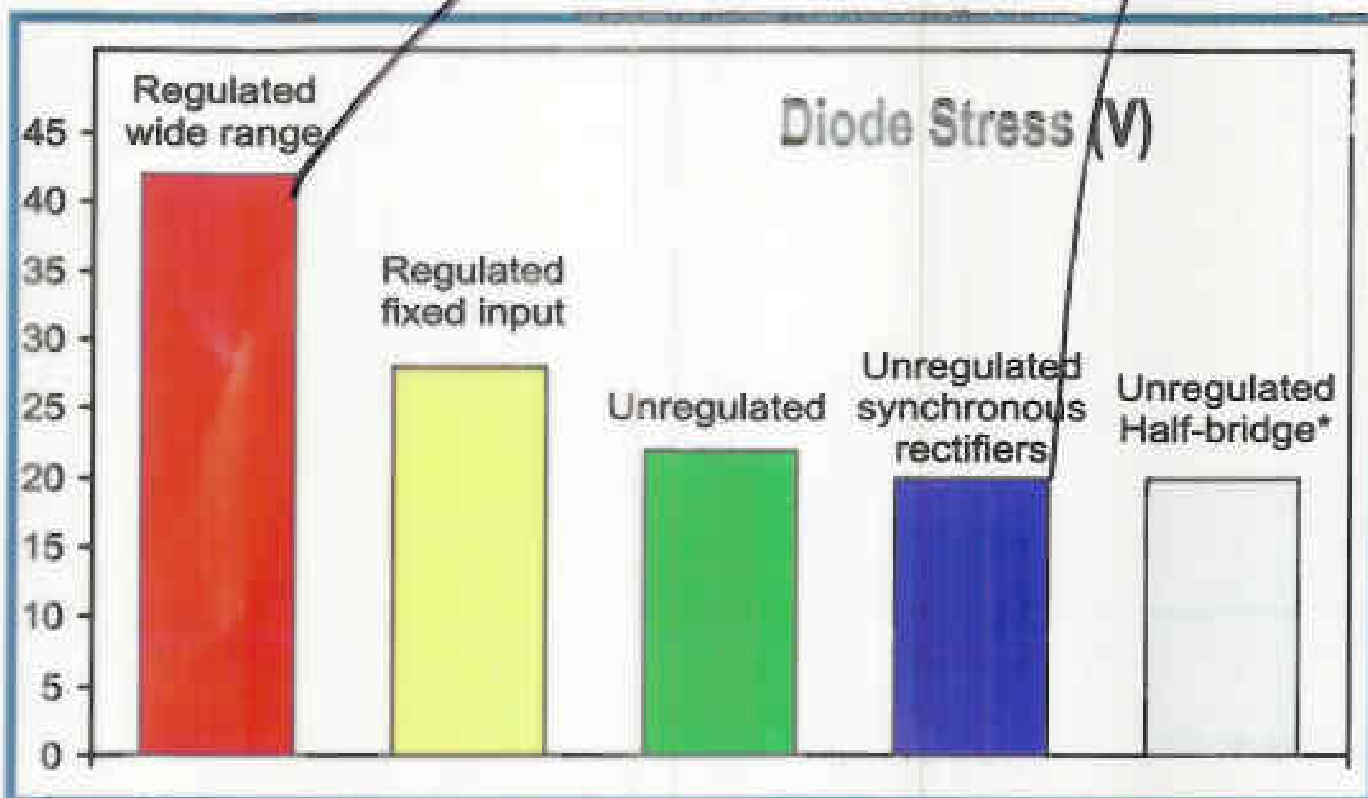


Figure 2c: Secondary rectifier voltage stress with changing specifications

Table II - Effect of Changing Specifications on Transformer Design

	Frequency	Core Area	Transformer Turns	Core Loss
Non-regulated Forward 60 V only Synchronous Rectifier	8:3 turns 200 kHz	0.54 cm^2	8:3	0.65 W
Non-regulated Forward 60 V only Synchronous Rectifier	3:1 turns 500 kHz	0.54 cm^2	3:1*	4.5 W
Half Bridge	3:1 turns 500 kHz	0.54 cm^2	3:1	core at fsw/2 1.25 W Bidirectional B

* *Closest available turns ratio - Bmax is very high with no design margin*

$B_{max} \sim \frac{1}{2}$

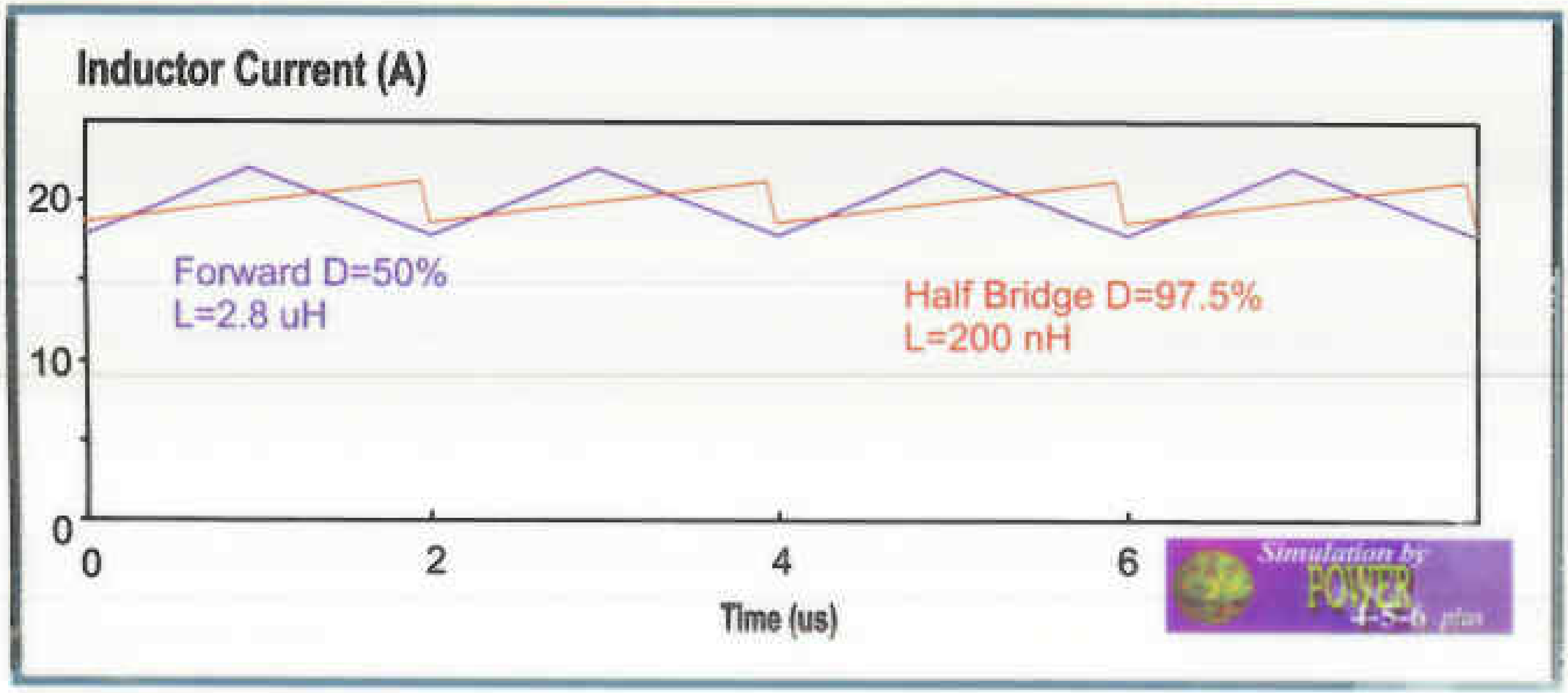


Figure 3a: Inductor currents for unregulated forward and half-bridge

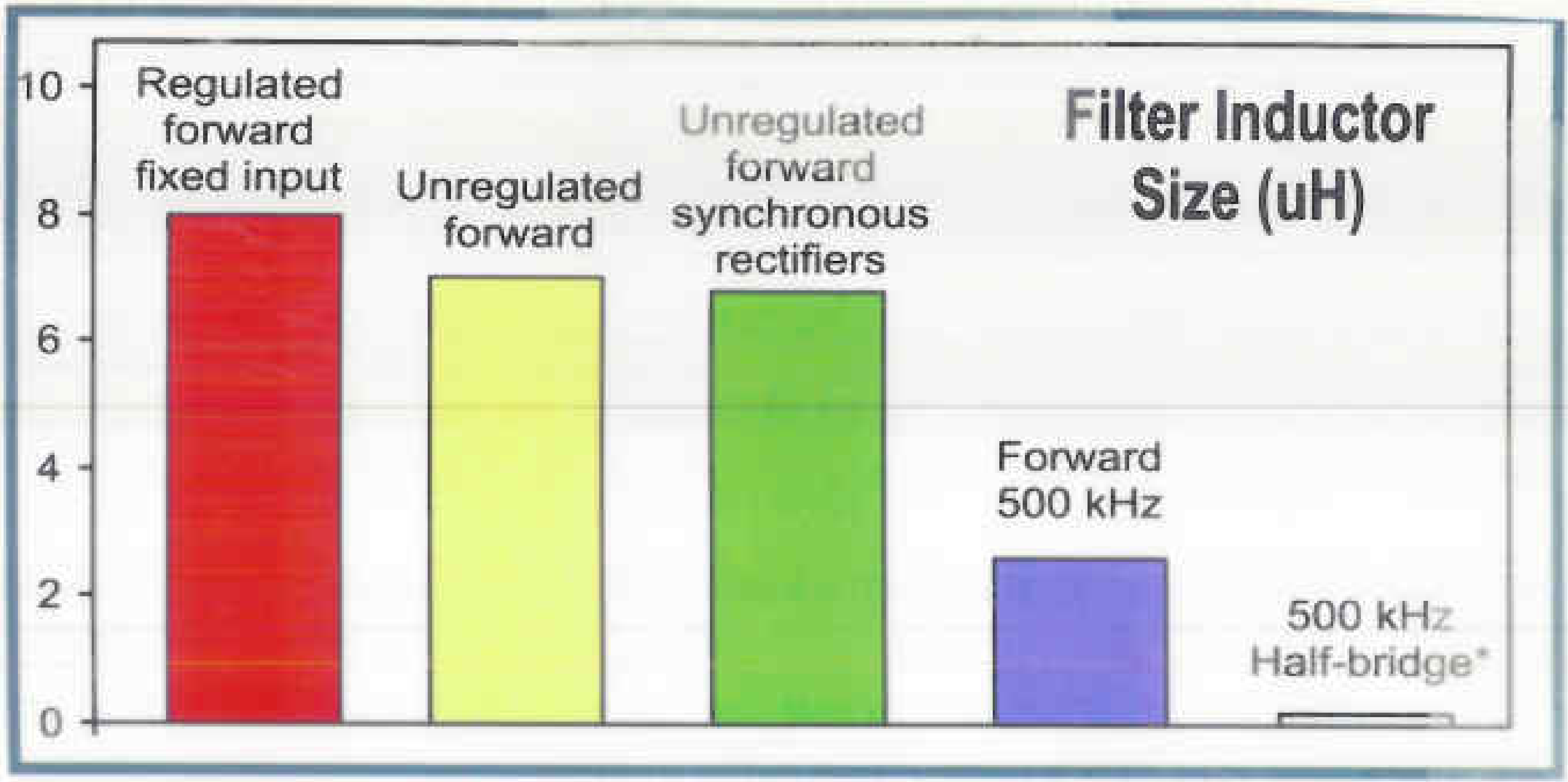
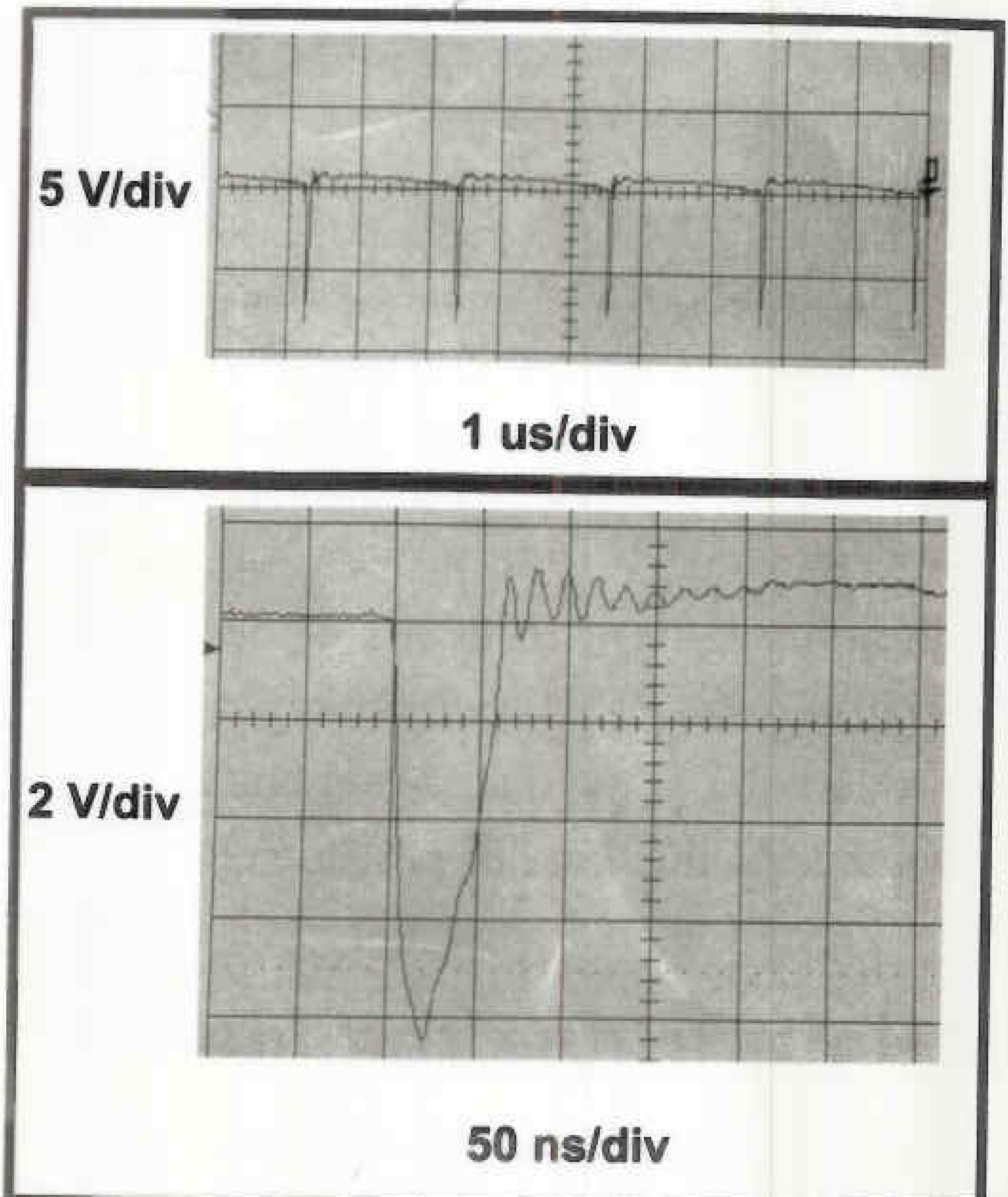


Figure 3b: Forward and half-bridge inductors



gure 5: Half bridge output voltage ripple at 110 W load

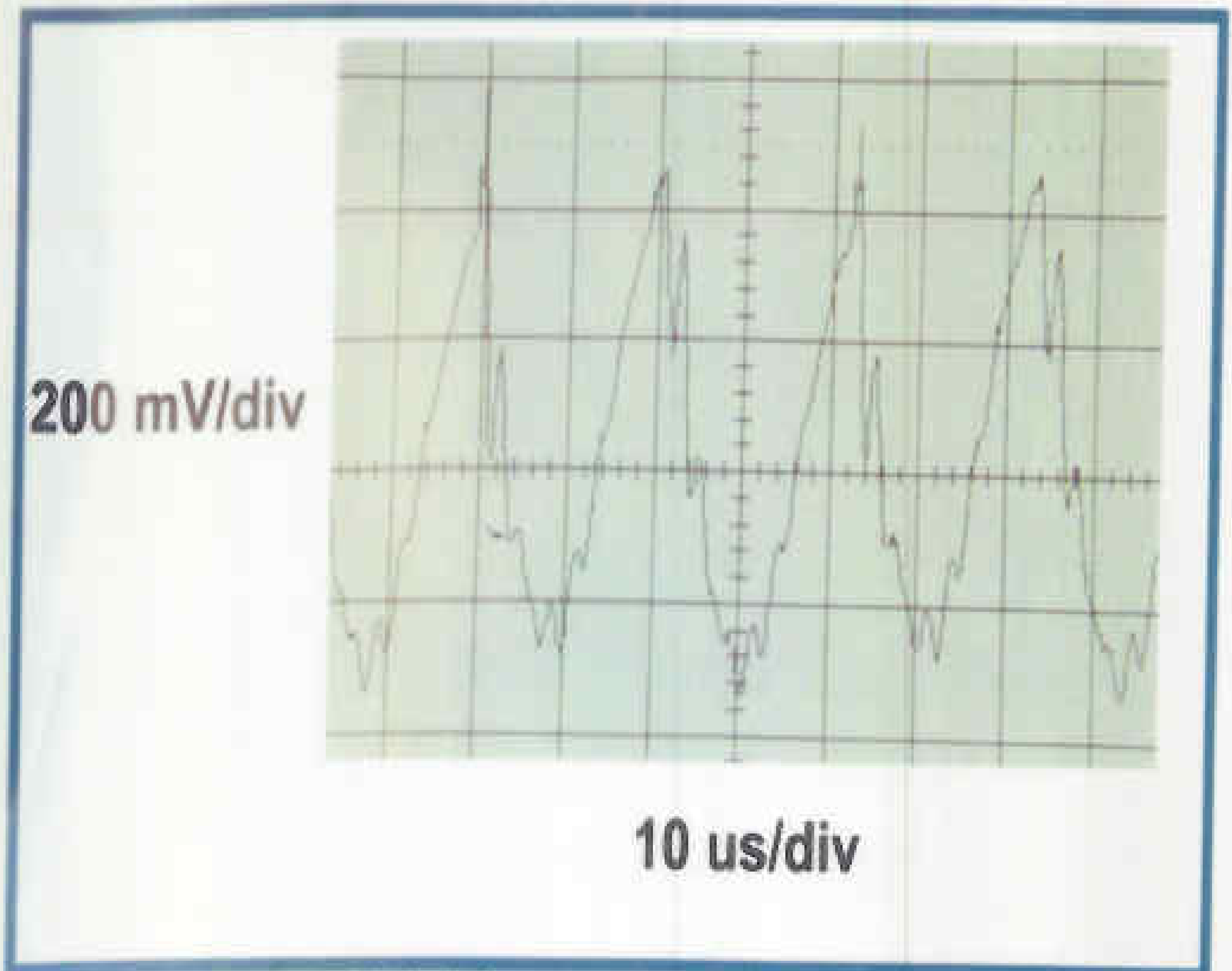


Figure 6a: Half bridge output voltage ripple at 110 W

LECTURE 11

Introduction to Feedback

Look Ahead to Ch 8/9 563

I. Feedback on PWM Converters

A. Why Employ Feedback?

3+, 1−

4

1. Improved Stability
2. Lower Z_{out} for Stiffer V(out) vs. I(out)
3. Faster Frequency Response
4. BUT Danger of Oscillation is introduced by feedback

B. How to implement feedback

1. Voltage Feedback – Power control
2. Current Feedback – f feedback IN ?

C. Various Semiconductor Control Chips and Switch Device Components

III. Transient Effects

A. Start Up

B. Other

DC – DC converter spec

Topology ? — requirements, choose a switching regulator topology[2] — you "choose" in Ch 6 HW

562	Black Box Calculations	Determine semiconductor parts and locate any trouble spots	V_{max}, I_{max} } Ch 4
563	Transformer Design	Design transformer, wire gauges, etc.	losses @ f_{sw} } Chs 13~15
562	Output Filter & Rectifier Design	Design output indicators & select rectifiers and capacitors.	losses @ f_{sw} } Chs 13~15
562	Power Switch & Driver Design	Design driver circuits	sw losses @ f_{sw} } Ch 4
563	Controller Design	Choose control mode & IC. Design basic functions.	i control, v control, P control } Ch 7, 8, 9, 10
563	Output Feedback Design	Design Voltage feedback & cross-regulation circuits	

1. Voltage Feedback (Chapter 8 and 9 of Erickson)

Feedback itself, in PWM dc-dc converters, can operate in two circuit modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The former has well orchestrated control of switches while the later has intervals controlled by the circuit and not the switch drivers.

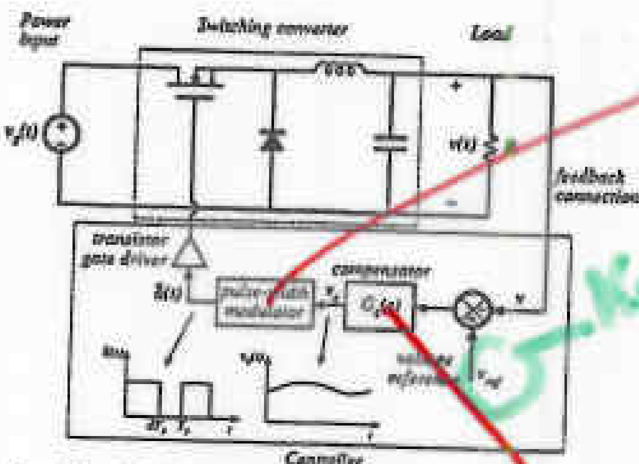


Fig. 7.1. A simple dc-dc regulator system, including a buck converter power stage and a feedback network.

PWM is Key to F. B.

$$A_{OL} = \frac{\Delta v_{out}}{\Delta D}$$

Loop gain with respect to duty cycle

G - Key

563

$\frac{V_{out}}{d}$ is trf. function

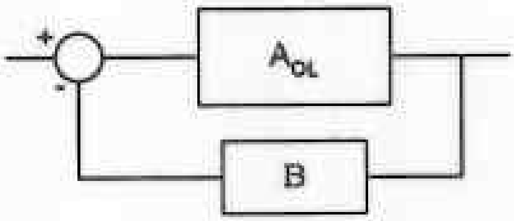
We will find later that for the same feedback loop on the same converter operating either in continuous conduction mode (CCM) or operating in discontinuous conduction mode (DCM) will have two very different closed loop gains and dynamic conditions:

Short Dtr of CCM

a. CCM has two poles and we need to design carefully for phase margin of 76° to avoid oscillation.

b. DCM has only one pole in transfer function. It is unconditionally stable and will never oscillate.

saftey Adv of DCM

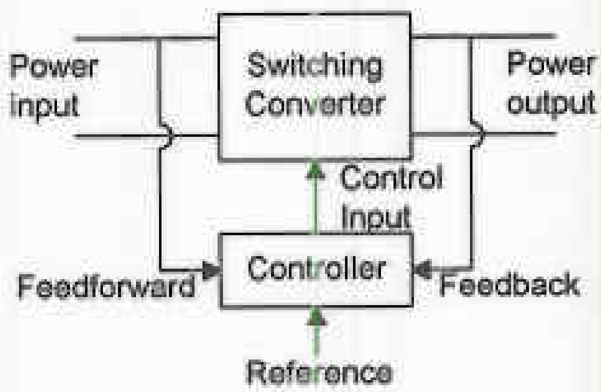


$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}$$

$\approx 1/\beta$ for large A_{OL}

This lecture is to give a view of the total system surrounding the PWM converter circuit. It is an awesome amount of auxiliary electronics around the simple PWM circuit but most of it is built into the commercial control and driver chips that we will employ. As a consequence we will have a broad but shallow coverage in this lecture with details of each portion of feedback, especially compensation of feedback, taken up again in second semester.

A. Why Employ Feedback?



1. Stability

$A_{OL} \rightarrow \infty$, $A_{CL} \sim 1/\beta$

so small variations in A_{OL} due to aging, thermal effects, or component variation have little effect.

2. Reduced Z_{out} to allow for large I_{out} at V_{out}.

$$Z_{out(CL)} = \frac{Z_{o(OL)}}{1 + A\beta}$$

Without feedback V_o/V_{in} determines D from M(D). With feedback D may vary dynamically to keep V_o fixed while V_{in} varies or the circuit changes.

I_L varies

3. Faster Frequency Response

Most converter transfer functions have at least two poles. Transient response for A_{OL} with two poles is much faster when using feedback due to gain-bandwidth product being constant. Reduced gain means wider bandwidth and faster transient response. Hence, for DC-DC converters with feedback we will need to find $A_{OL}(\omega)$ in order to design proper transient response and evaluate:

$$A_{CL}(\omega) = \frac{A_{OL}(\omega)}{1 + A\beta}$$ Loop gain vs. ω, see Ch. 7 of Erickson

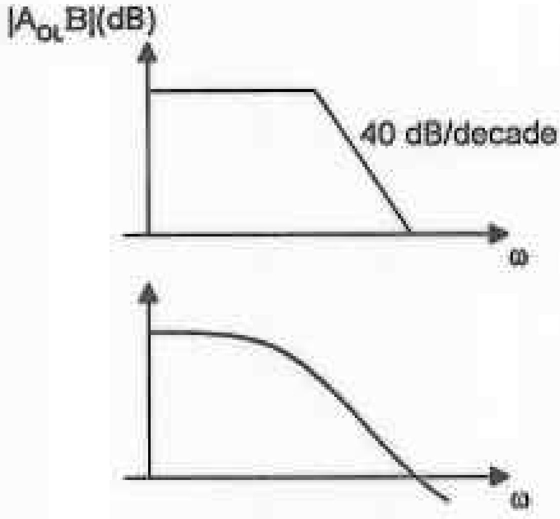
4. Danger of feedback is oscillation--if $A\beta \to -1$ then

$A_{CL} \to \infty$

Dark Side of -feedback

For two poles, phase shift may reach 180° at $|A\beta| = 1$.

This condition is well known to any audio system that suddenly starts to SCREECH.



$|A\beta| \rightarrow 1$ or 0 dB

and $\phi = 180°$

Recall from op amp design and control theory, one designs the feedback loop carefully such that undesired loop oscillation does not occur at any frequency. In some server computer power supplies or system tape drives, safe reliable operation is as important as speed - ultrasafe case.

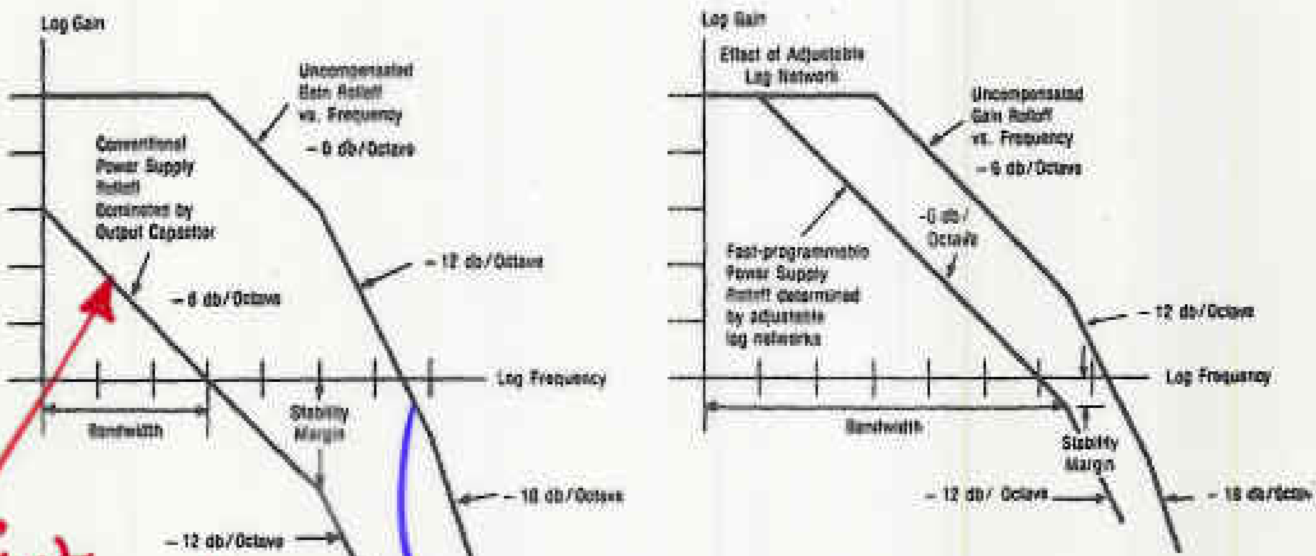
Ultra-safe case: cross unity gain of A_{OL} only at a slope of 20 dB/octave due to a single pole only. Only one pole in A_{OL} converters are made by design. Discontinuous mode and current programmed mode converters are examples of one pole transfer functions we can design for. See Chapter 10 and 11 of Erickson respectively.

1 pole always stable But slow response to transient disturb

We will see second semester that for an optimum feedback design we need to hit a specific value of phase margin for the open loop gain. This value gives the fastest response without any danger of oscillation.

Transient Response

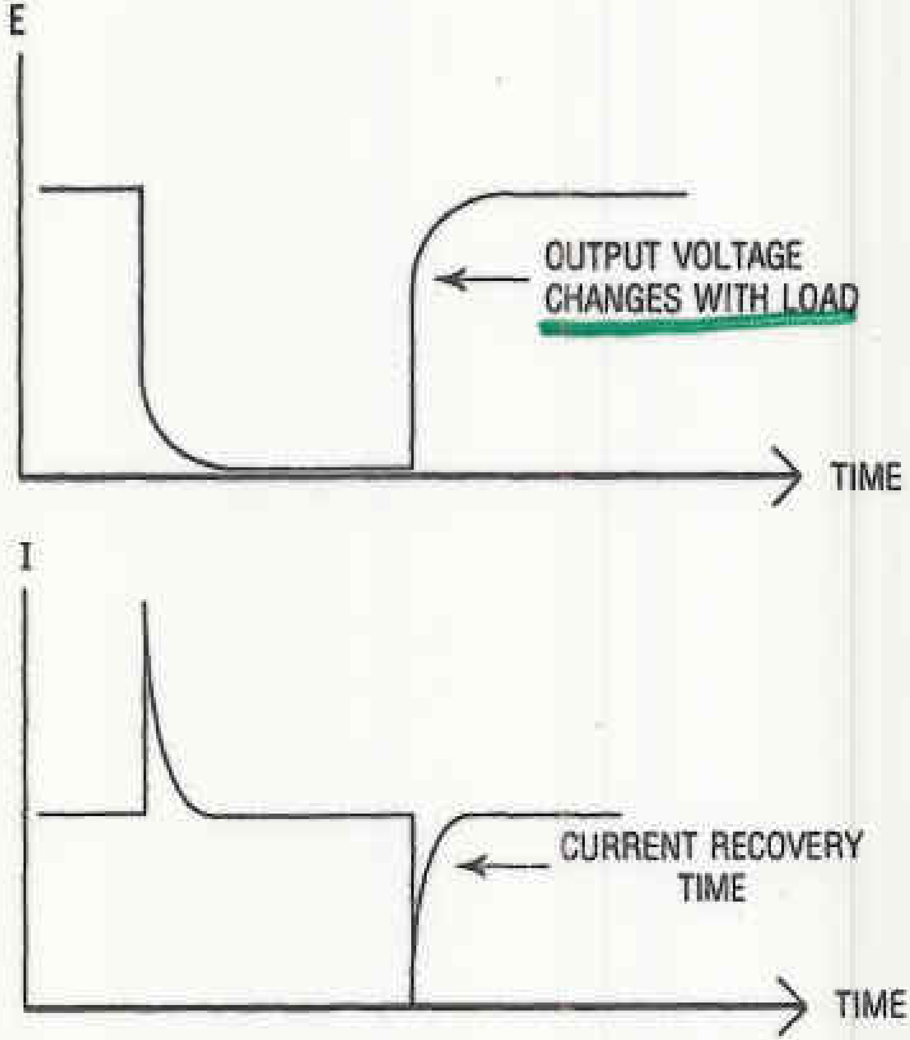
$$\Delta t \sim \frac{1}{\pi f_{cross\text{-}over}} \simeq \frac{1}{\pi BW}$$



C_{out} slow but stable

Fast dynamics but... unstable?

: A comparison of the gain-frequency (Bodé) plots illustrates the increased bandwidth that results when a power supply's output capacitor is removed.



The effect of a changing load on a current stabilizer. The output capacitor's charge and discharge time controls the recovery time.

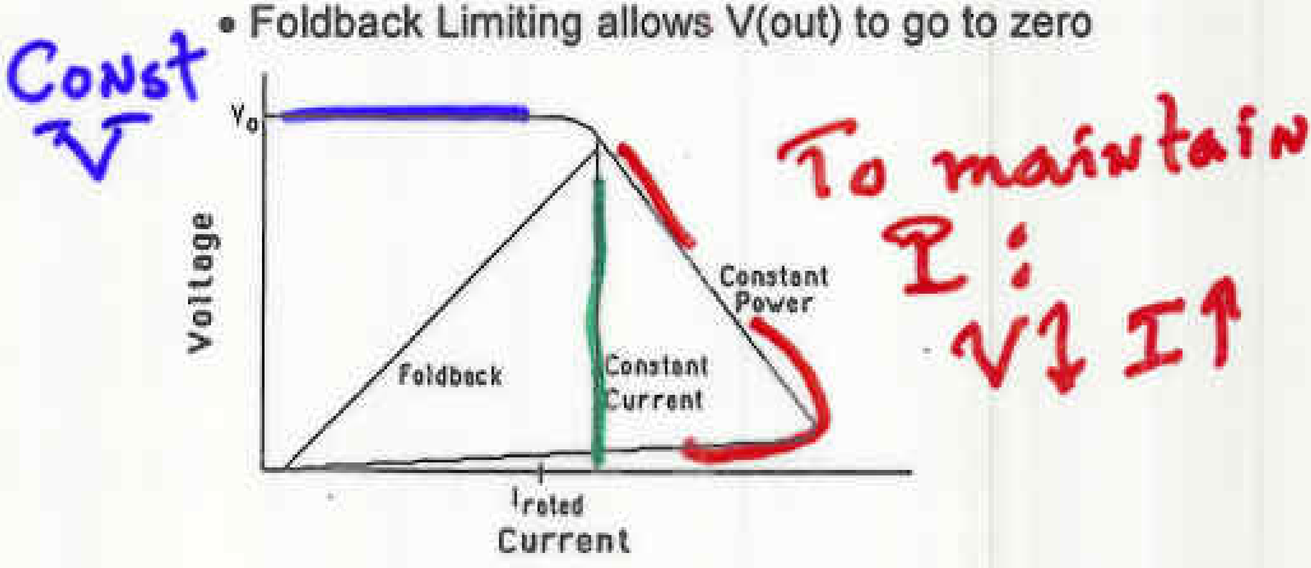
R_2 and V_2 provide a current to R_1 that is properly weighted as do R_3 and V_3 with their contribution. In total the current through R_1 will add so that the voltage across R_1 is equal to V_{ref} in equilibrium.

A more complex system with four outputs is illustrated with only three weights as the + and – 12 volts are similar.

d. Over current Protection

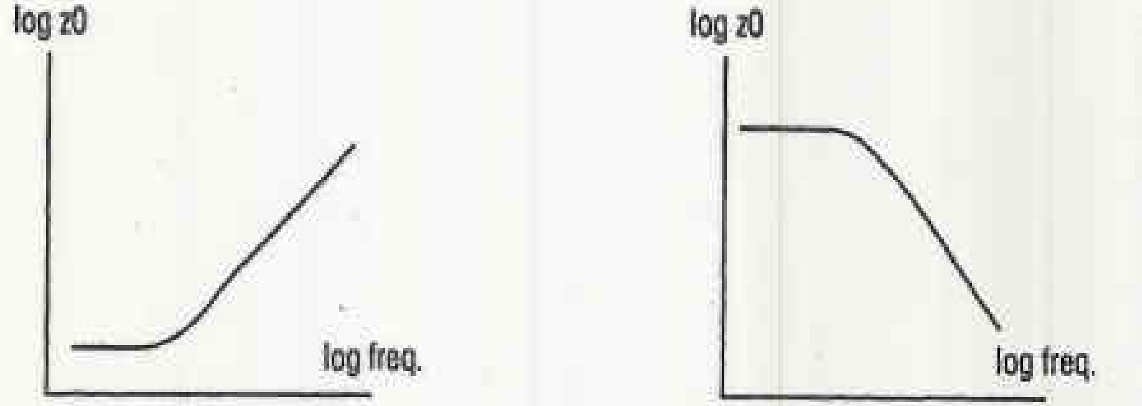
We want to protect against failures in the load, like an inadvertent short. There are three types of overcurrent protection.

- Constant Power limiting
- Constant Current Limiting
- Foldback Limiting allows V(out) to go to zero



Types of overcurrent protection.

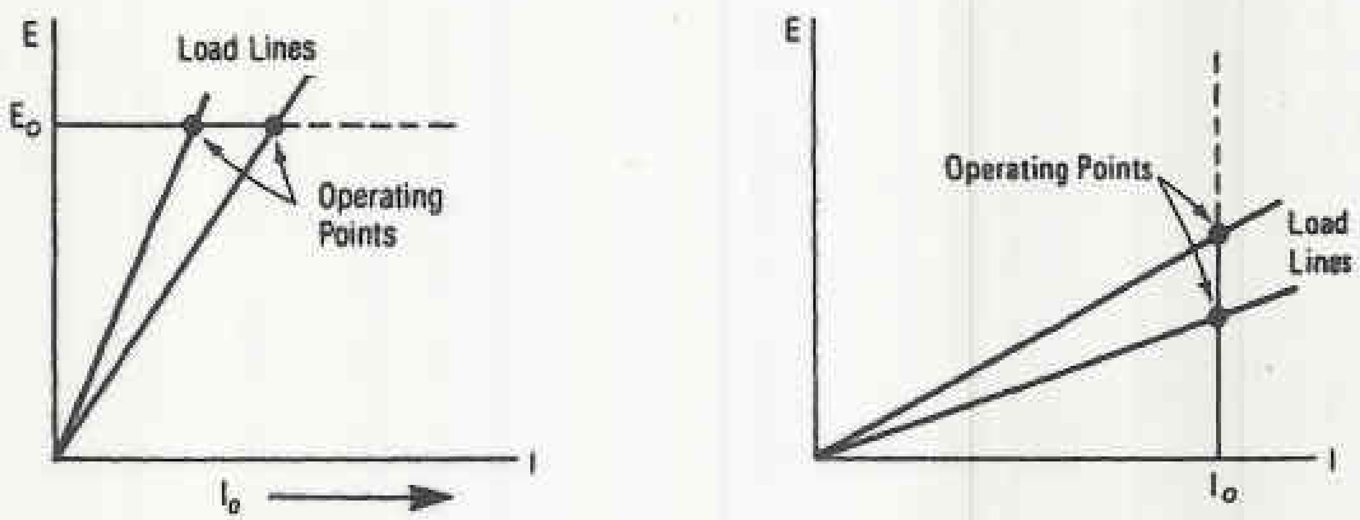
e. Overvoltage Protection



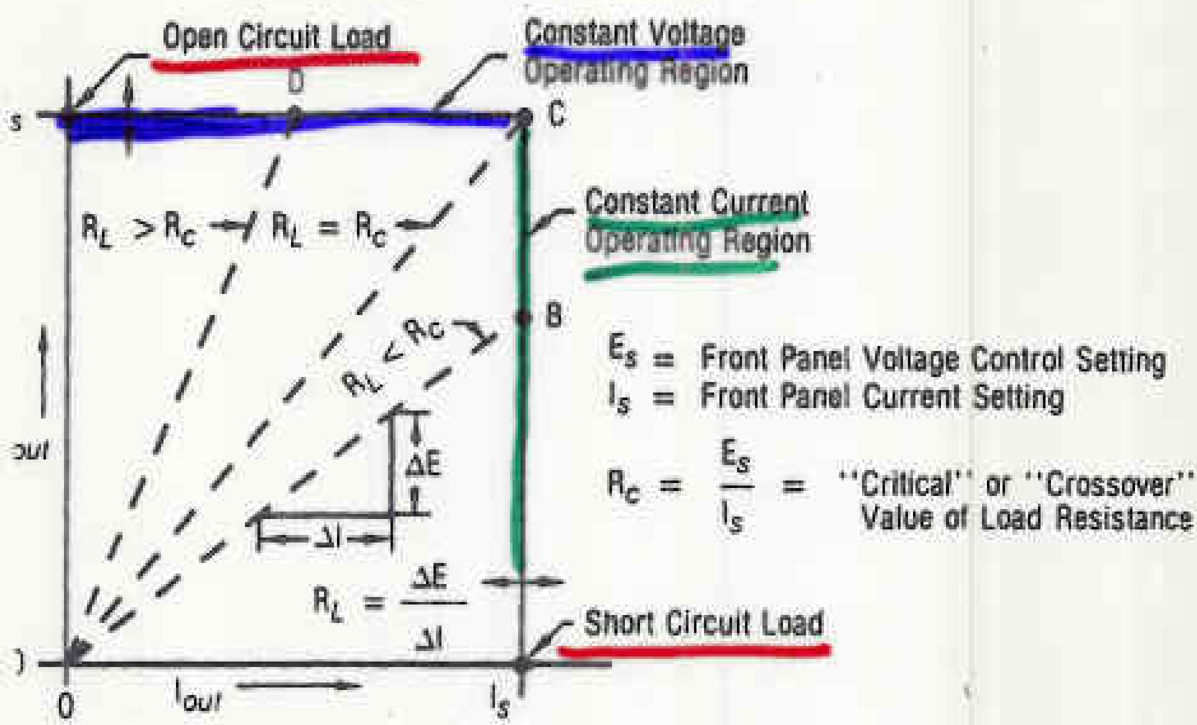
Voltage stabilizer's Impedance increases as an equivalent series inductance.

: Current stabilizer's Impedance decreases as an equivalent shunt capacitance.

Plot of output impedance vs frequency for a voltage stabilizer and for a current stabilizer.

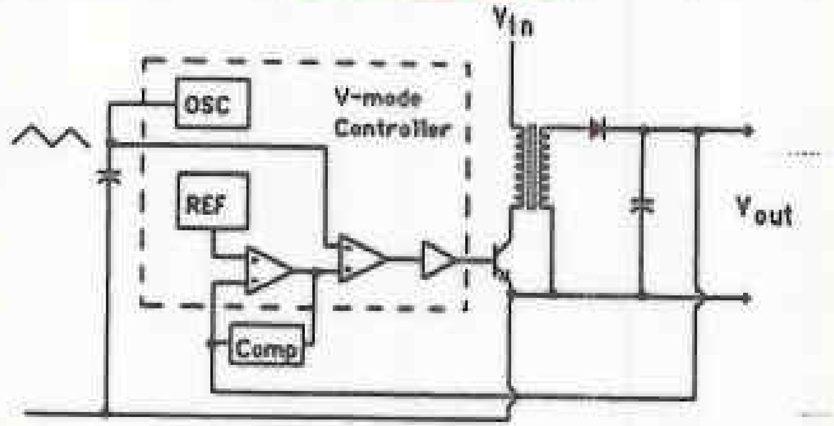


The concept of "voltage stabilization" or "current stabilization" relates to the locus of points that a varying load will trace if you observe the changing output voltage and current of the power supply being loaded.



The rectangular locus of an automatic crossover design in which the voltage mode serves to protect the current from overload and vice versa.

In summary for voltage feedback we have:



Voltage-mode control.

• Has a characteristic comparator fed by the output voltage and the ramp voltage across a timing capacitor

• V control is slow and cannot protect against fast current transients in the power switch

• the transient response is too SLOW to protect switches

• Many switch failures occur due to core saturation of inductors when using V control

2. Current Programmed Mode Feedback CPM PWM converter—Chapter 10 of Erickson

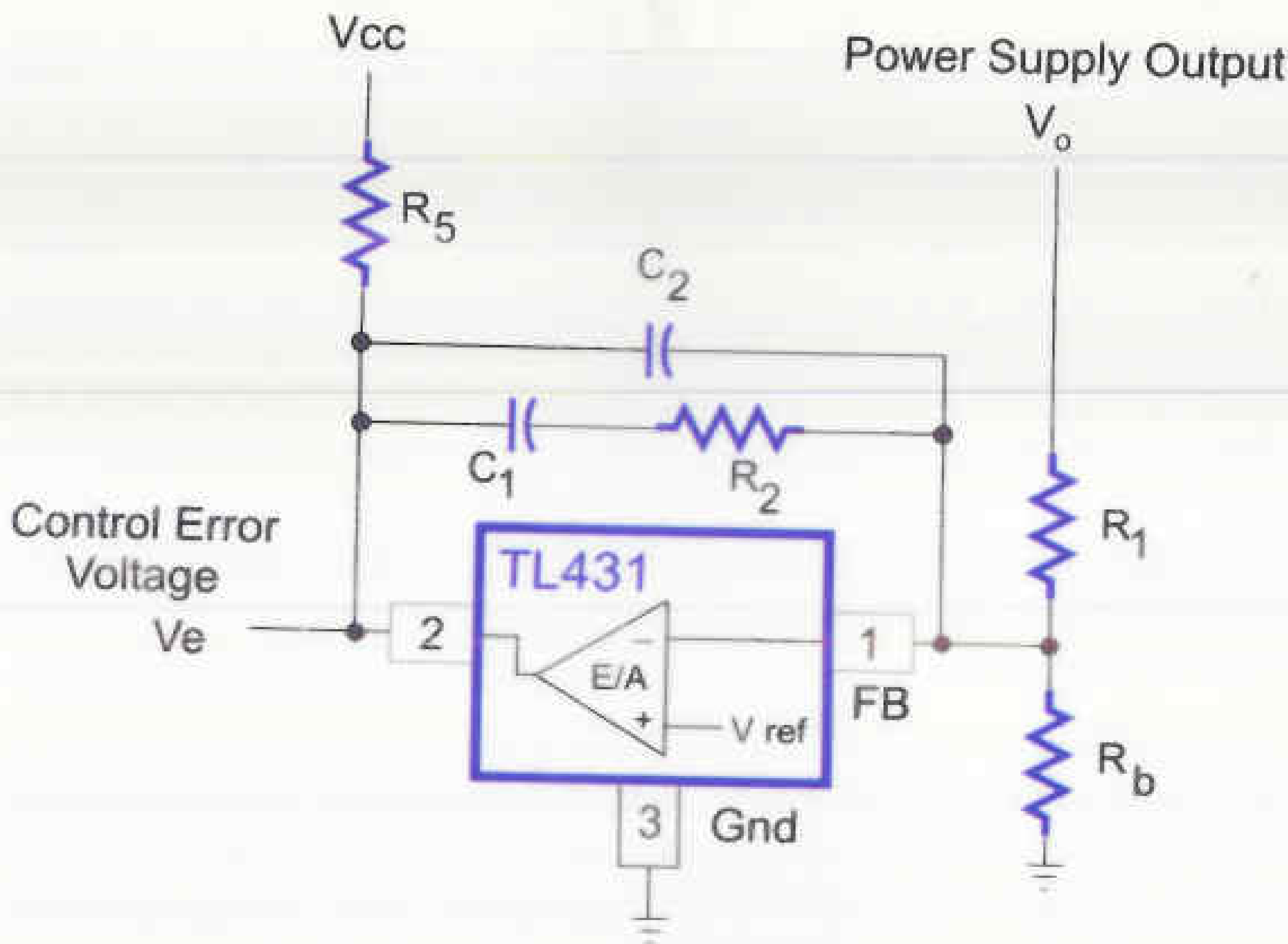
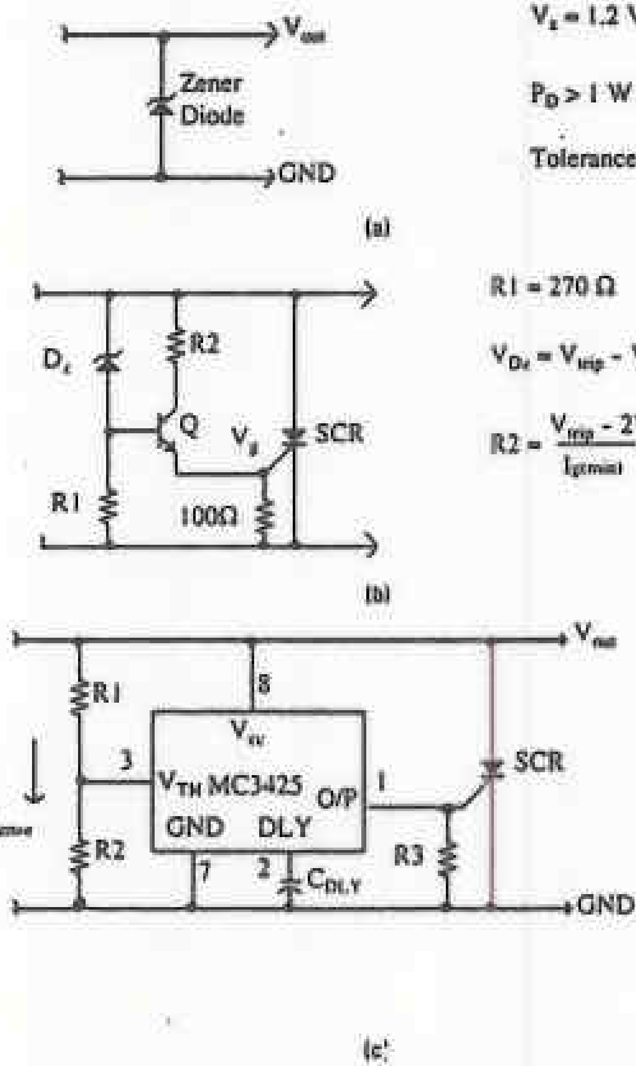


Figure 2: TL431 Used as a Type II Amplifier

power supplies at the time, it didn't make any sense to me to use a lower performance part than the best amplifiers that were available.

We assume that the feedback loop has opened or the load current on one output has gone to zero causing the voltage to rise above the maximum specification. In this case we need separate hard wired output sensors and a separate comparator to activate override of the error amplifier as shown below via three approaches

Overvoltage protection $V > V_z$



$V_z = 1.2\ V_{out(rated)}$

$P_D > 1$ W

Tolerance $\leq 5\%$

$R1 = 270\ \Omega$

$V_{Dz} = V_{trip} - V_{BE} - V_{g(th)}$

$R2 = \dfrac{V_{trip} - 2V}{I_{g(min)}}$

i crowbar

$V_{trip} = 2.5V(1 + \dfrac{R1}{R2})$

$I_{sense} = 1$ mA

$R2 = \dfrac{2.5\ V}{I_{sense}}$

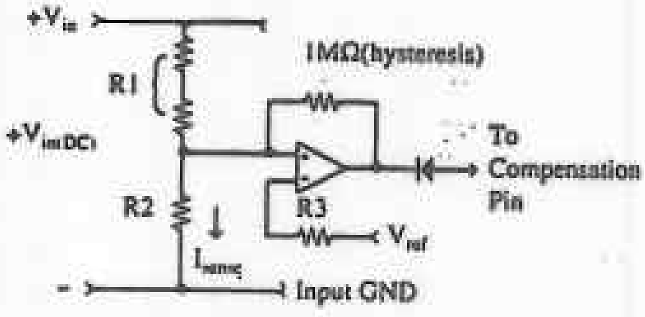
$R1 = \dfrac{V_{trip} - 2.5\ V}{I_{sense}}$

$C_{DLY} = \dfrac{V_{DLY}}{12{,}500}$

Overvoltage protection schemes: (a) Zener diode clamp; (b) overvoltage crowbar; (c) integrated overvoltage crowbar.

f. Undervoltage Shutdown

Here we assume that brownout conditions occur at the input which could inadvertently cause the duty cycle to latch up to unity and lose control. A simple comparator sensing the line input will avoid this case as shown below.



$$R2 = \frac{V_{ref}}{I_{sense}}$$

$$R1 = \frac{V_{in(min)} - V_{ref}}{I_{sense}}$$

$$R3 \cong \frac{(R1)(R2)}{R1 + R2}$$

Op Amp: MC33172P

A typical input undervoltage shut-down circuit.

If a logic or microprocessor chip as well as a hard disc drive is driven by a power supply we may also need a POWER ABOUT TO FAIL signal be generated to allow a sufficient time to institute a orderly shutdown. As much warning time as possible is desired. This is beyond today's discussion.

PSpice Models of Transients

III. Transient Effects

There are two separate effects we will consider. One is the isolated turn-on of the converter which has a long transient time to reach steady-state output. During this time the control chip and driver circuits may not be powered up in time. If this occurs, we may not be able to drive the switch properly and we can destroy the expensive power switch. The second is the fast switching at each T_s which causes losses as we try tomaintain the output.

A. Slow turn on vs. steady state

Ch 12 pg 439

Key is clock & RS flip-flop

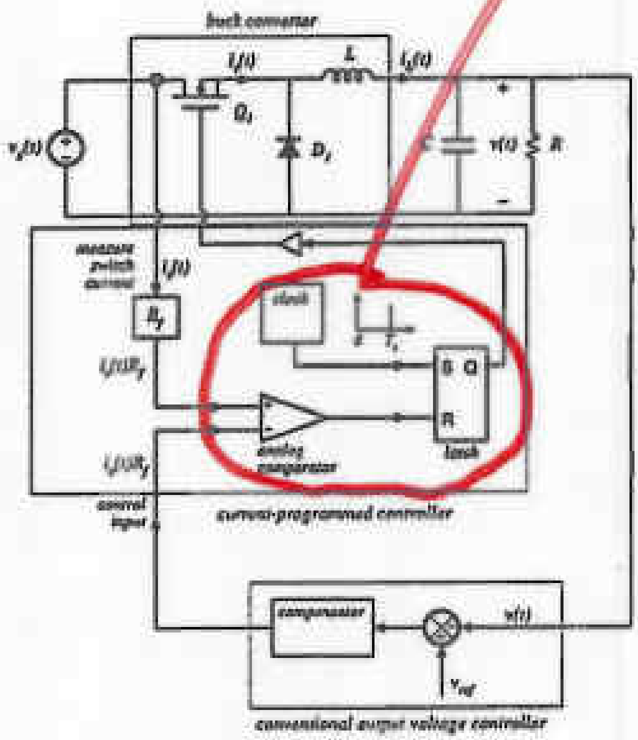


Fig. 11.1. Current-programmed control of a buck converter. The peak transistor current replaces the duty cycle as the control input.

To protect costly solid state switches we often monitor i_s anyway to avoid I_{pk}. So why not utilize this monitor for current feedback? Combine i_s monitor and conventional v_{out} controller to set D and D'. Both changes in Vo and is will cause compensating changes in D to fix system parameters we desire fixed.

Consider for now only current feedback signals:

i limit

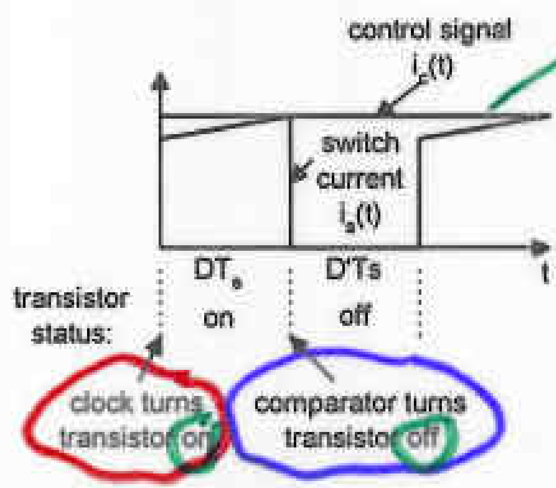


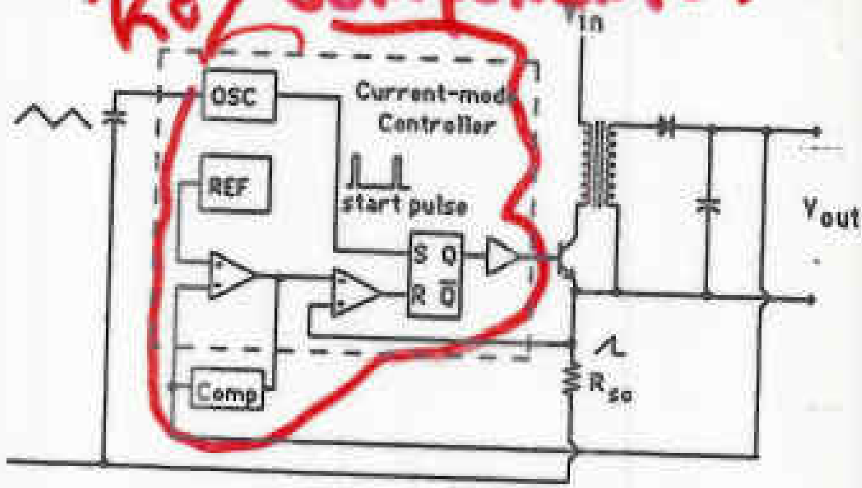
Fig. 11.2 Switch current $i_s(t)$ & control current $i_c(t)$ waveforms for the current programmed system of Fig. 11.1.

I_s is compared to $I_{control}$ to set D and D' the transition from D to D' is set when $I_s > I_c$

Ref, feedback

In summary for current feedback we have:

Key components: OSC, RS flip-flop



A current-mode controller.

• Characterized by a comparator fed by the difference between the error voltage and the instantaneous power switch current. Modern switch devices have on board current sensors to protect the switch from over current

•Now peak currents are sensed immediately and switches protected in a more direct and faster responding manner. This reduces costly field replacement of switches.

•

C. Various Semiconductor Control and Switch Device Components

1. Overview

The three major categories of PWM converter parts, for the PWM parts bill of lading, are given below.

a. <u>Cheap IC controller chips exist with many on-board capabilities:</u>

vout ~ -cos ωt

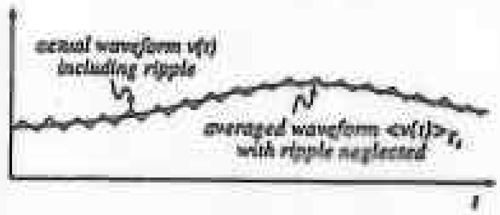


Fig. 7.2. Ac variation of the converter signals: transistor gate drive signal, in which the duty cycle varies slowly, and the resulting converter output voltage waveform. Both the actual waveform $v(t)$ (including high frequency switching ripple) and its averaged, or low-frequency component, $\langle v(t) \rangle_{T_s}$ are illustrated.

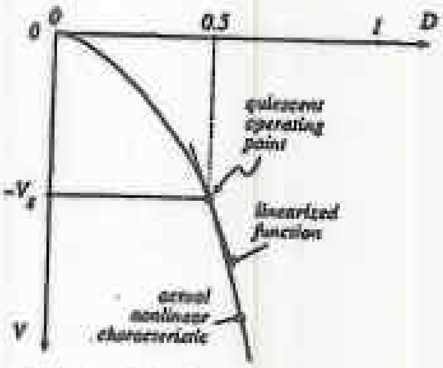


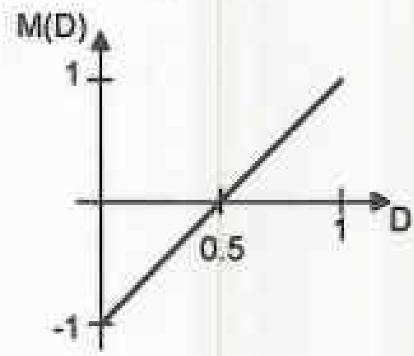
Fig. 7.5. Linearization of the static control-to-output characteristic of the buck-boost converter about the quiescent operating point $D = 0.5$.

How could we get a sinusoid centered about zero volts?

(2) Bridge-inverter case: voltage fed, not current fed

In a fixed D operation we find $V_{out} = M(D)V_{in}$.

$$\frac{V_{out}}{V_g} = 2D - 1$$



Noting that the output is symmetric about 0.5. We set D=0.5 and V_o=0. Add a time varying component $D = 0.5 - \Delta d \cos \omega t$ to achieve sinusoidal output around zero volts.

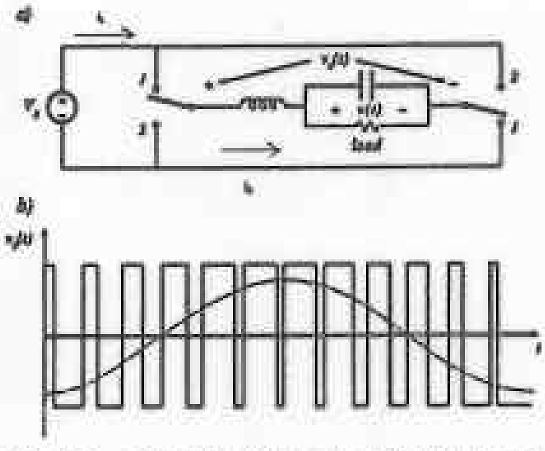


Fig. 1.13. A bridge-type dc-1øac inverter: (a) ideal inverter circuit, (b) typical pulse-width-modulated switch voltage waveform $v_s(t)$, and its low-frequency component.

Later we will model the two synchronized SPDT switches by a switch averaged two port model.

(b) DC-DC converter with feedback

To better stabilize DC-DC converters, we use feedback that looks at a fixed V_{ref} compared to the changing V_{out}, which sets the proper D for desired V_o dynamically. If V_o varies for whatever reason then the on duty cycle D varies to stabilize V_o back to the desired value.

D will become a function of time rather than a constant and the transfer function of the inverter becomes the output voltage divided by the duty cycle $\frac{V_o}{d}$ will be valid.

On the following page is a full schematic for a flyback converter. **FOR PRACTICE** look through the schematic to find the peripheral circuitry in a PWM:

- Input filter and rectifier circuit block
- Various Outputs
- Control and PWM Circuits

•timing components •current sensing

•PWM with variable D •switch drivers

(b) Power devices for switching: See Chapter 5 of text

•MOSFET's •IGBT's •diodes
•GTO (Gate turn-off Thyristor)
•MCT (MOS-Controlled Thyristor)

Choose

(c) Reactive elements:
•Capacitors •Inductors on cores

Choose

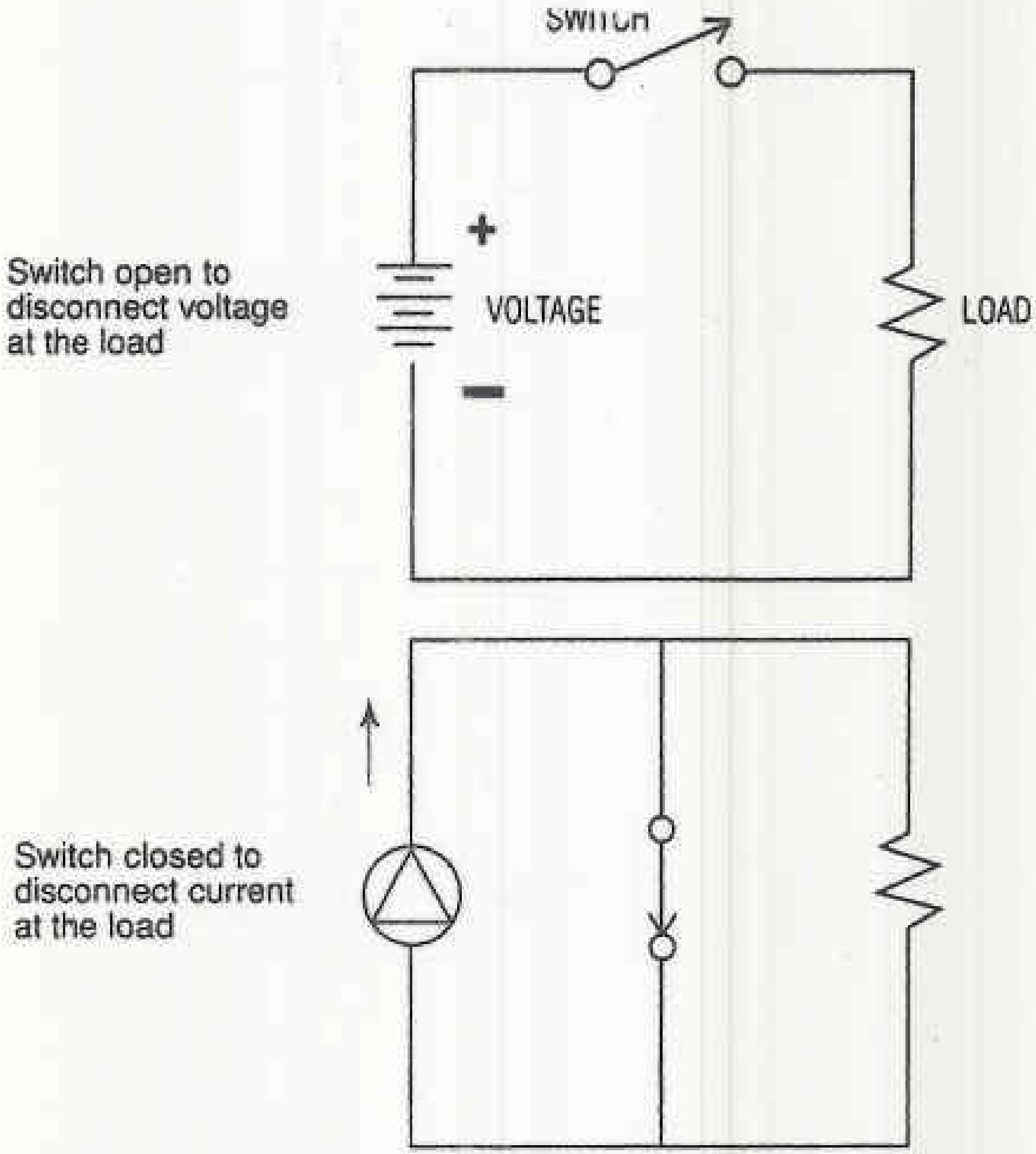
In practice **parasitic R, L, and C components** often **make up half the circuit model components though they do not appear on the bill of lading.**

2. Commercial Controller Chips

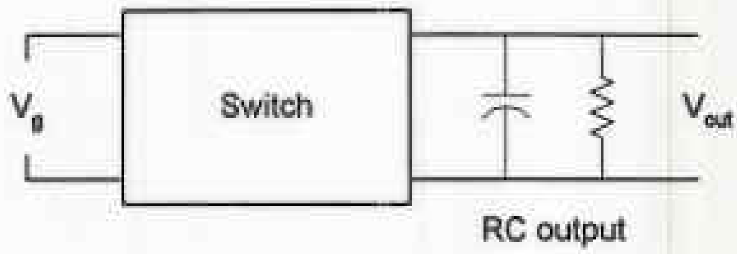
The controller chip is available from integrated circuit manufacturers at very low cost, yet, featuring a host of capabilities. Two types of control chips are listed on the next page. Features on board the chips include:

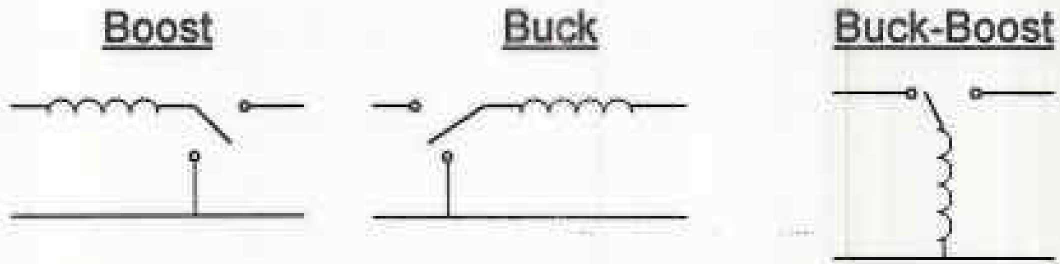
- Power MOSFET Drive Circuits for the power switch
- Multiple Output Sensing with Weighting of Each Output
- Over-current Shutdown circuits
- Over-voltage Protection Circuits
- Under-voltage Protection Circuits

a. Commercial Control Chips



Disconnecting voltage and current sources from their load

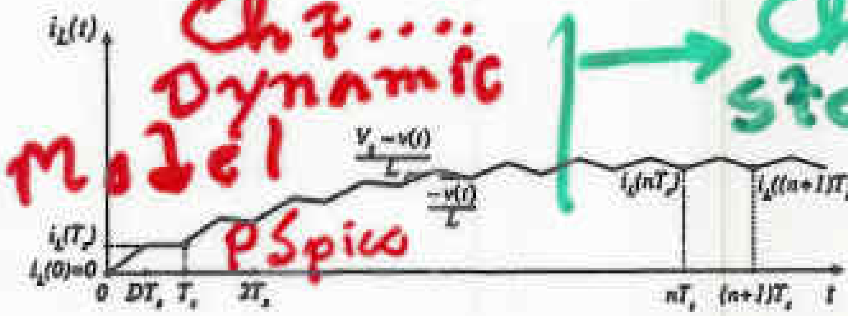




Consider buck case:

Apply V_g switch at f_{sw}.

Turn-on requires: @ $t = 0$, $i_L = 0$; @ $t = \infty$, $i_L = I_{out}$



Ch 7.... Dynamic Model

PSpice

Ch 1-6 steady state

Fig. 2.11. Inductor current waveform during converter turn-on transient.

di/dt

(1) Turn on:

Up-ramp slope @ $t = 0$: $s_u = \dfrac{V_g - 0}{L}$

Up-ramp slope @ $t = \infty$: $s_u = \dfrac{V_g - V_{out}}{L}$

Slopes change vs time during transients

Whereas the downslope ramp is always: $s_d = \dfrac{-V_{out}}{L}$

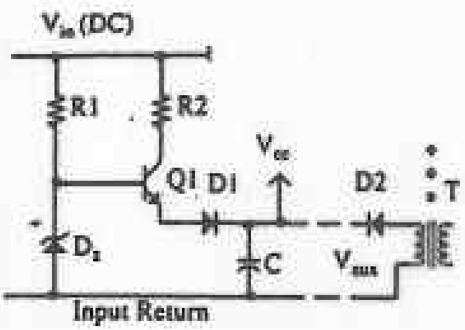
In both cases V_{out} varies from 0 to V_{out};

V_{out}(buck s.s.) = DV_g regardless of f_{sw}

Steady-state does have ac and dc for dc-dc converters

$v_{out} = V_{out}(dc) + v_{out}(ac) \leftarrow$ ac part is 0.1 to 10% at f_{sw}

We need a separate power supply IC when the input voltage is above the range for the control chip itself so that we can power up the control chip and the drivers BEFORE the power switch is toggled.Otherwise we could cause switch failure See one implementation using a linear regulator chip below.



R1: $R1 \le \dfrac{V_{in(min)} - V_{DZ}}{I_{DZ(min)}}$

R2: $R2 = \dfrac{V_{in(min)} - V_{DZ}}{I_{start}}$

D1: 1N4148 D2: MUR1X0

Dz: 500 mW, > $V_{cc(min)}$ of IC

Q1: $V_{CEO} > V_{in(max)}$, I_C = 300 mA

The high-voltage linear regulator bootstrap start-up circuit (used only at start-up and foldback periods).

(2) Steady state conditions for DC-AC converters or DC converters with feedback

(a) DC-AC converter case

(1) General case

By modulating the duty cycle at a frequency w_m we can change V_{out}, but only if $\omega_m < \omega_s$. That is from DC V_{in} we can get an AC output centered around a dc value.

$V_o = DV_g$, let $D = \cos \omega_m t \Rightarrow V_o = V_g \cos \omega_m t$.

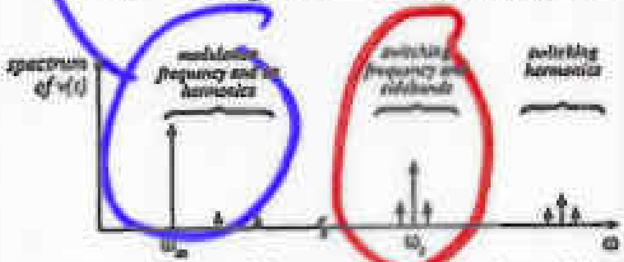


Fig. 7.3. Spectrum of the output voltage waveform $v(t)$ of Fig. 7.2.

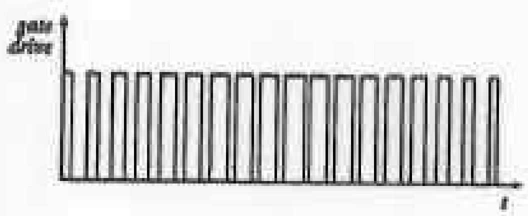
Fourier spectrum for

$D = \cos \omega_m t$

if $\omega_m \ll \omega_s$

RC output filter is chosen so it passes signals $\omega < n\omega_m$ and stops signals $\omega > n\omega_m$

For fixed D the $V_o = V_{in} M(D)$ is at a dc value. Next we let D vary with time as shown below.



For $D \sim \cos \omega t$ we can get ac output around an effective DC value by:

This sinusoidal D(t) will cause a sinusoidal $V_o(t)$.

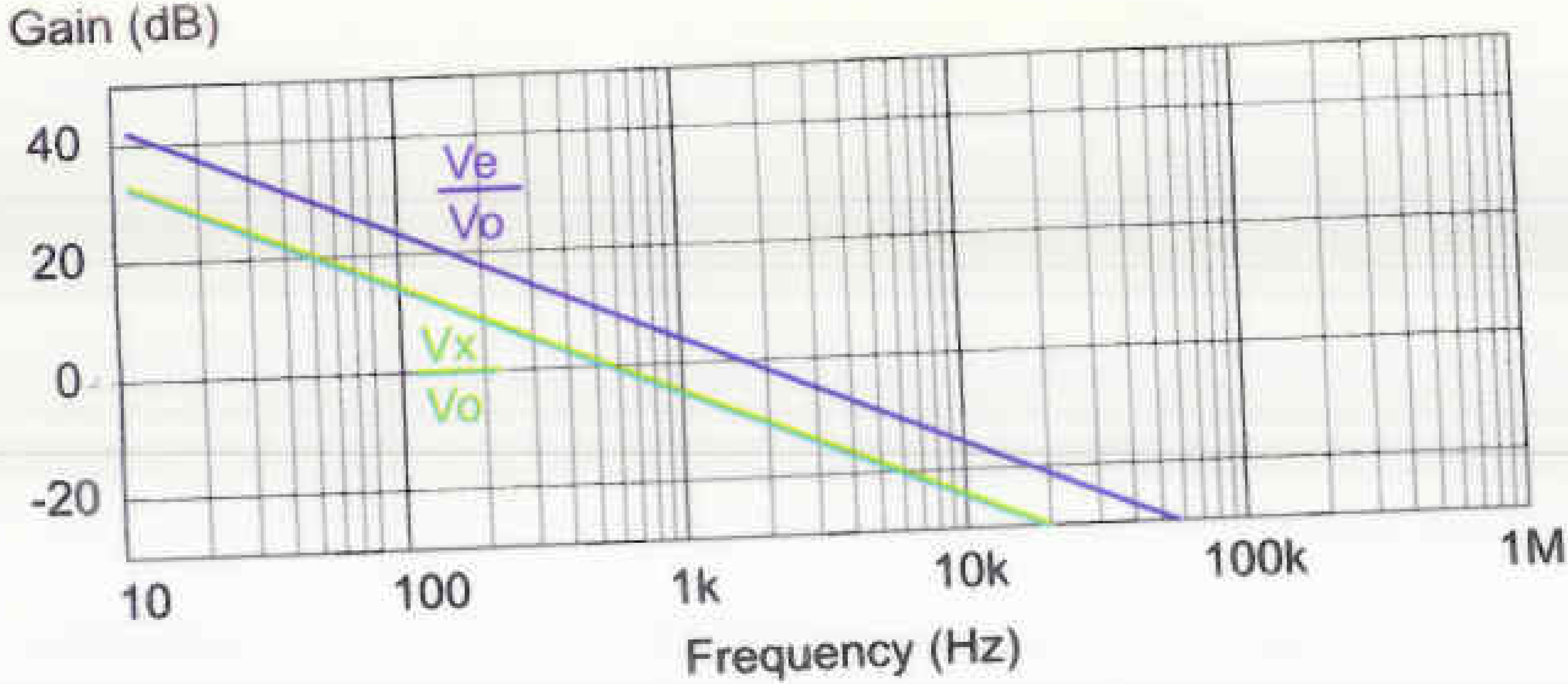
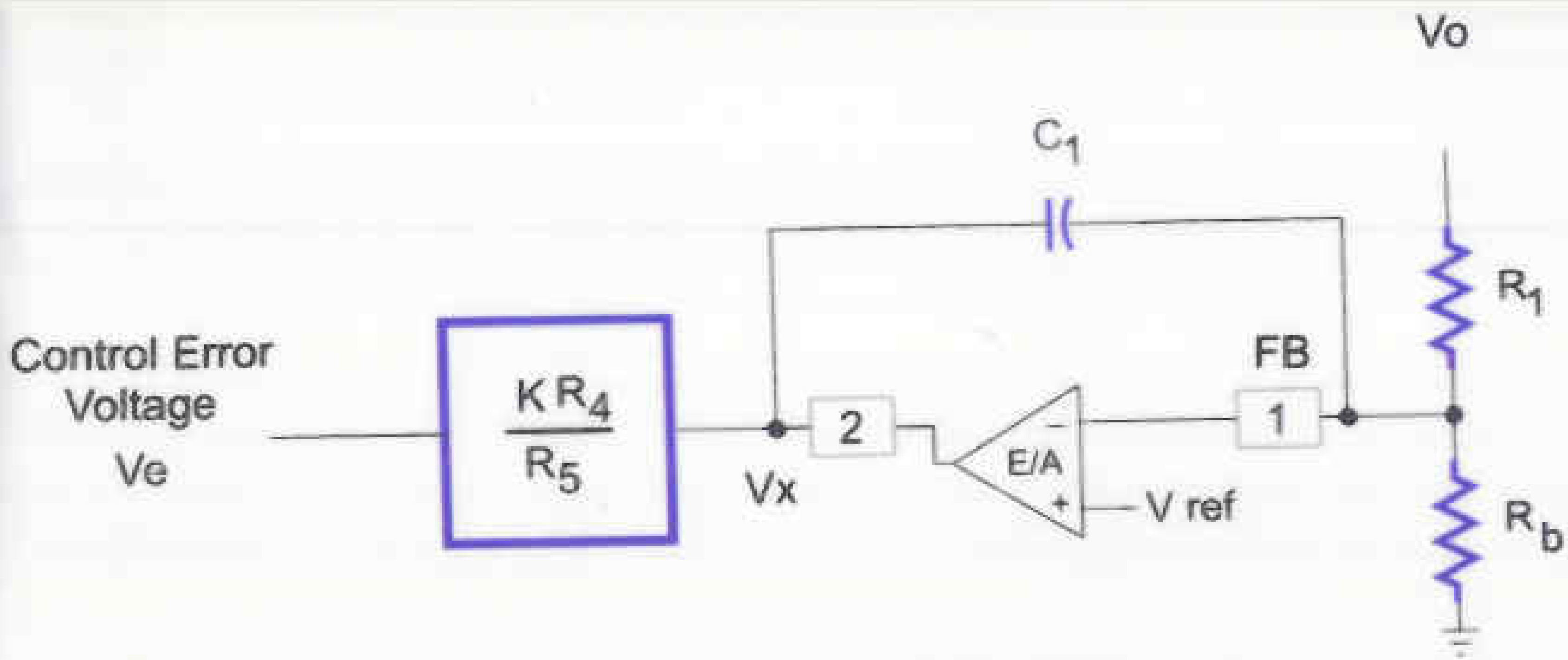


Figure 4b: Low Frequency Gain of Typical TL431 Circuit

4. TL431 Compensation - Mid Frequency

At a higher frequency, the gain of the integrator around the TL431 amplifier reaches unity, and beyond this point, the output signal is attenuated. However, there is always gain from ... output voltage to optocoupler diode current due to the



$$\text{Low Frequency Gain} = \frac{K R_4}{R_5} \frac{1}{SC_1R_1}$$

Figure 4a: Low Frequency Circuit for Typical TL431 Connection

Output

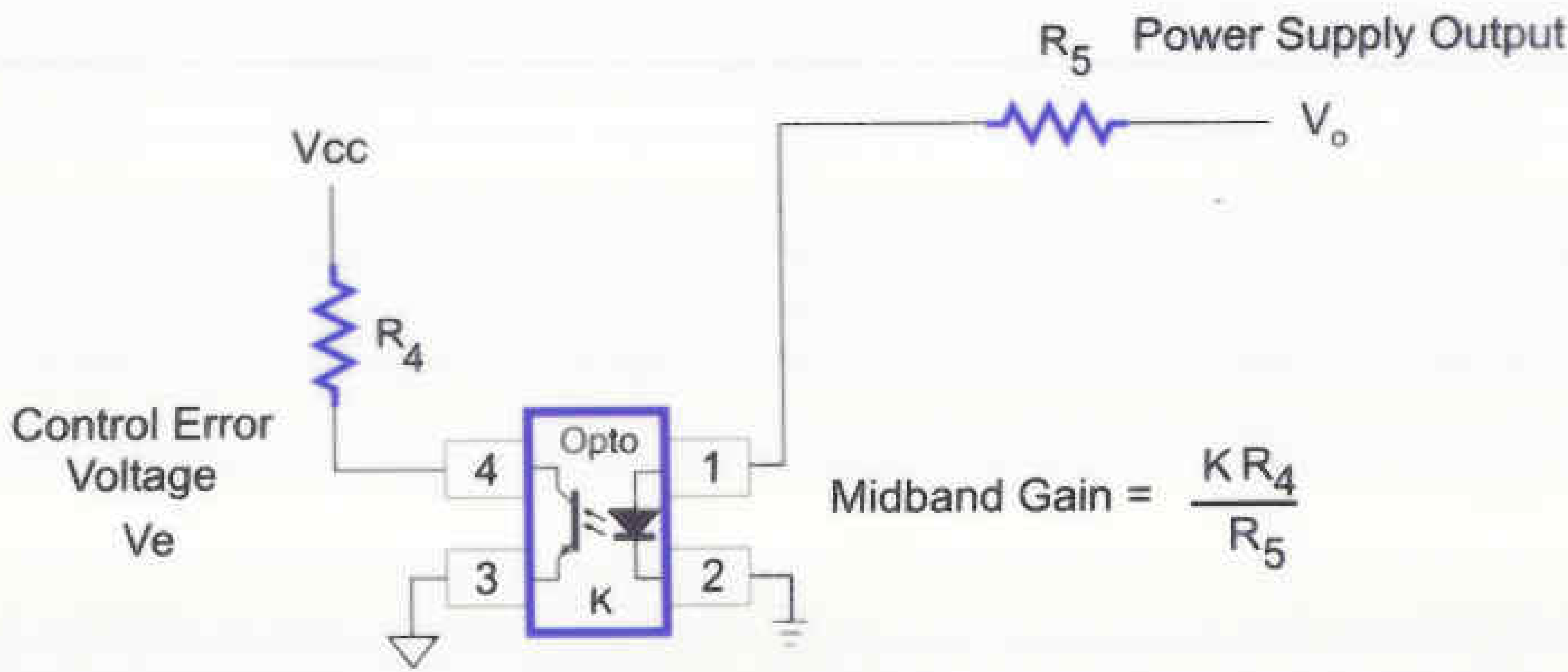


Figure 5: TL431 Circuit Midband Gain

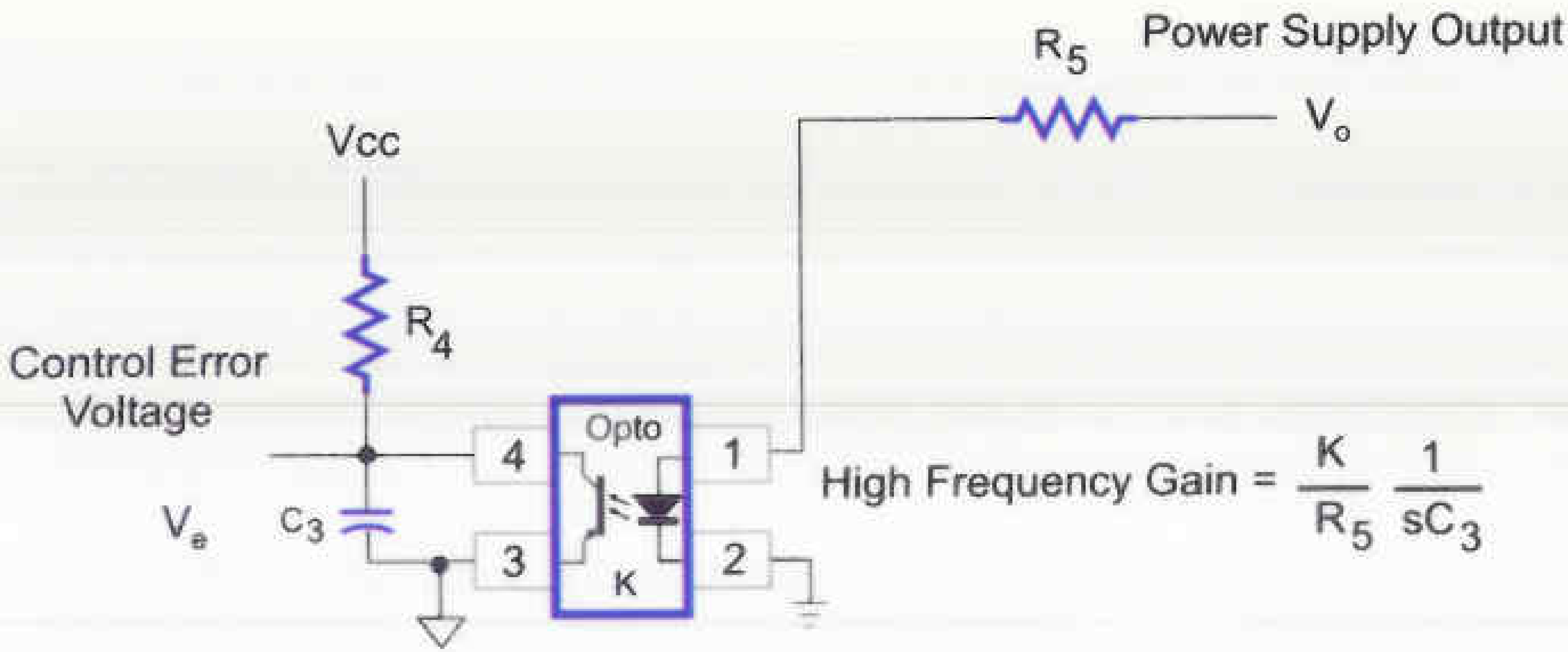


Figure 6a: TL431 High Frequency Gain Circuit

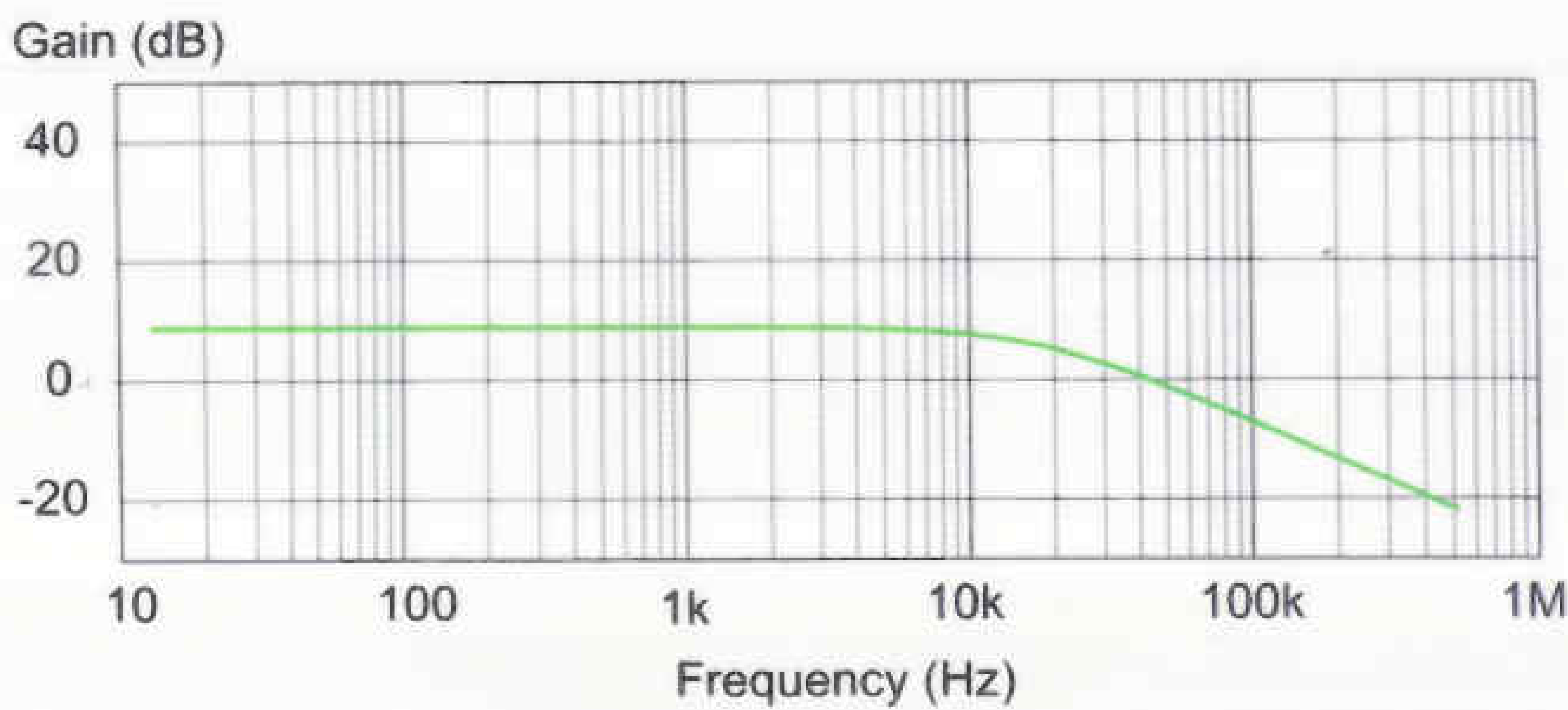


Figure 6b: Mid-Frequency and High-Frequency Gain Plot

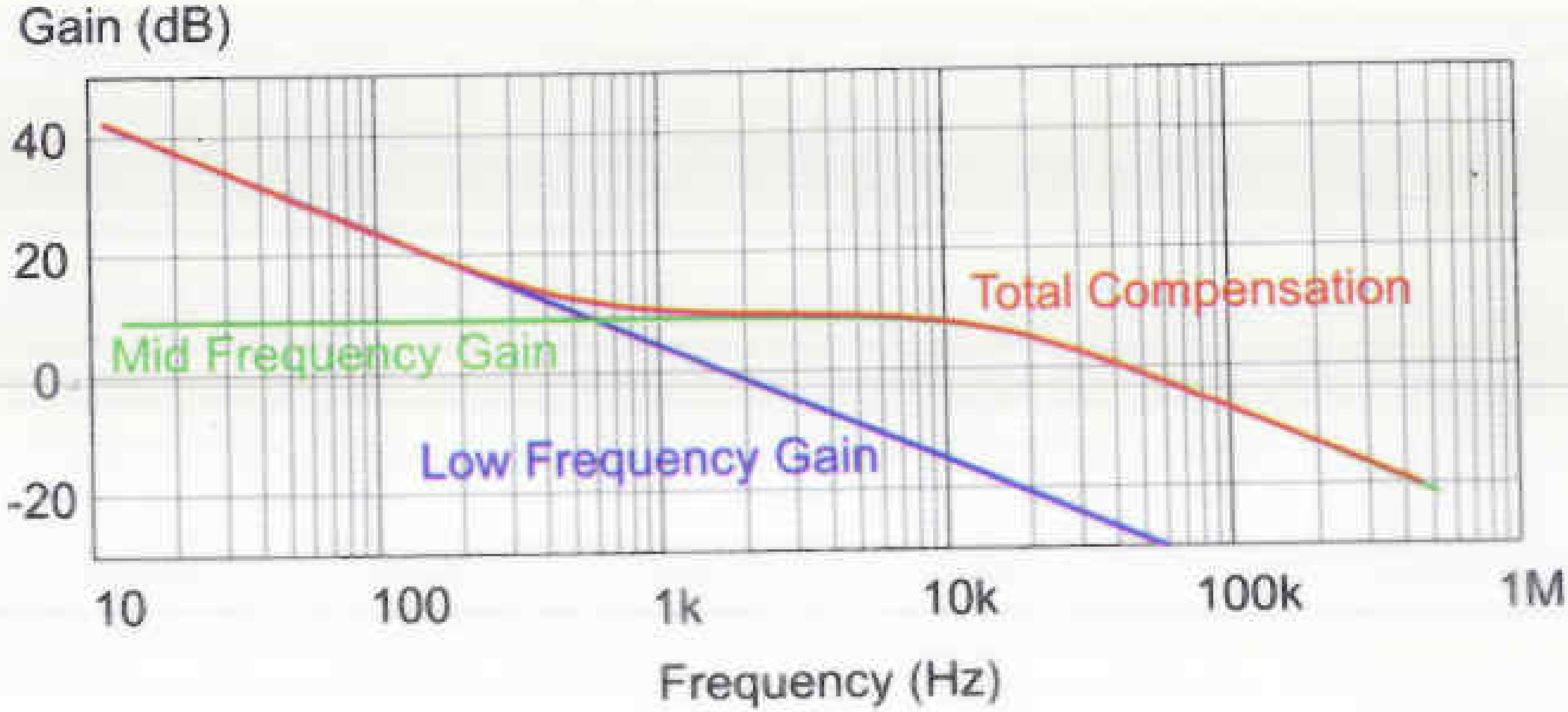


Figure 7: TL431 Final Compensation Gain

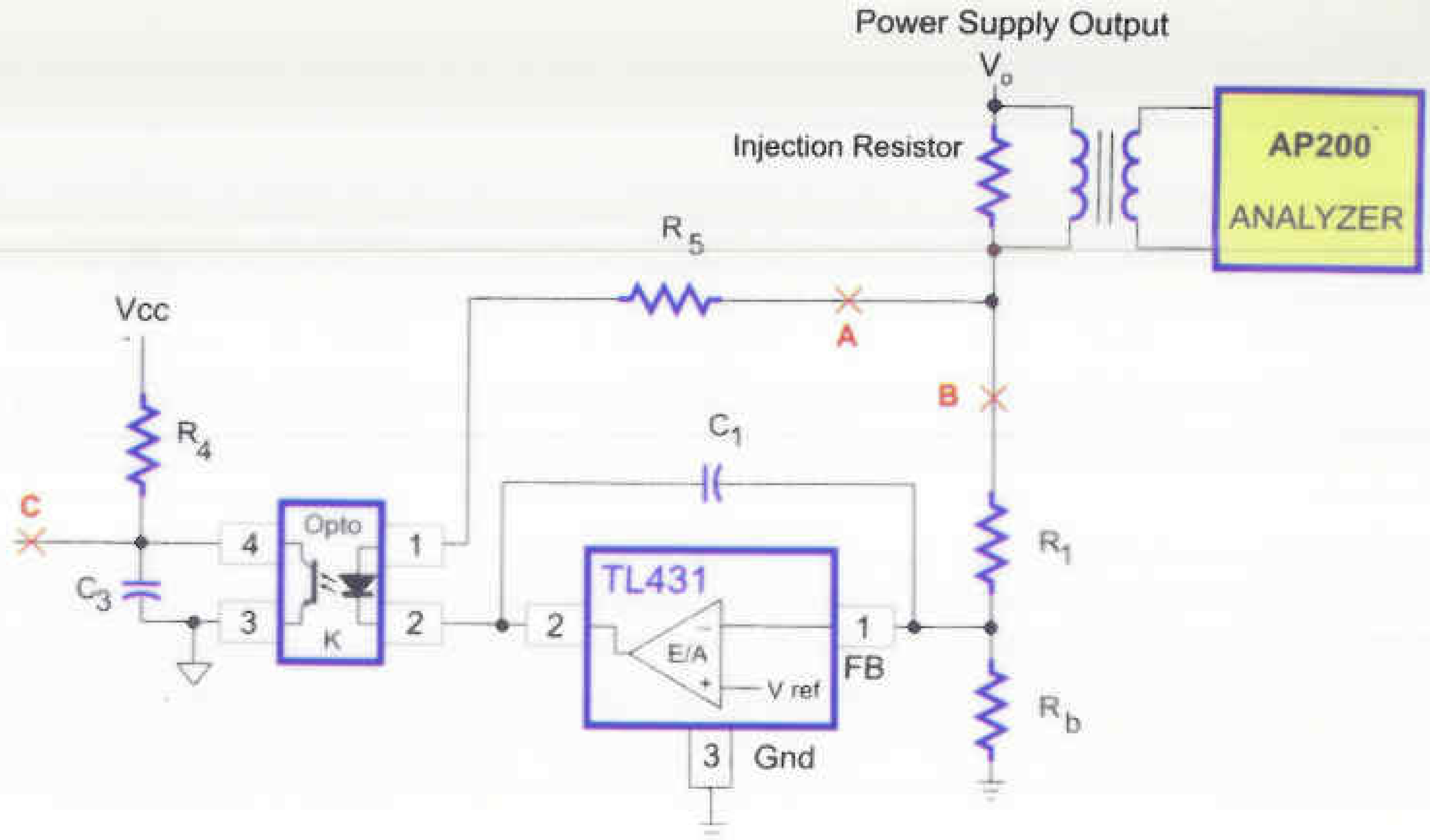


Figure 8: TL431 Loop Measurement Points

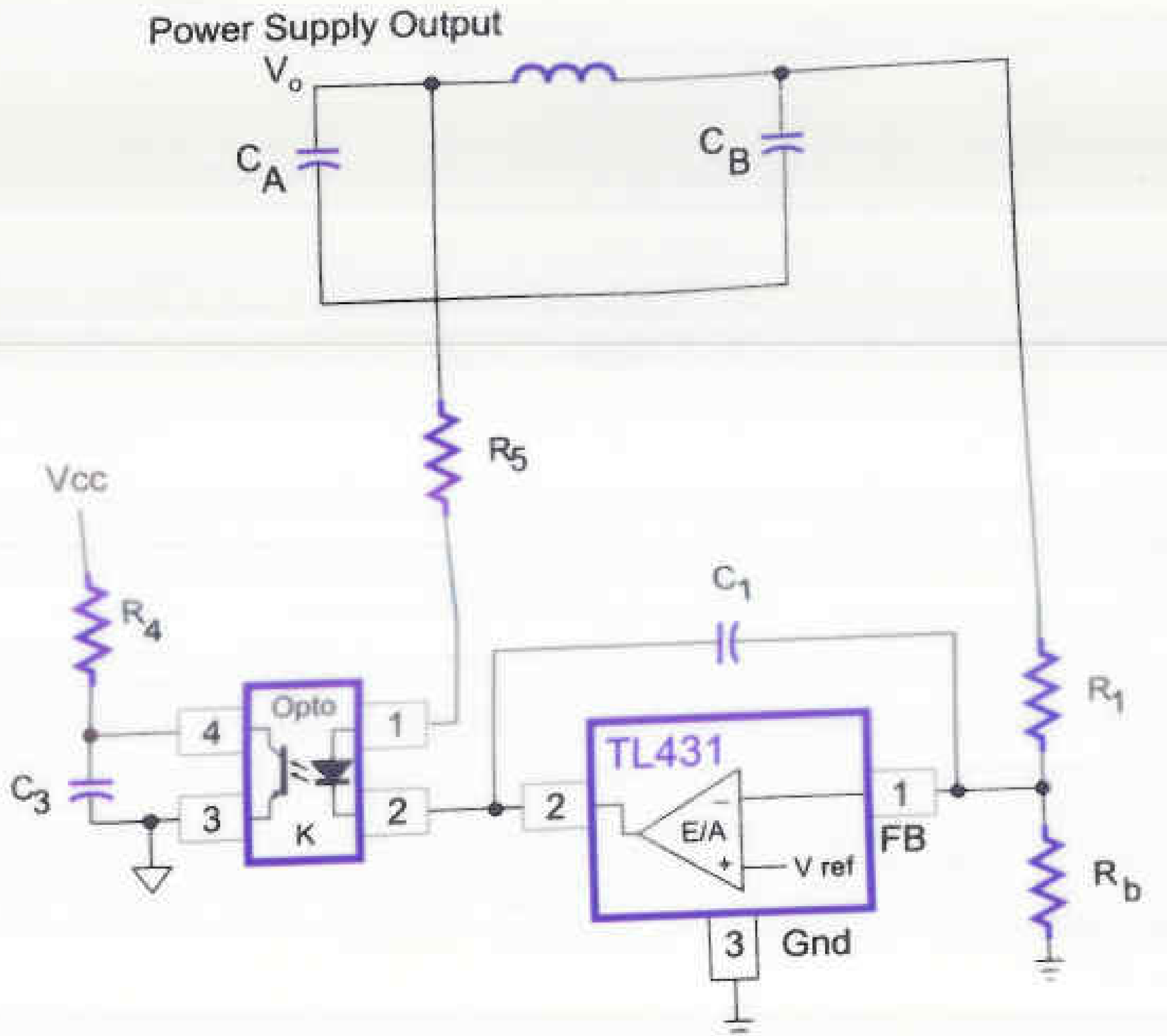


Figure 9a: Typical TL431 Configuration with Second-Stage Filter